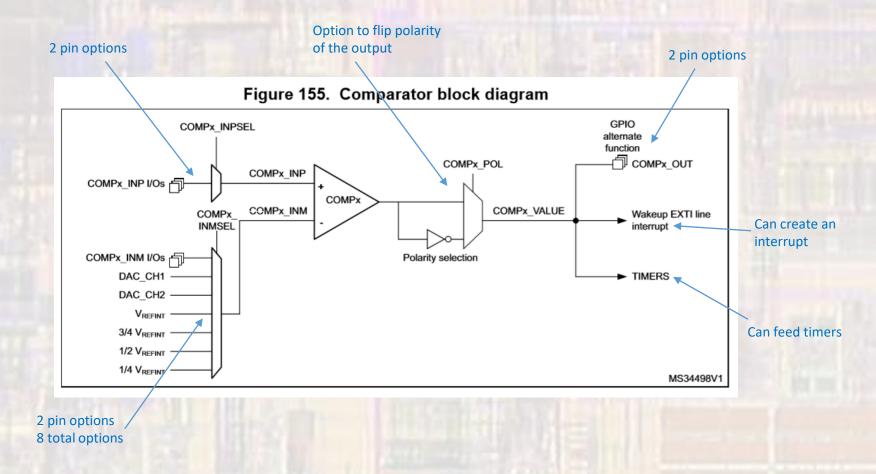
Last updated 6/23/21

- Comparators
  - Nucleo-L476RG has two high speed comparators
    - Mbed does not support the comparators
    - We will need to write our own low-level code

Comparator Configuration



#### Comparator Connections - Inputs

- Nucleo-L476RG uses programmable I/O selection to choose the INP and INM connections
- Multiple steps are required to enable these connections
  - Port(s) must be enabled (clocks enabled)
  - Pins must be selected as Analog Inputs (using the Pin I/O configuration registers)
  - Pins must be selected in the COMPx registers

Table 143. COMP1 in	nput plus assignment			
COMP1_INP	COMP1_INPSEL			
PC5	0			
PB2	1			
Table 144. COMP1 in	put minus assignment			
COMP1_INM	COMP1_INMSEL[2:0]			
¼V <sub>REFINT</sub>	000			
½ V <sub>REFINT</sub>	001			
¾ V <sub>REFINT</sub>	010			
V <sub>REFINT</sub>	011			
DAC Channel1	100			
DAC Channel2	101			
PB1	110			
PC4	111			

Table 145. COMP2 in	nput plus assignment			
COMP2_INP	COMP2_INPSEL 0			
PB4				
PB6	1			
Table 146. COMP2 in	put minus assignment			
COMP2_INM	COMP2_INMSEL[2:0]			
%V <sub>REFINT</sub>	000			
½ V <sub>REFINT</sub>	001			
¾ V <sub>REFINT</sub>	010			
V <sub>refint</sub>	011			
DAC Channel1	100			
DAC Channel2	101 110			
PB3				
P87	111			

- Comparator Connections Output
  - Nucleo-L476RG uses programmable I/O selection for the OUT connection
  - Multiple steps are required to enable these connections
    - Port must be enabled (clocks enabled)
    - Pins must be configured to allow Alternate Function
    - The COMPx output must be selected as the alternate function

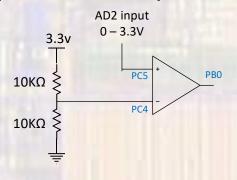
Table 18. Alternate function AF8 to AF15 <sup>(1)</sup> (continued)											
		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15		
Port		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	LCD	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTO		
	PB0	-	-	QUADSPI_BK1_IO1	LCD_SEG5	COMP1_OUT	-	-	EVENTO		
	РВ1	-	-	QUADSPI_BK1_IO0	LCD_SEG6		-	LPTIM2_IN1	EVENTO		
	PB2	-	-	-	-	-	-	-	EVENTO		
	PB3	-	-	-	LCD_SEG7	-	SAI1_SCK_B	-	EVENTO		
	PB4	UART5_RTS _DE	TSC_G2_IO1	-	LCD_SEG8		SAI1_MCLK_ B	TIM17_BKIN	EVENTO		
	PB5	UART5_CTS	TSC_G2_IO2	-	LCD_SEG9	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTO		
	PB6	-	TSC_G2_IO3	-	-	TIM8_BKIN2_ COMP2	SAI1_FS_B	TIM16_CH1N	EVENTO		
	PB7	UART4_CTS	TSC_G2_IO4	-	LCD_SEG21	FMC_NL	TIM8_BKIN_ COMP1	TIM17_CH1N	EVENTO		
Port B	<b>PB8</b>	-	CAN1_RX	-	LCD_SEG16	SDMMC1_D4	SAI1_MCLK_ A	TIM16_CH1	EVENTO		
	PB9	-	CAN1_TX	-	LCD_COM3	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTO		
	PB10	LPUART1_ RX	-	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A	-	EVENTO		
	PB11	LPUART1_TX	-	QUADSPI_NCS	LCD_SEG11	COMP2_OUT	-	-	EVENTO		
	PB12	LPUART1_ RTS_DE	TSC_G1_IO1	-	LCD_SEG12	SWPMI1_IO	SAI2_FS_A	TIM15_BKIN	EVENTO		
	PB13	LPUART1_ CTS	TSC_G1_IO2	-	LCD_SEG13	SWPMI1_TX	SAI2_SCK_A	TIM15_CH1N	EVENTO		
	PB14	-	TSC_G1_IO3	-	LCD_SEG14	SWPMI1_RX	SAI2_MCLK_ A	TIM15_CH1	EVENTO		
	PB15	-	TSC_G1_IO4	-	LCD_SEG15	SWPMI1_SUSPEND	SAI2_SD_A	TIM15_CH2	EVENTO		

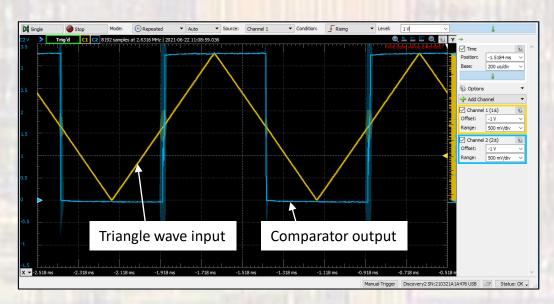
- Simple example
  - Comparator setup

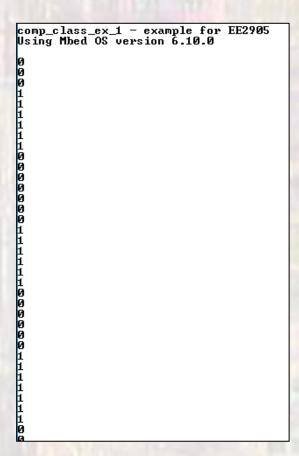
```
// comp class ex 1 project
// created 6/4/21 by ti
// rev 0
// Comparator example file for class
// shows basic comparator operation
// also shows direct register access
#include "mbed.h"
#include <stdio.h>
int main(void) {
   setbuf(stdout, NULL); // disable buffering
   // splash
   printf("comp class ex 1 - example for EE2905\n");
   printf("Using Mbed OS version %d.%d.%d\n\n",
          MBED MAJOR VERSION, MBED MINOR VERSION, MBED PATCH VERSION);
   // Using PC5 as the + input, PC4 as the - input, and PB0 as the output
   // Must enable PortC to access the comparator inputs
   // RCC AHB2ENR bit 2 for port C
   RCC->AHB2ENR |= 0x04;
   // Set inP(PC4) and inM(PC5) to analog in mode
   GPIOC->MODER |= 0x00000F00;
```

```
// Must enable PortB AND enable it's alternate function to access the
   // comparator output
   // RCC AHB2ENR bit 1 for port B
   RCC->AHB2ENR |= 0x02;
   // Set PBO to alternate function
   // 10 to bits 1-0
   GPIOB->MODER = (GPIOB->MODER | 0x00000002) & ~0x00000001;
   // Select alternate function 12 - comparator output
  // 1100 to bits 3-0
   // NOTE: documentation calls this AFRL
   GPIOB -> AFR[0] = 0x0000000C;
  // Enable comparator peripheral clock
   // APB2 (high speed APB)
   // RCC APB2ENR, 1 to bit 0 to enable
   RCC->APB2ENR |= 0x00000001:
   // Setup COMP1 values
   // INP - PC5, 0 to bit 7
   // INM - PC4, 111 to bits 6-4
  // On, 1 to bit 0
   // all others 0
   COMP1->CSR = 0x00000071:
   while (1) {
       // Read from the comparator output value
       // This is what is sent to the output pin
       // output register, bit 30
       printf("%x\n", (COMP1->CSR & 0x40000000) && 1);
       wait us(10000);
   }// end while
   return 0:
}// end main
```

- Simple example results
  - Comparator setup







- Simple example results
  - Comparator setup

