Inter-Integrated Circuit (I2C) Basics

also commonly called Two Wire Interface (TWI)

Last updated 6/21/21

- Overview
 - 8 bit synchronous shift register used to communicate externally
 - 9 bit total communication packet
 - uni-directional
 - Most often used to communicate with peripherals
 - displays, sensors, converters
 - Supports multiple masters and multiple slaves
 - 4 modes of operation
 - Master Receive
 - Master Transmit
 - Slave Receive
 - Slave Transmit

- Overview
 - Open drain configuration
 - outputs only pull down
 - pull up resistors or current sources pull up



- I2C Timing
 - SDA data line
 - SCL clock line
 - Data must be valid during the entire positive clock cycle time



- I2C Timing
 - Special timing requirements for
 - start transmission
 - stop transmission
 - repeated start transition
 - master does not relinquish the bus in this mode



- I2C Timing
 - Addressing
 - Indicate which slave to transmit to or receive from by first transmitting the "address" of the desired device
 - Often this value is hardwired via external pins on the slave device
 - 7 bits for each address



I2C Timing

- R/W bit indicates a read or write operation is to follow
 - Read is active high
- ACK Acknowledge
 - The master drives the data bus from start through the R/W bit and then releases the bus
 - The slave then pulls down the bus in the last clock cycle to indicate a completed transmission



- I2C Timing
 - ACK cont'd
 - If the master fails to see the slave pull down the bus in the 9th clock cycle (NACK) no acknowledge
 - Transmission failed
 - Some sort of error action is required



- I2C Timing
 - Data packet
 - After getting an ACK on the address data can be sent
 - 8 bits of data
 - 1 bit for a data ACK
 - This can be repeated many times



- Multi-Master Arbitration
 - First master that attempts to transmit a 1 when the other transmits a 0 – loses arbitration and shuts off

