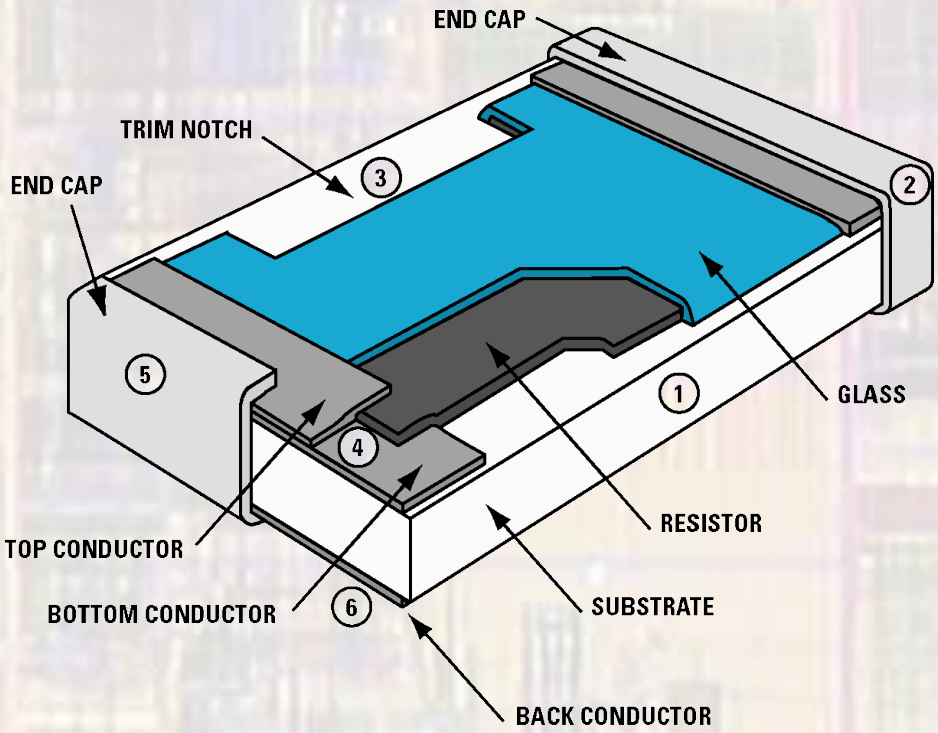
Packaging

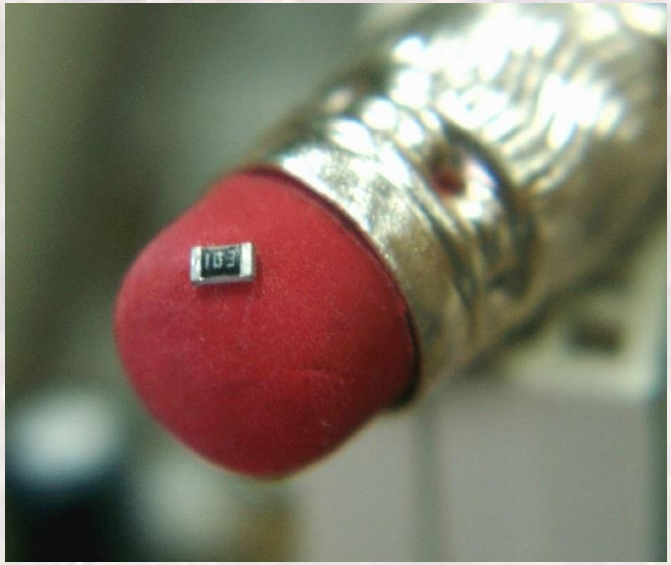
Last updated 6/23/21

Packaging

- Chip Resistor

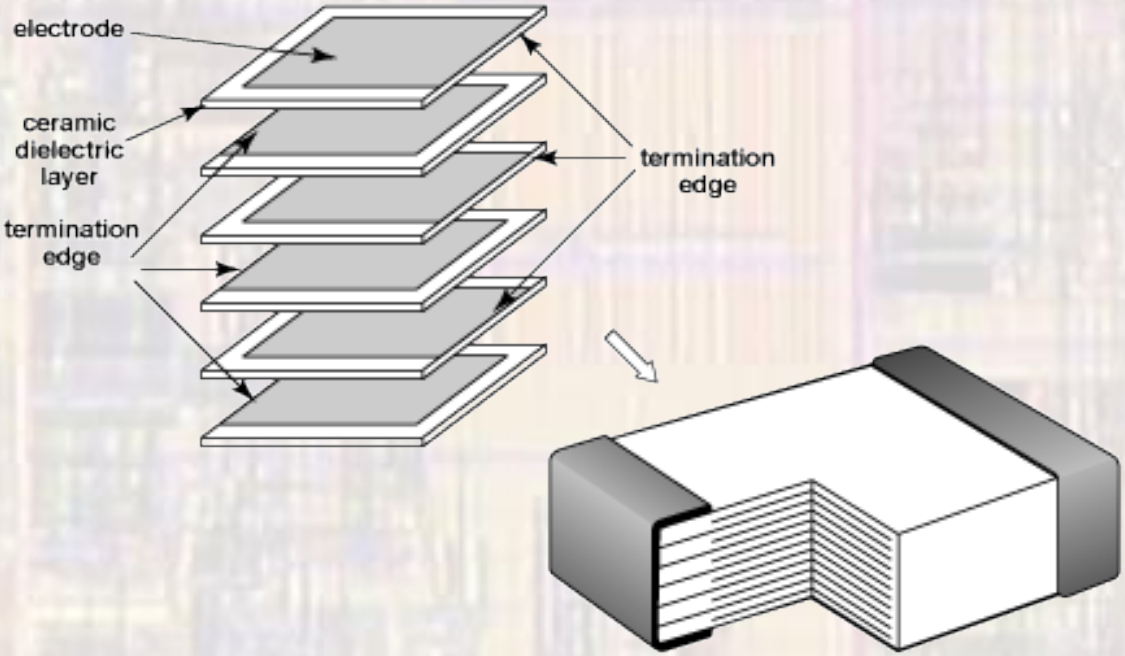


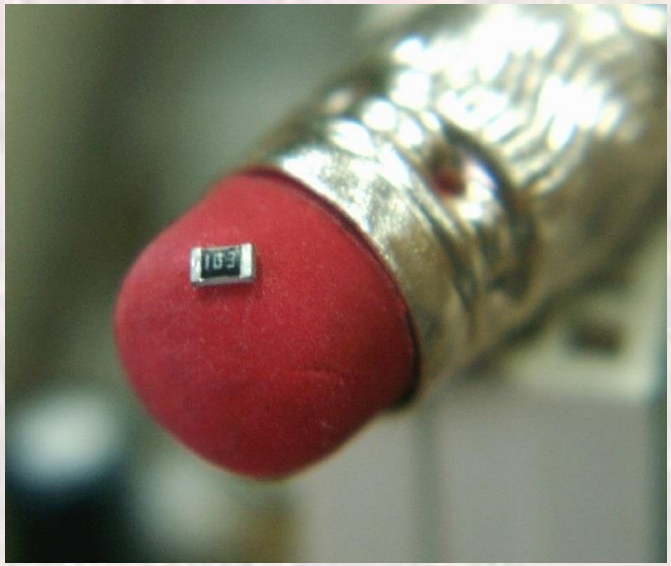
ANATOMY OF A HIGH RELIABILITY THICK FILM CHIP RESISTOR

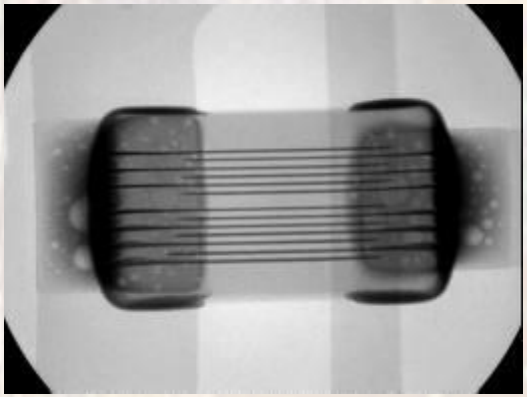


Packaging

- Chip Capacitor

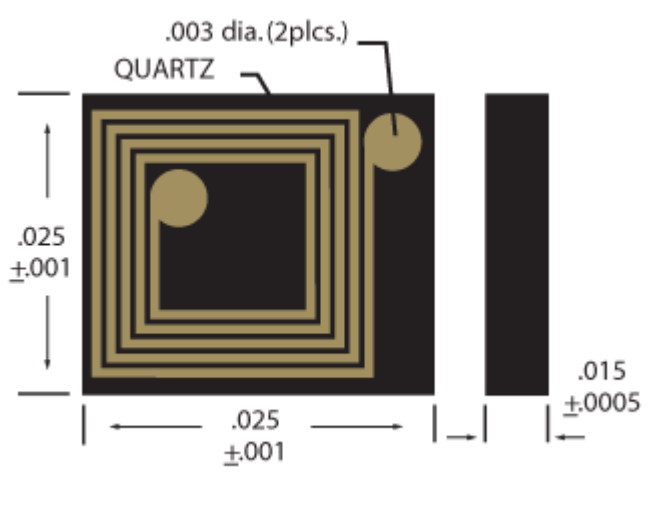


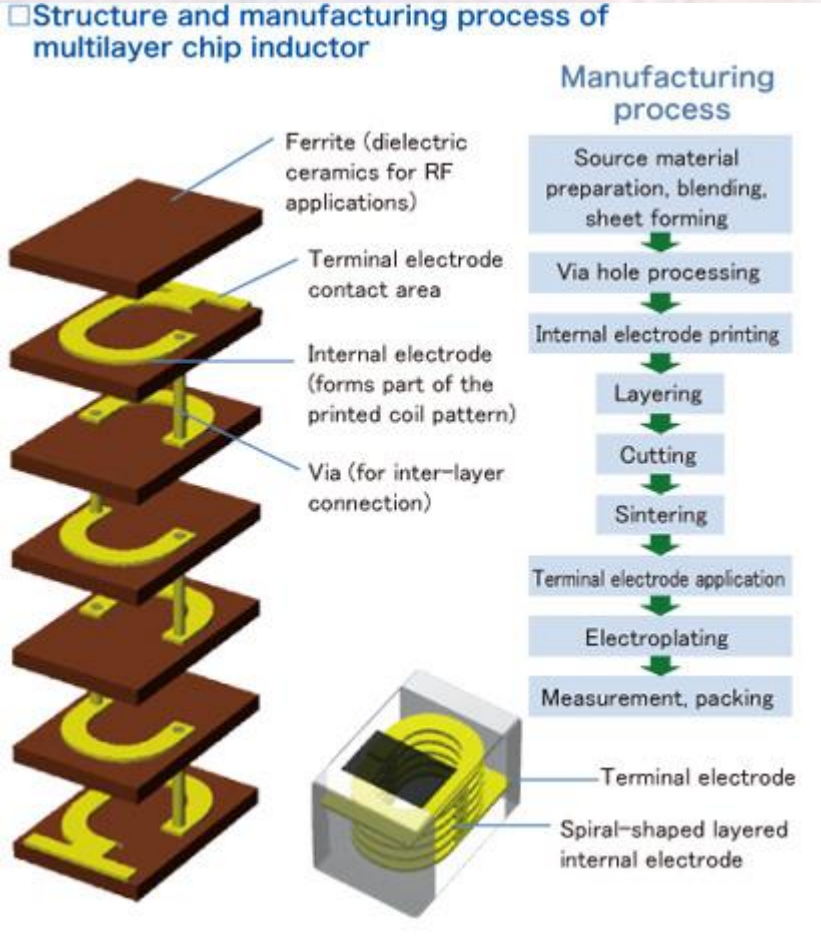




System Design

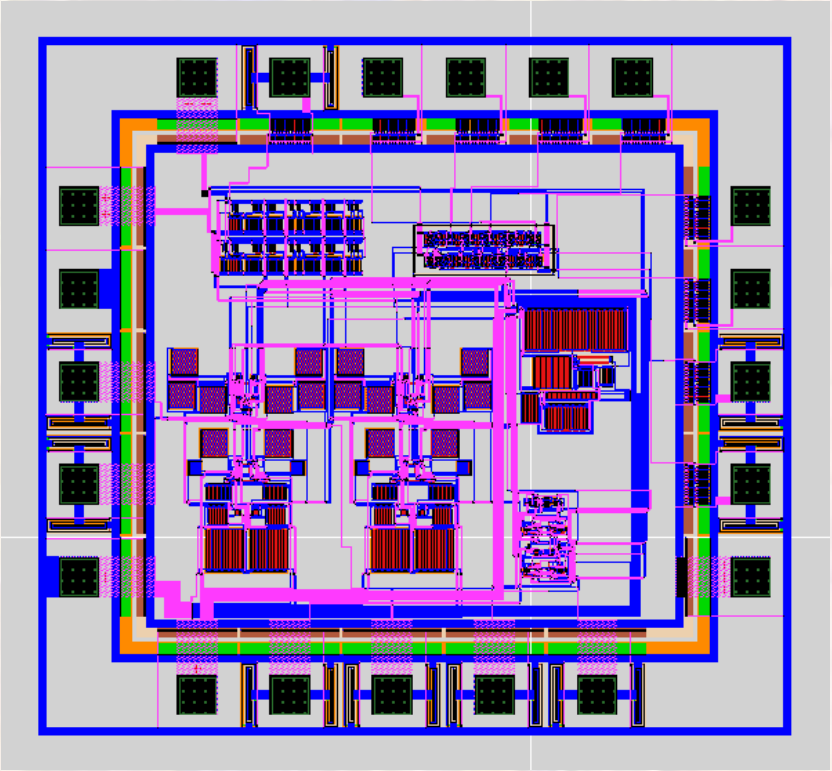
- Chip Inductor

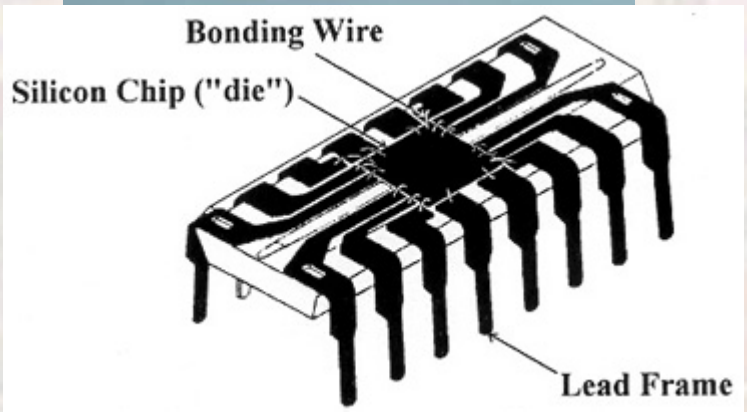




Packaging

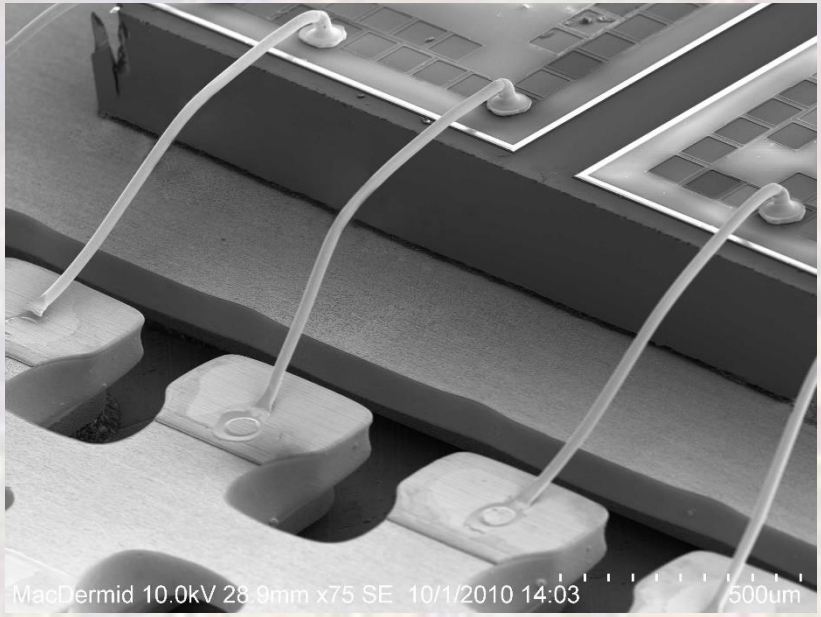
- Die Bond Pad
  Lead Frame

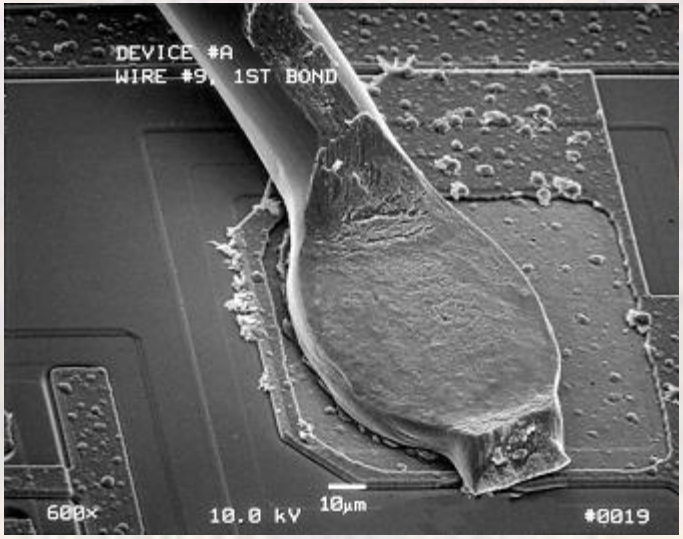


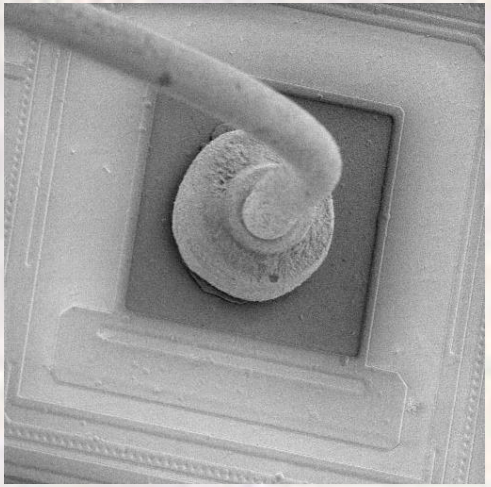


Packaging

- Die Bond Pad







Packaging

- Die Bond Pad

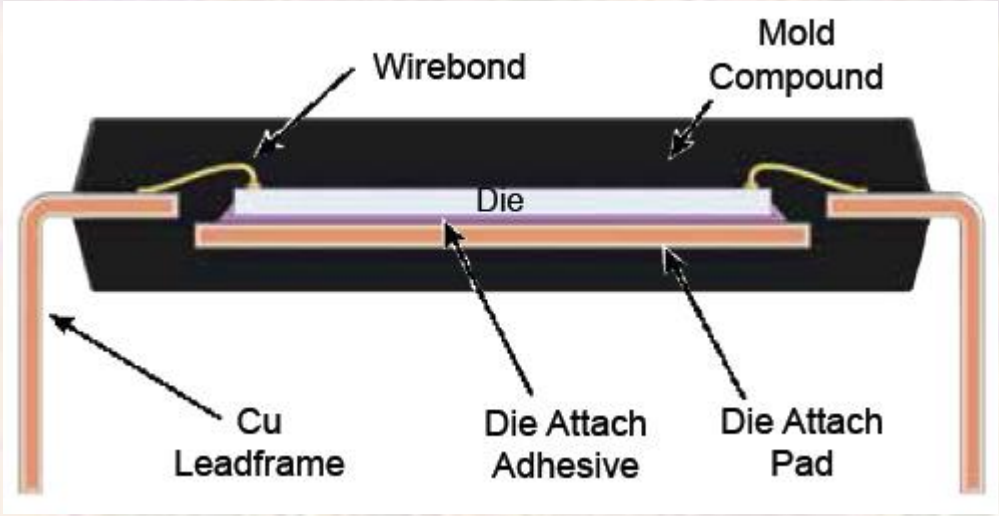
video

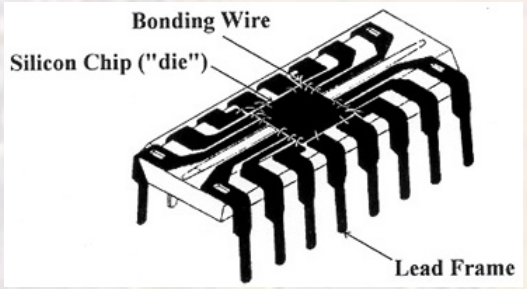
Packaging

- TO – Transistor Outline

Packaging

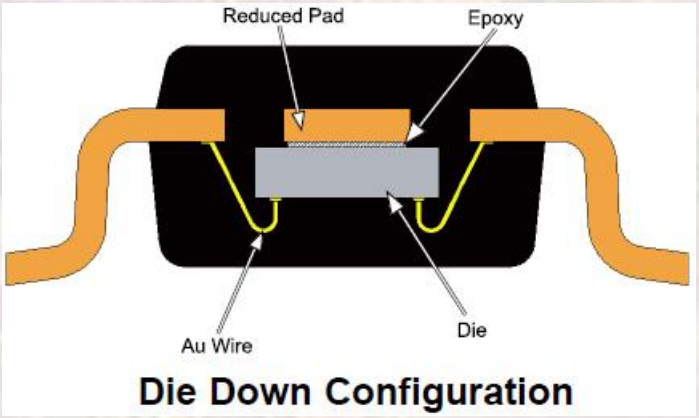
- PDIP – Plastic Dual Inline Package





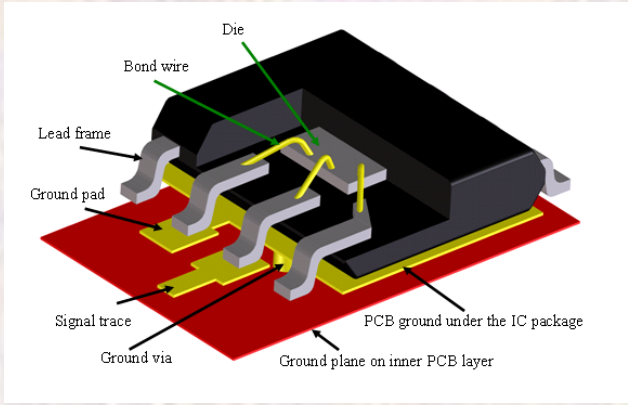
Packaging

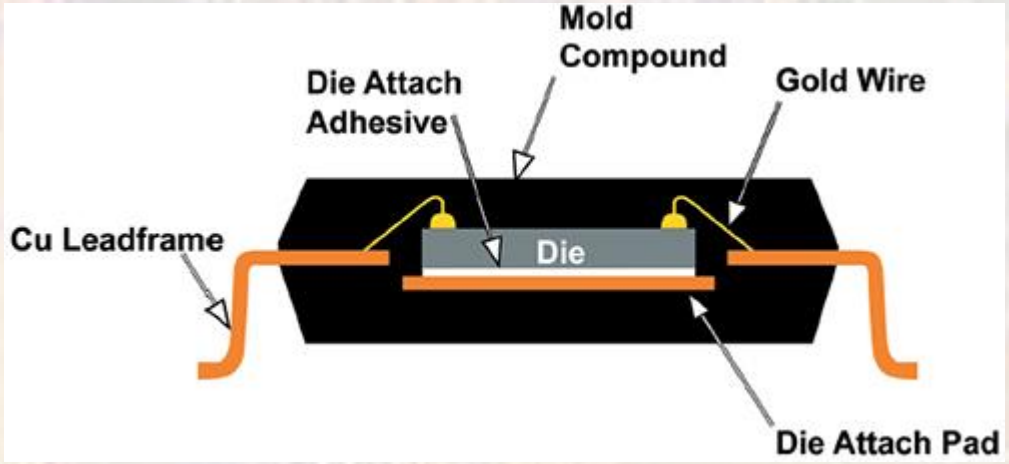
- SOT – Standard Outline Transistor



Packaging

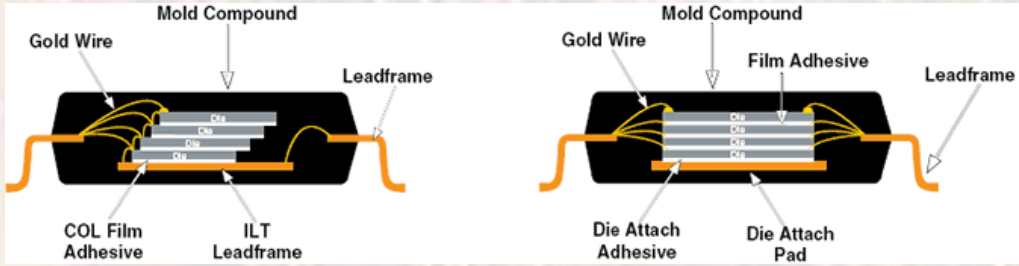
- SSOP – Shrink Small Outline





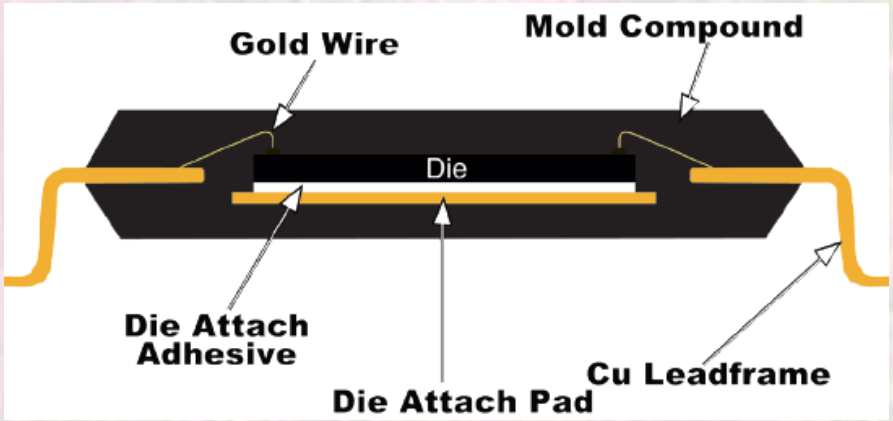
Packaging

- TSOP – Thin Small Outline



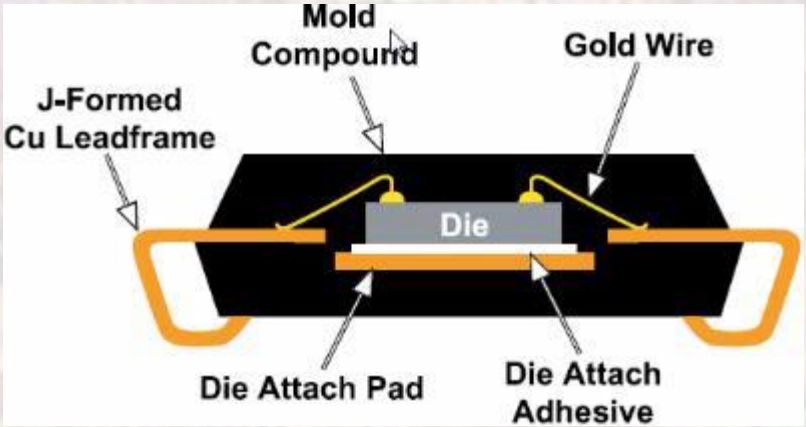
Packaging

- TQFP – Thin Quad Flat



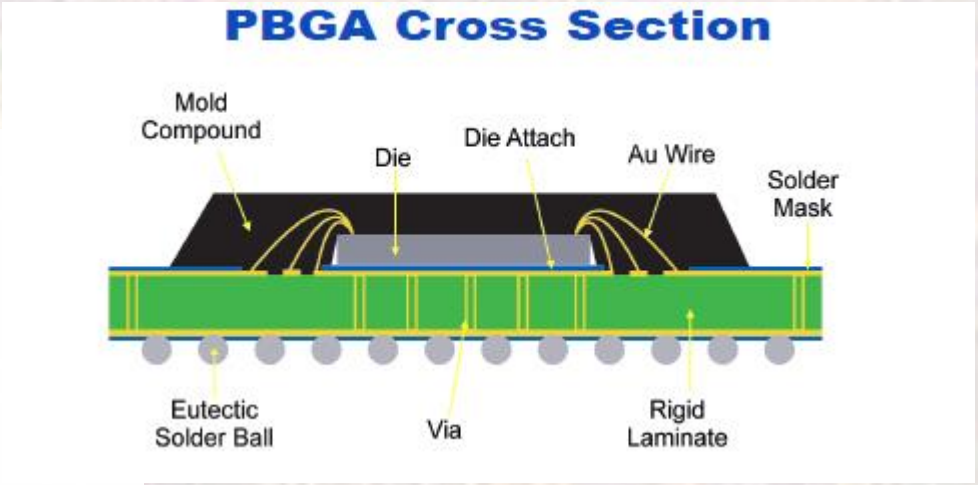
Packaging

- PLCC – Plastic Leaded Chip Carrier



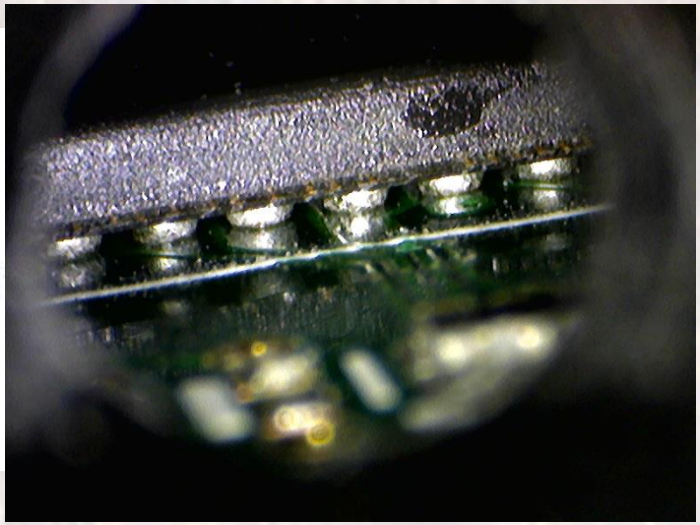
Packaging

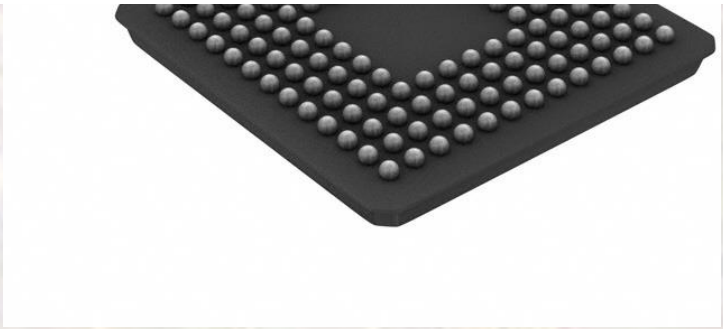
- Ball Grid Array (BGA)



Packaging

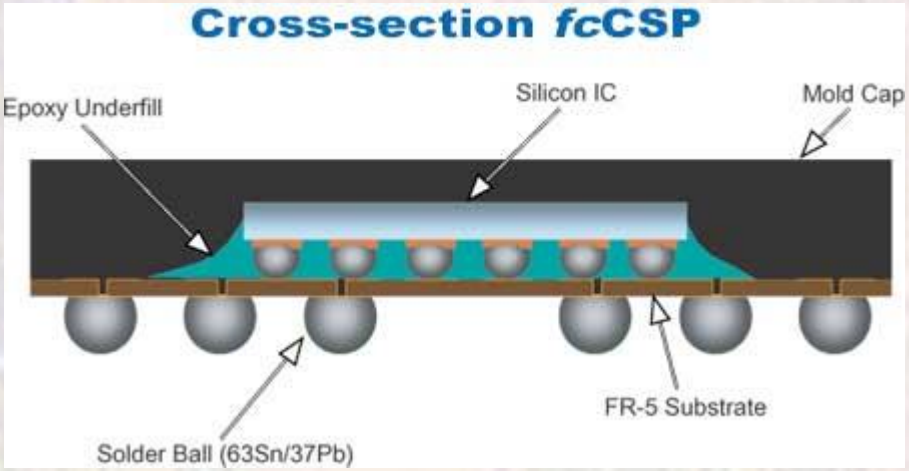
- Ball Grid Array (BGA)





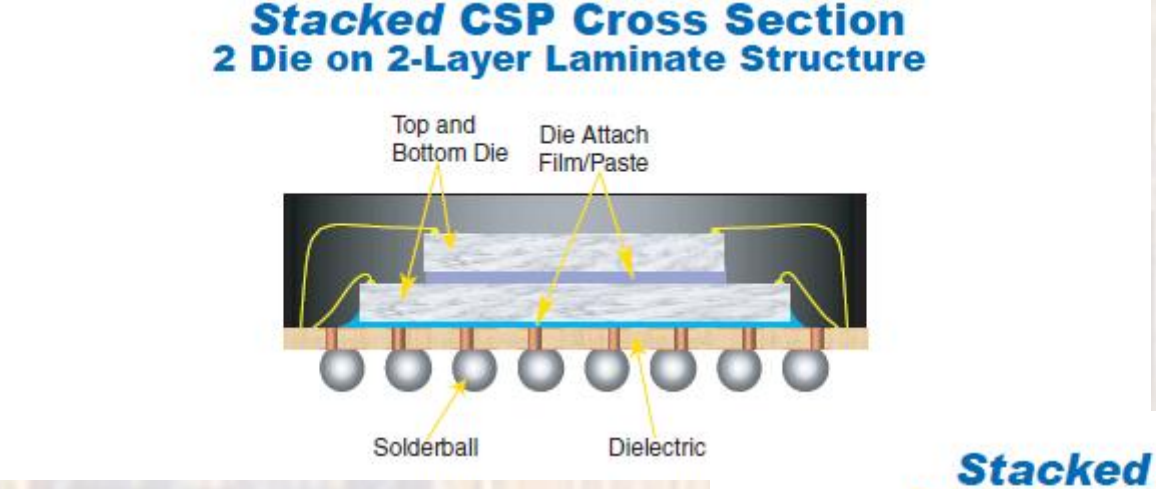
Packaging

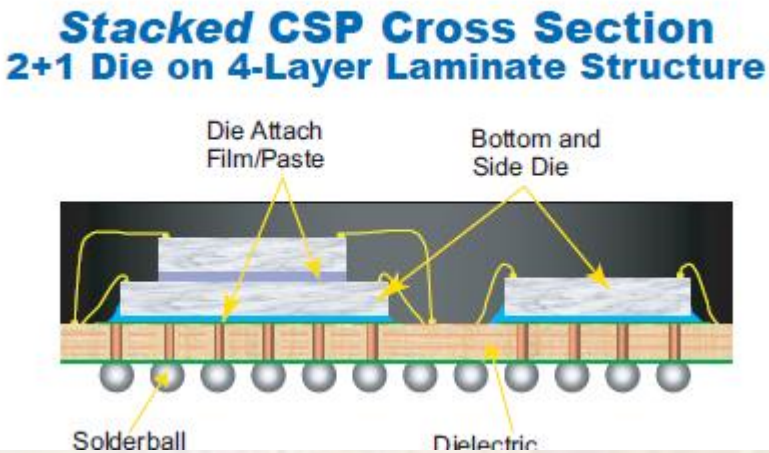
- Flip Chip BGA/CSP (Chip Scale Package)



Packaging

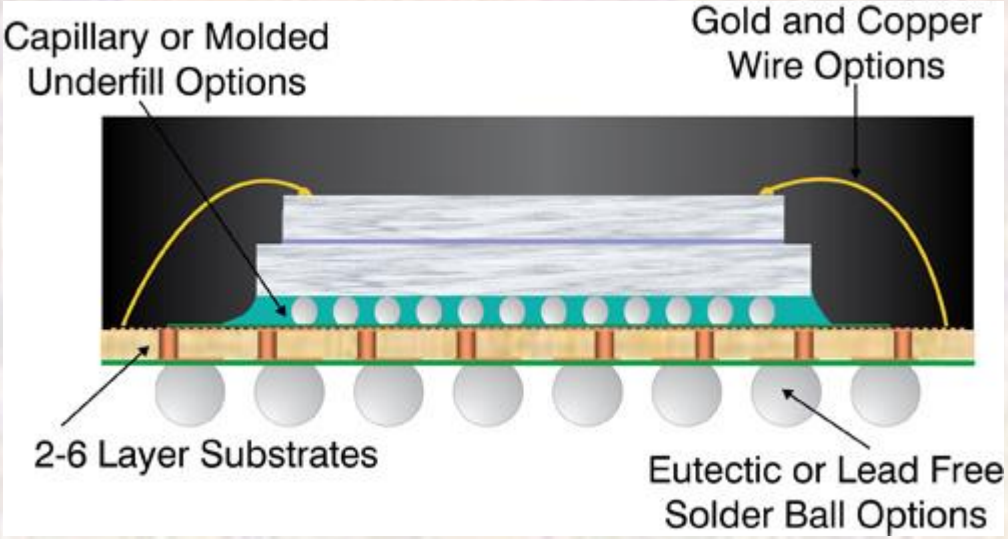
- Stacked CSP





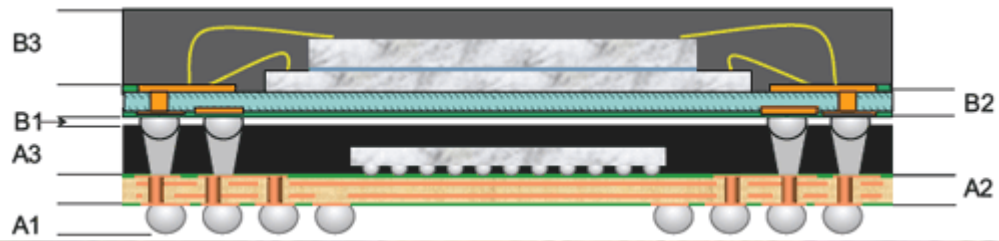
Packaging

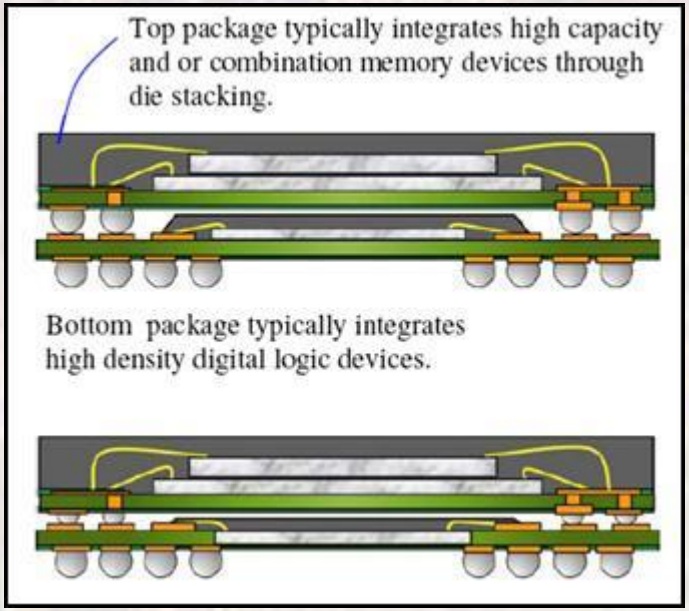
- Flip Chip Stacked



Packaging

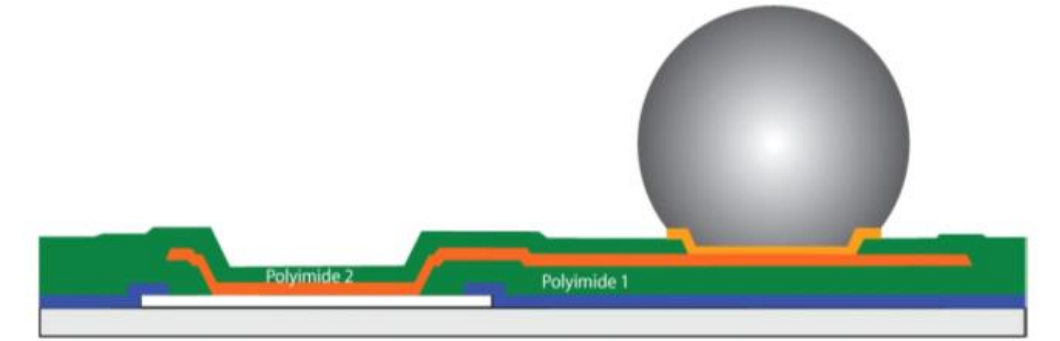
- Package on Package (PoP)



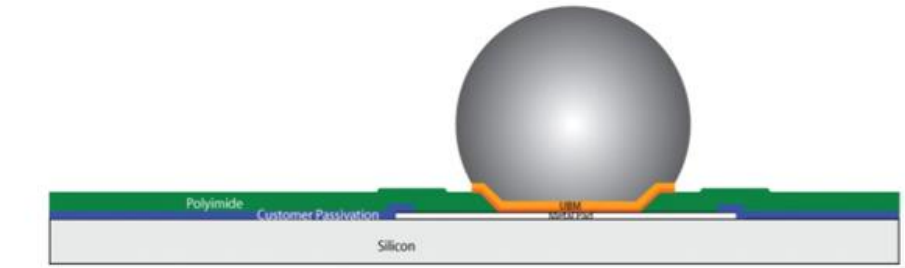


Packaging

- Wafer level CSP



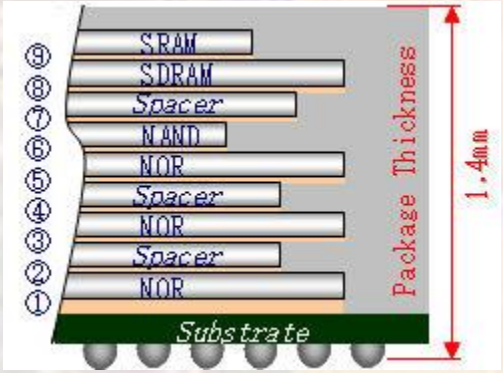
CSPnl – Bump on Redistribution

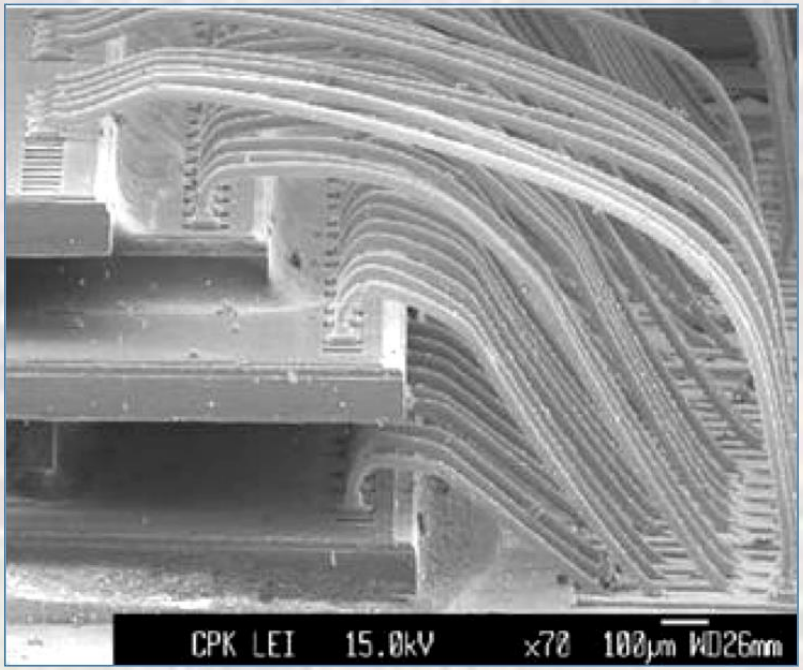


CSPnl – Bump on Repassivation

Packaging

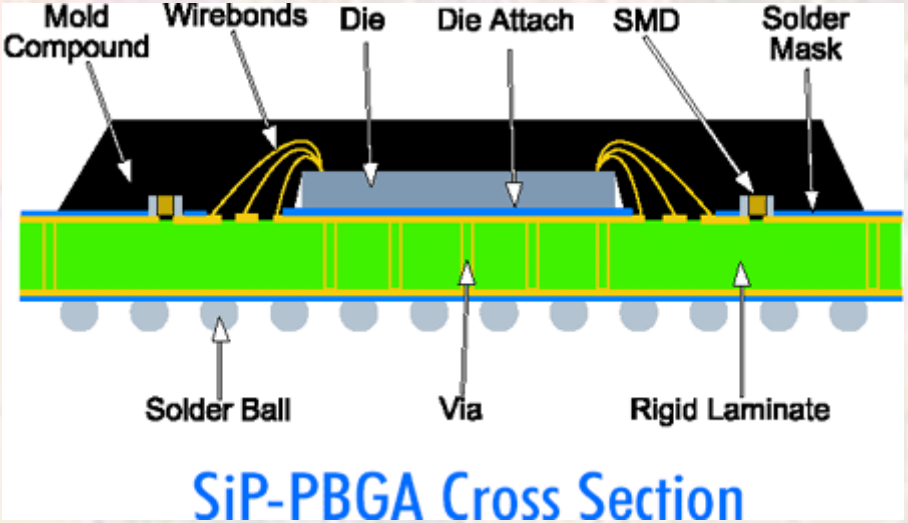
- Stacked Package





Packaging

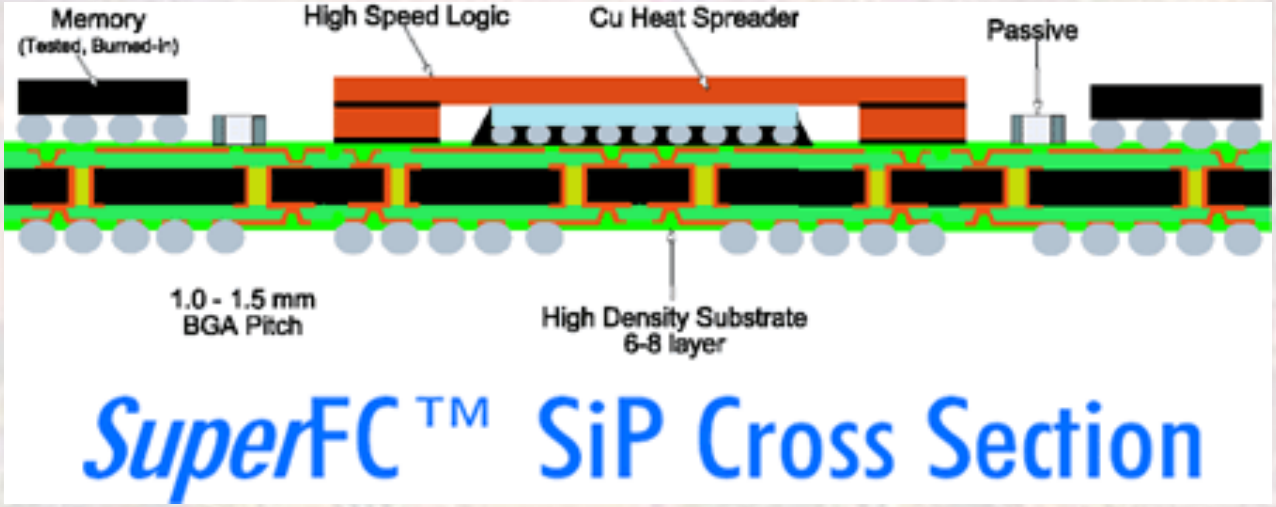
- SiP – System in Package



SiP-PBGA Cross Section

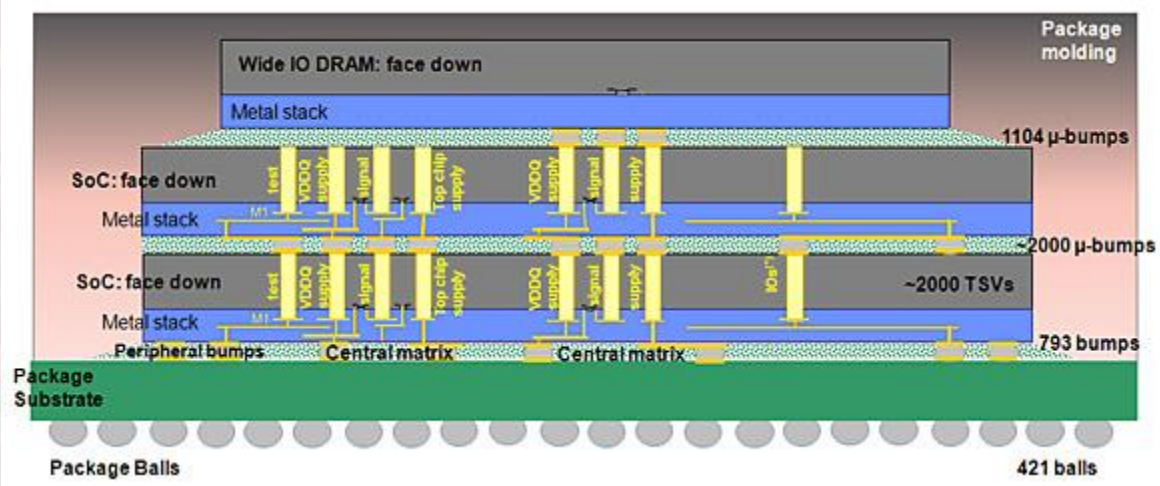
Packaging

- SiP – System in Package



Packaging

- Silicon Through Vias



Packaging

- Micro-Electro-Mechanical Device

Packaging

- SMT Carriers