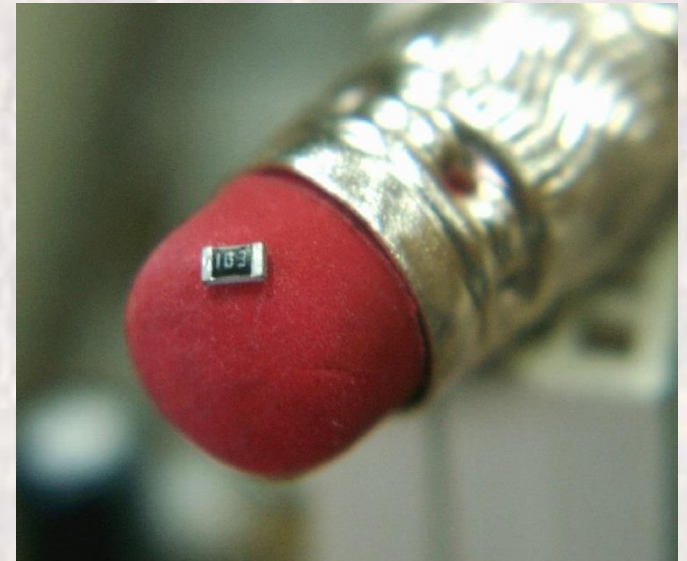
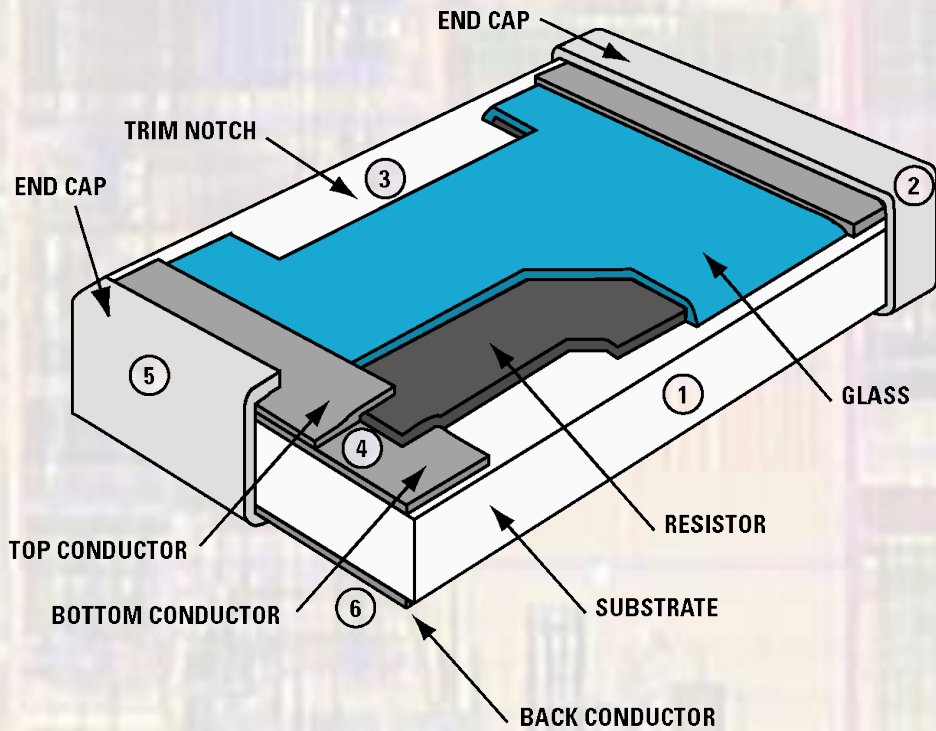


# Packaging

Last updated 6/23/21

# Packaging

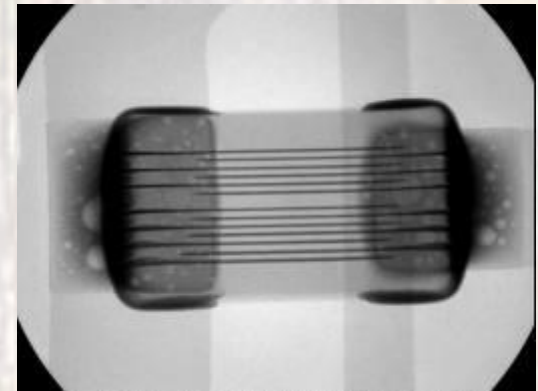
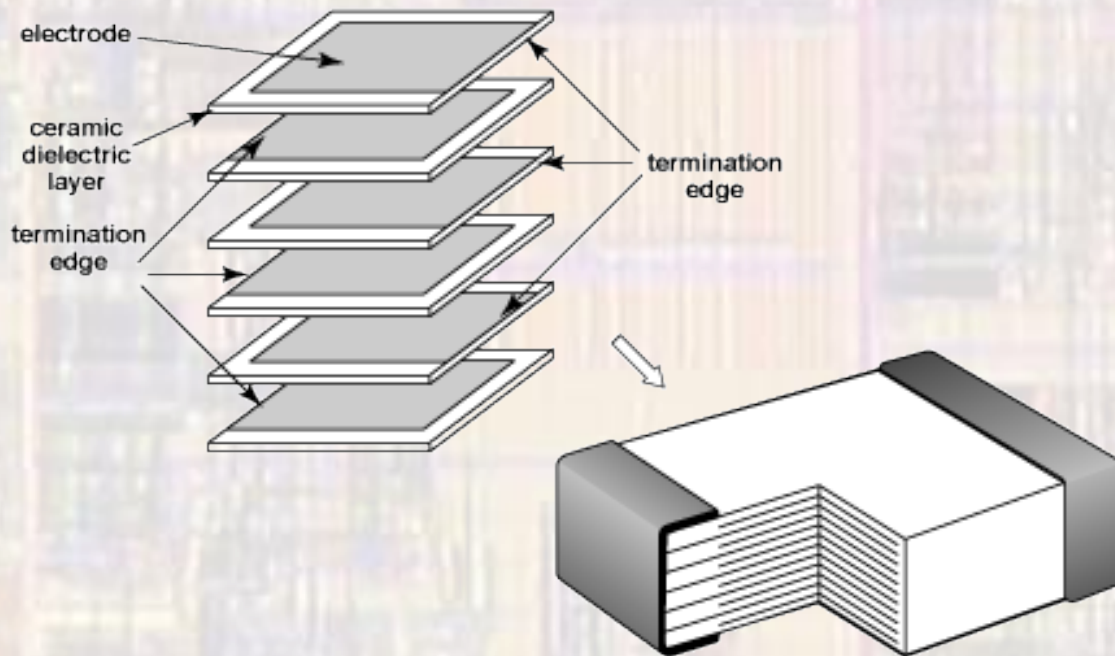
- Chip Resistor



**ANATOMY OF A HIGH RELIABILITY THICK FILM CHIP RESISTOR**

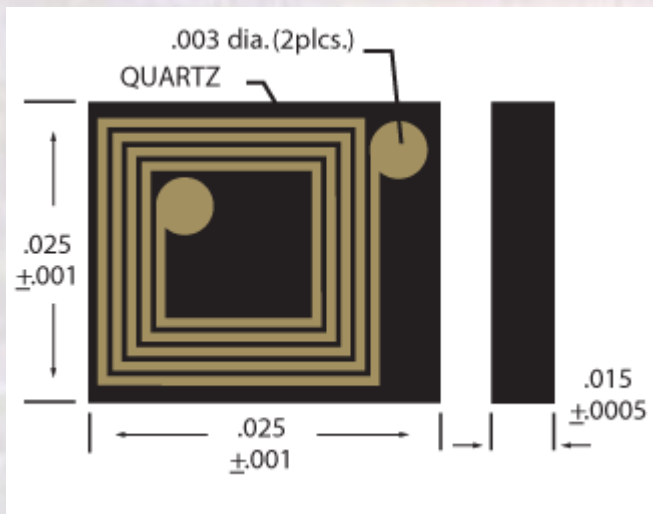
# Packaging

- Chip Capacitor

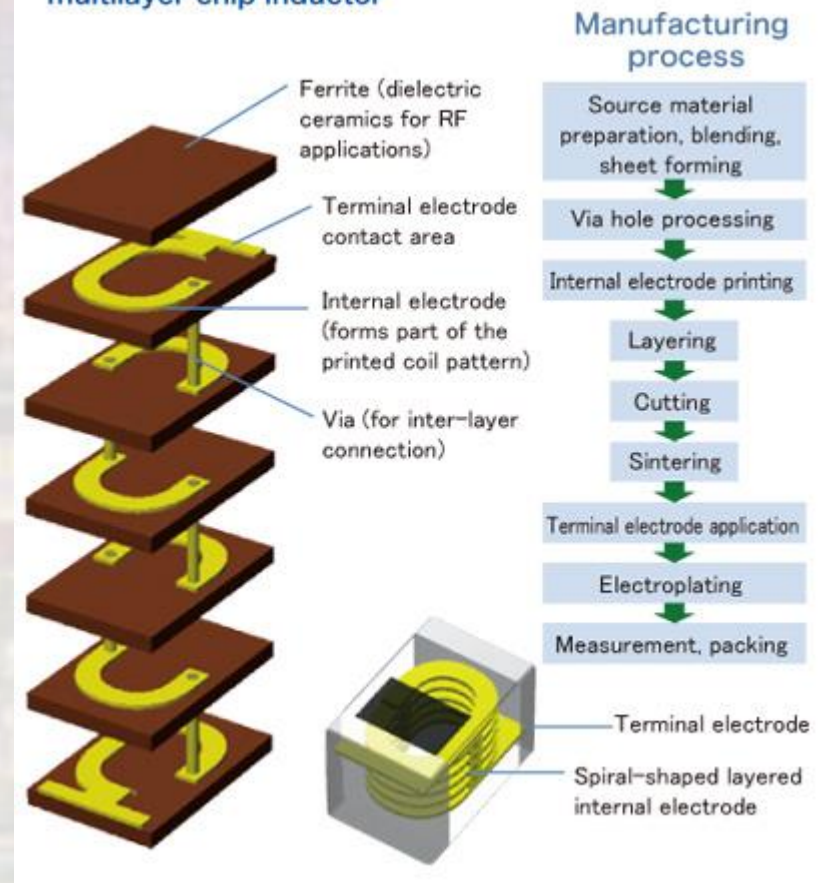


# System Design

- Chip Inductor

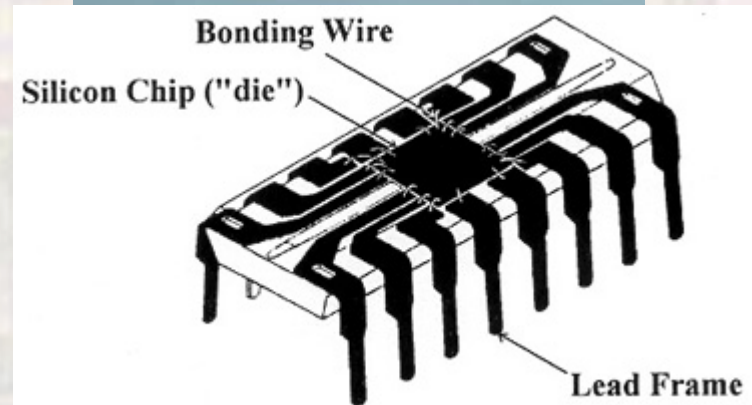
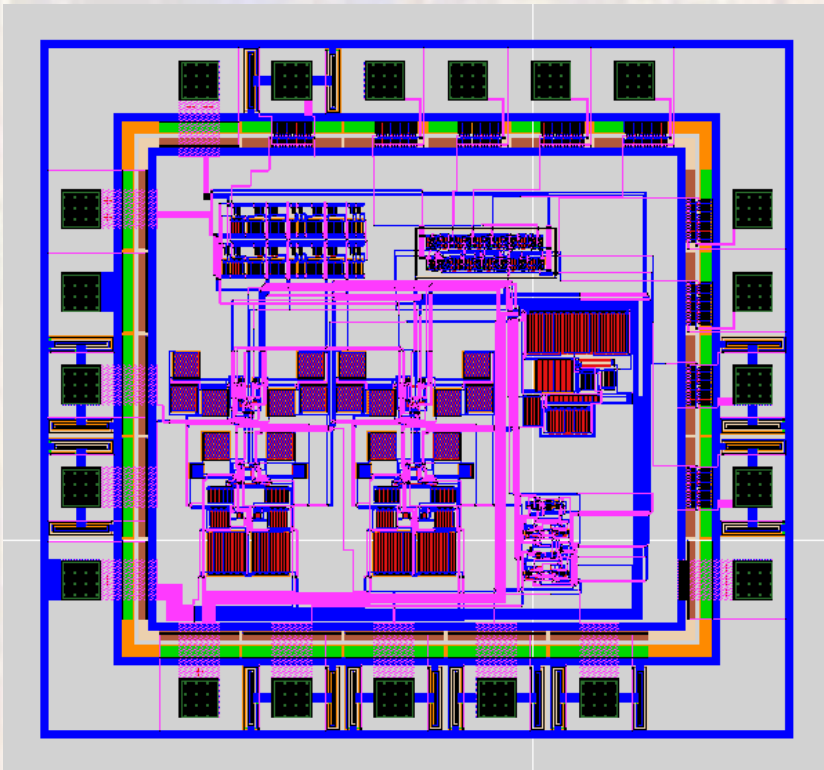


## Structure and manufacturing process of multilayer chip inductor



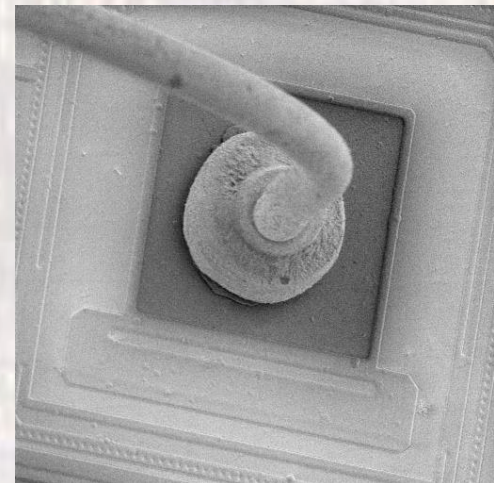
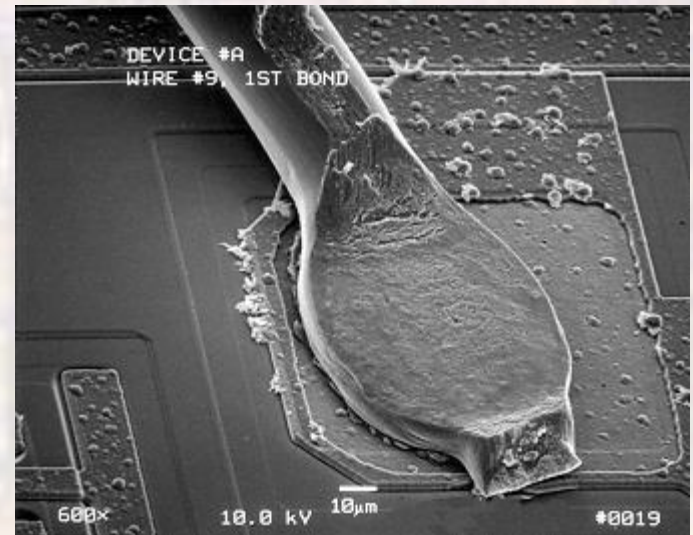
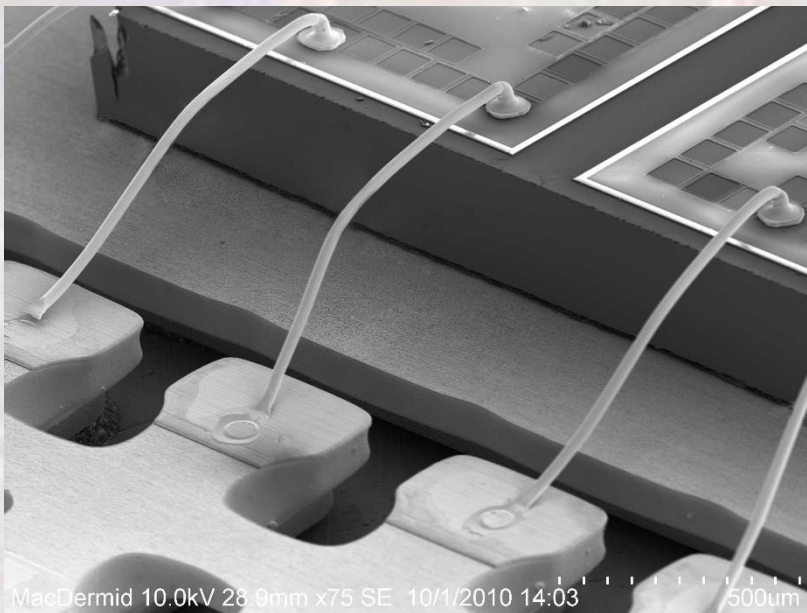
# Packaging

- Die Bond Pad  
Lead Frame



# Packaging

- Die Bond Pad



# Packaging

- Die Bond Pad

video

# Packaging

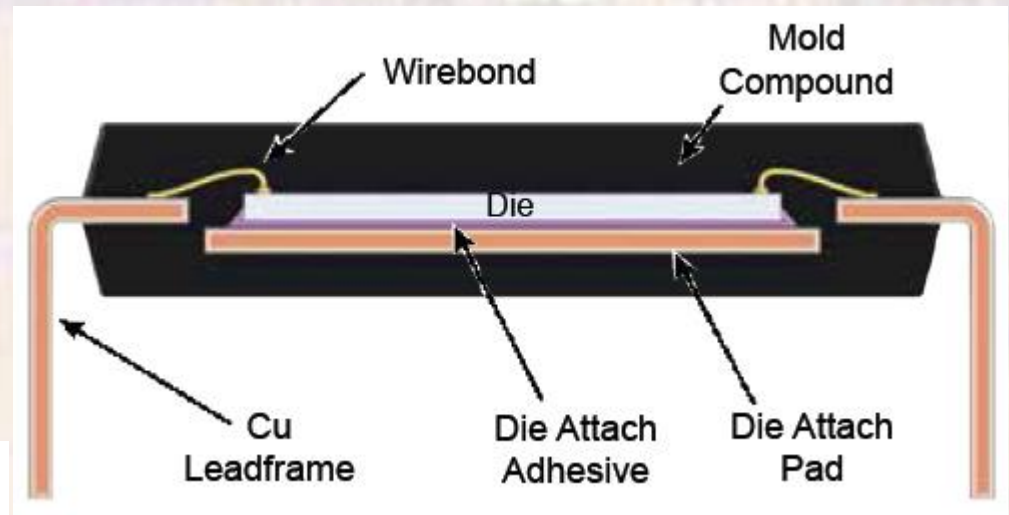
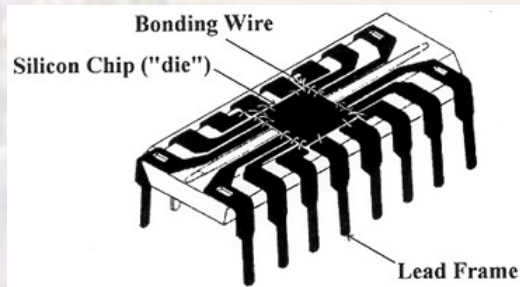
- TO – Transistor Outline





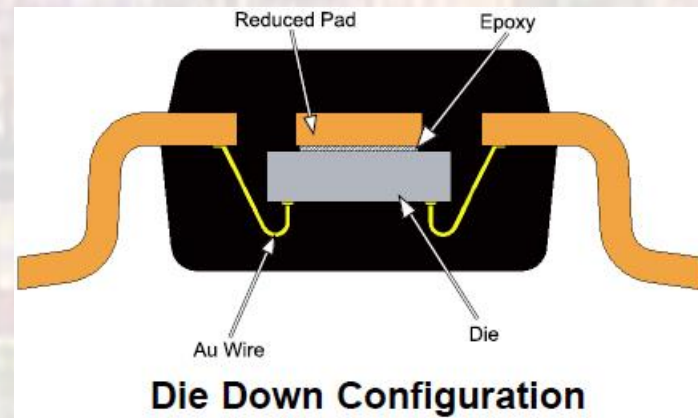
# Packaging

- PDIP – Plastic Dual Inline Package



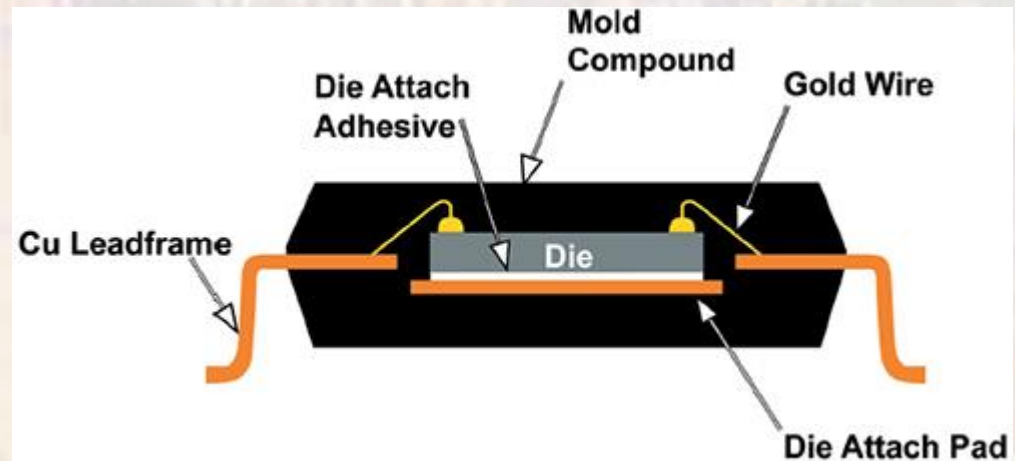
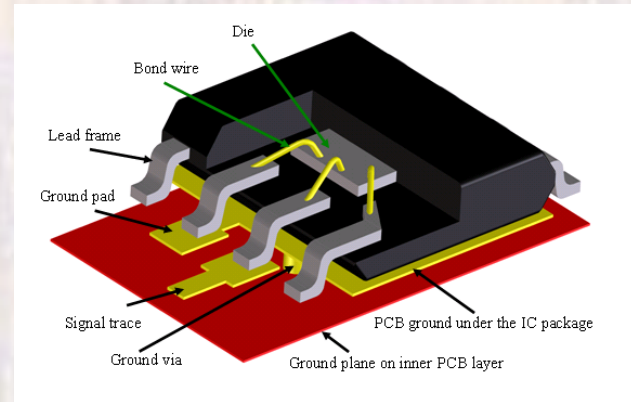
# Packaging

- SOT – Standard Outline Transistor



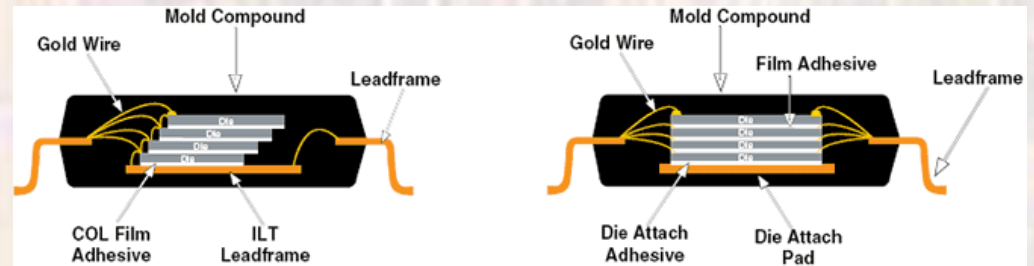
# Packaging

- SSOP – Shrink Small Outline



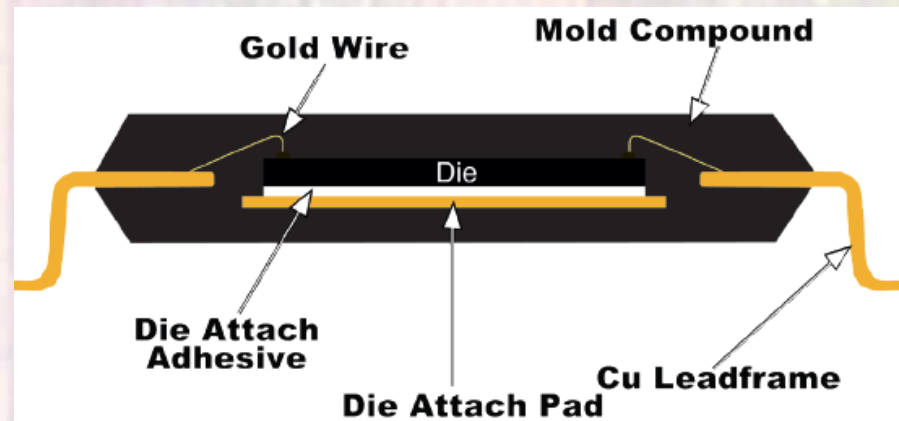
# Packaging

- TSOP – Thin Small Outline



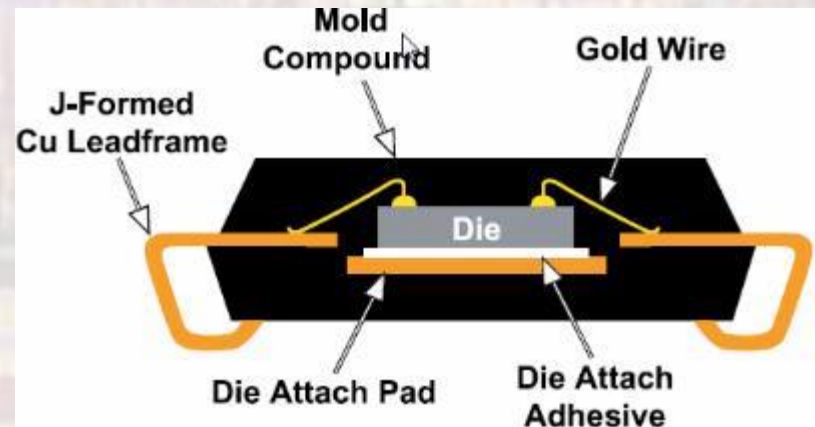
# Packaging

- TQFP – Thin Quad Flat



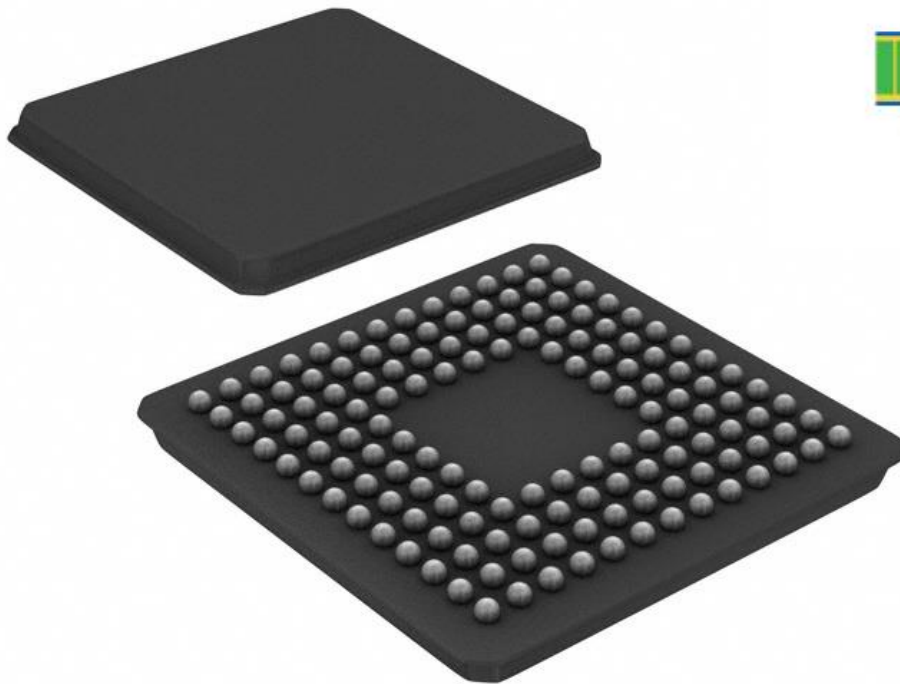
# Packaging

- PLCC – Plastic Leaded Chip Carrier

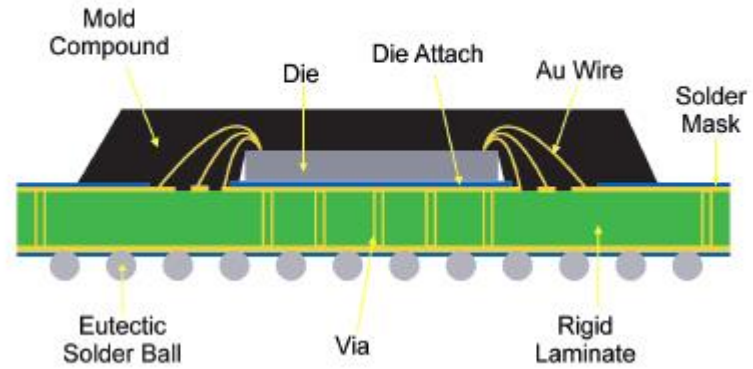


# Packaging

- Ball Grid Array (BGA)



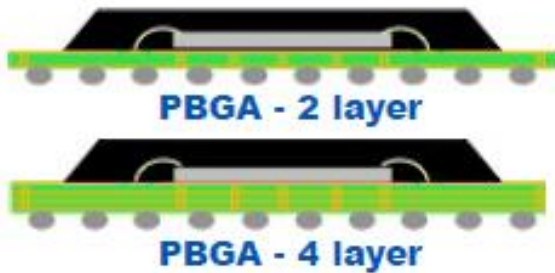
## PBGA Cross Section



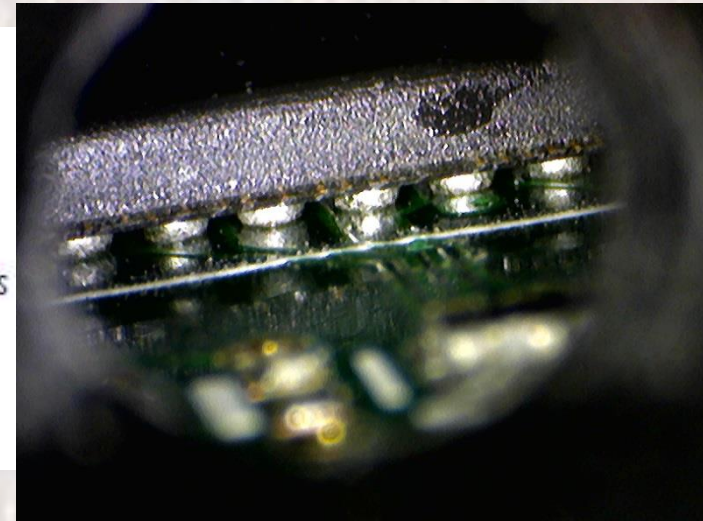
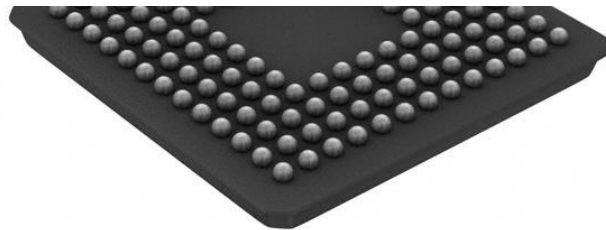
# Packaging

- Ball Grid Array (BGA)

## PBGA Standard Package Offering:



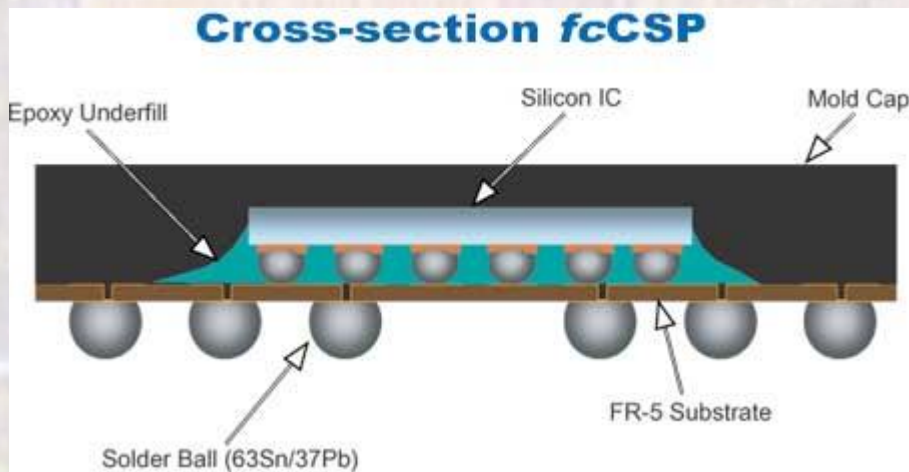
PBGA (Qualified L2AA/260°C)  
2 / 4 / 6 Layer  
4-Layer with 1oz (35 $\mu$ m) Internal Cu Planes  
Single or Multi-Die





# Packaging

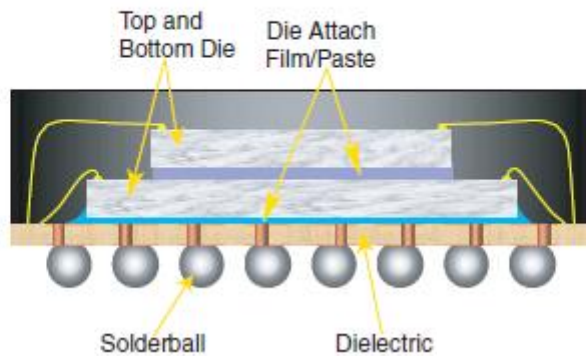
- Flip Chip BGA/CSP (Chip Scale Package)



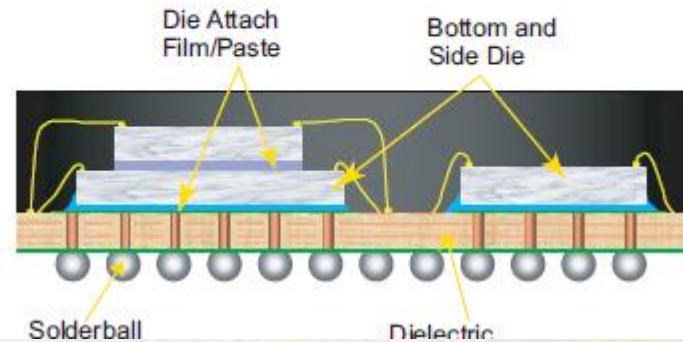
# Packaging

- Stacked CSP

**Stacked CSP Cross Section**  
**2 Die on 2-Layer Laminate Structure**

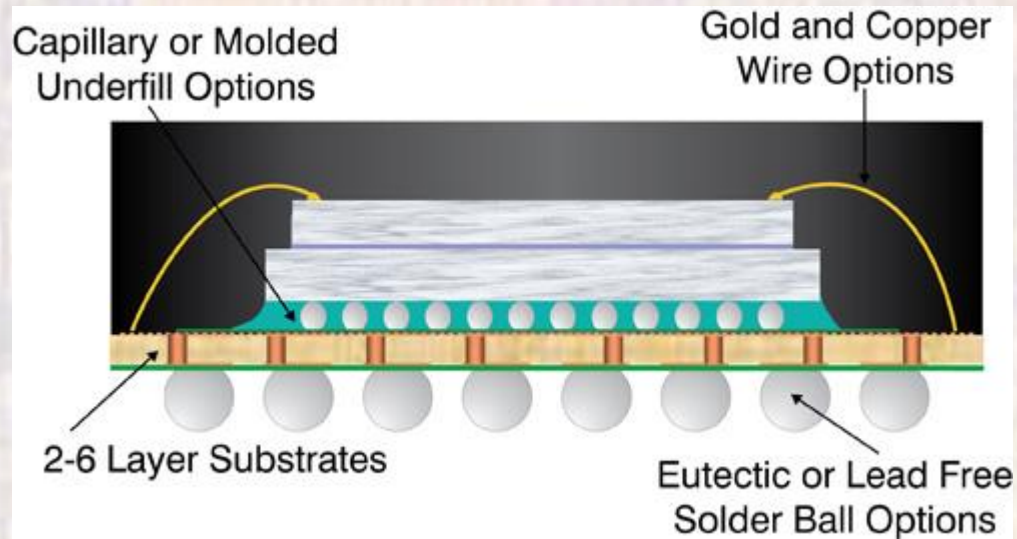


**Stacked CSP Cross Section**  
**2+1 Die on 4-Layer Laminate Structure**



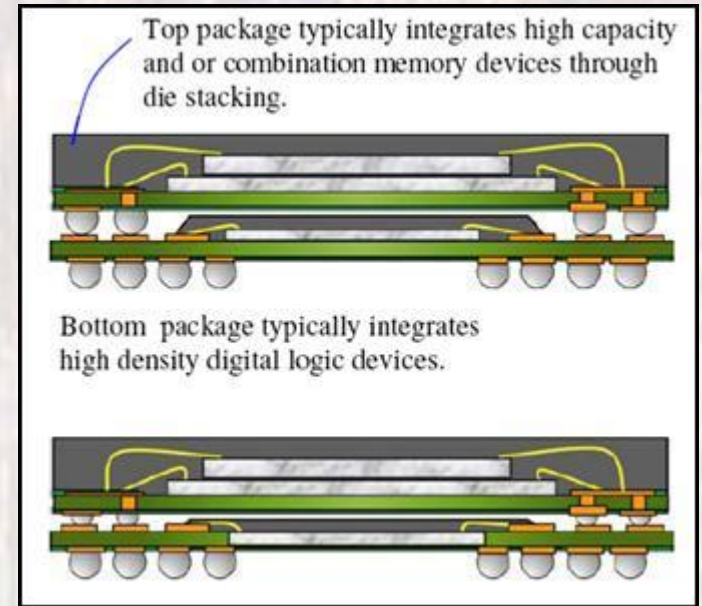
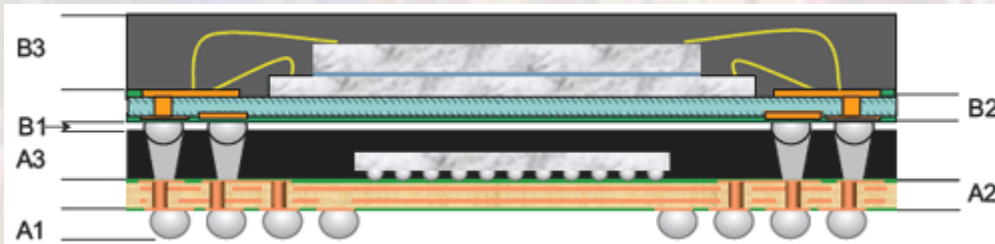
# Packaging

- Flip Chip Stacked



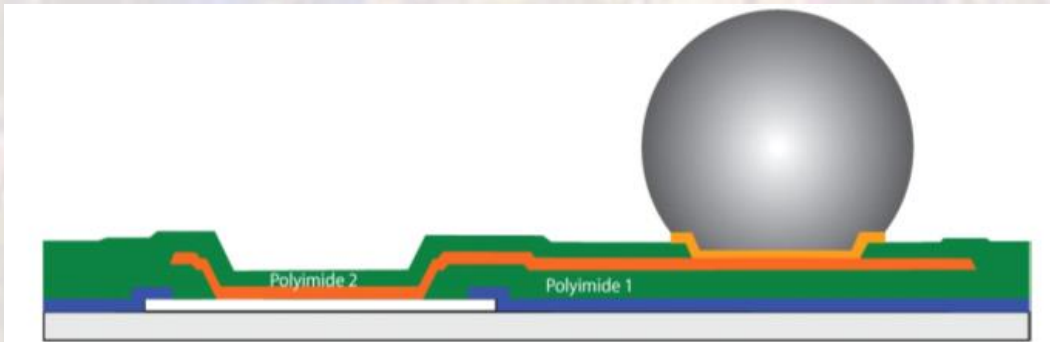
# Packaging

- Package on Package (PoP)

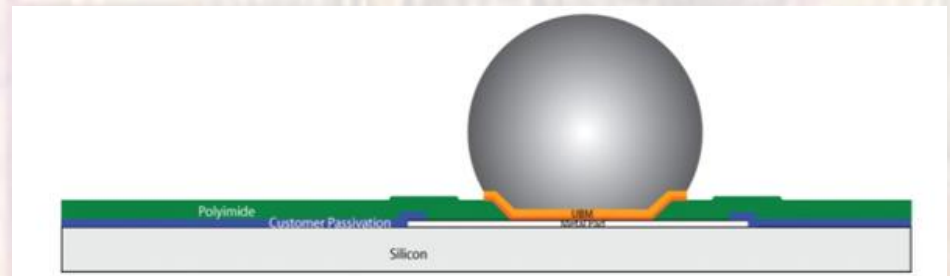


# Packaging

- Wafer level CSP



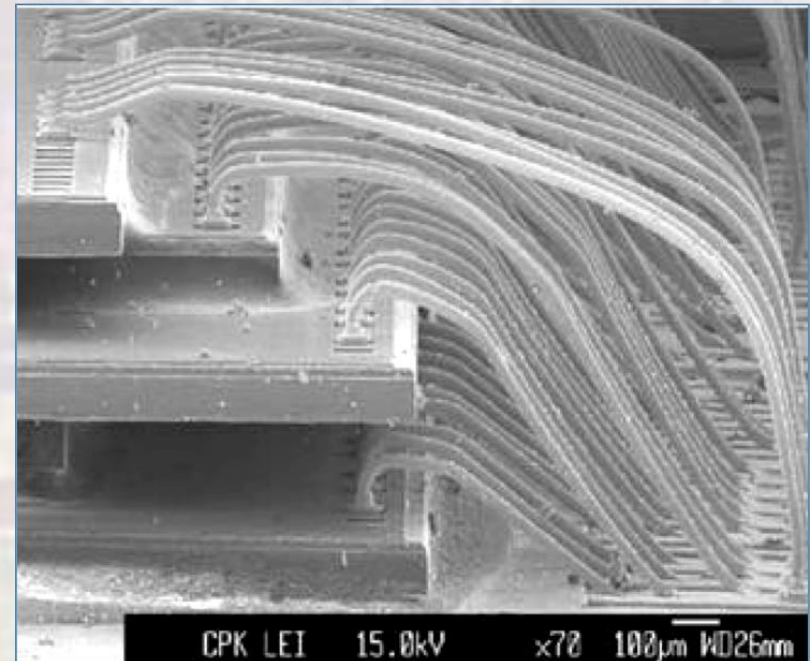
CSPnl – Bump on Redistribution



CSPnl – Bump on Repassivation

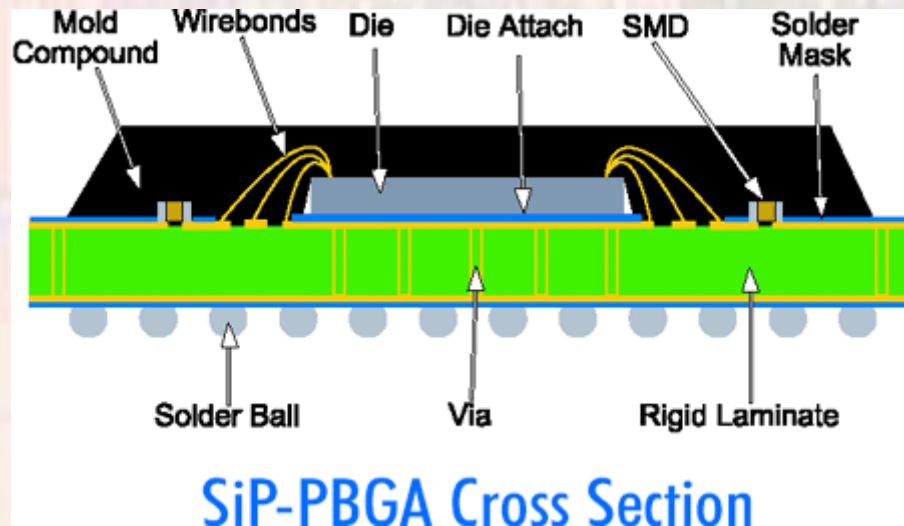
# Packaging

- Stacked Package



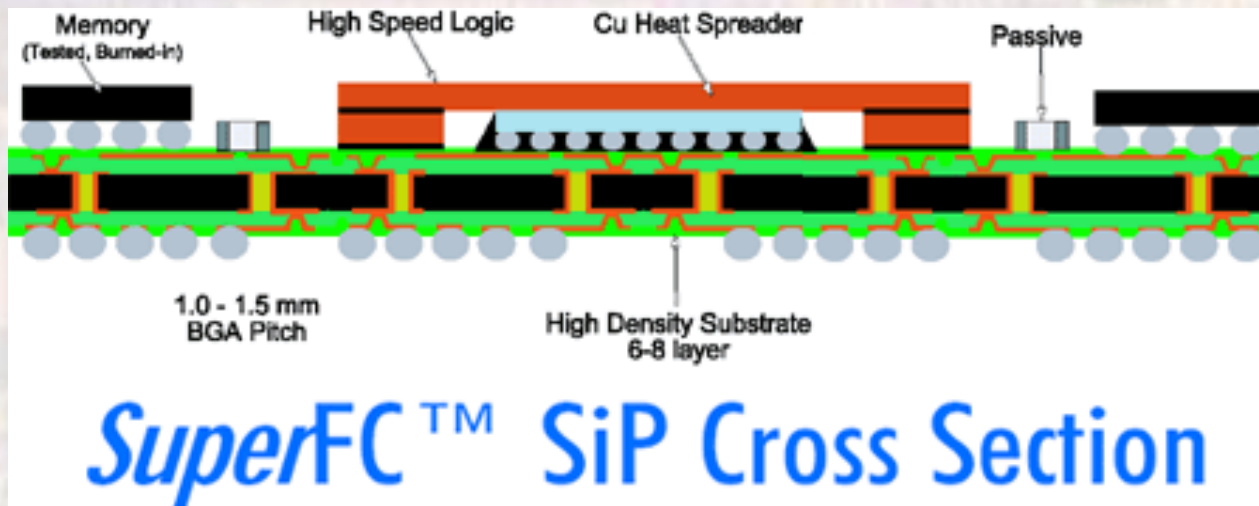
# Packaging

- SiP – System in Package



# Packaging

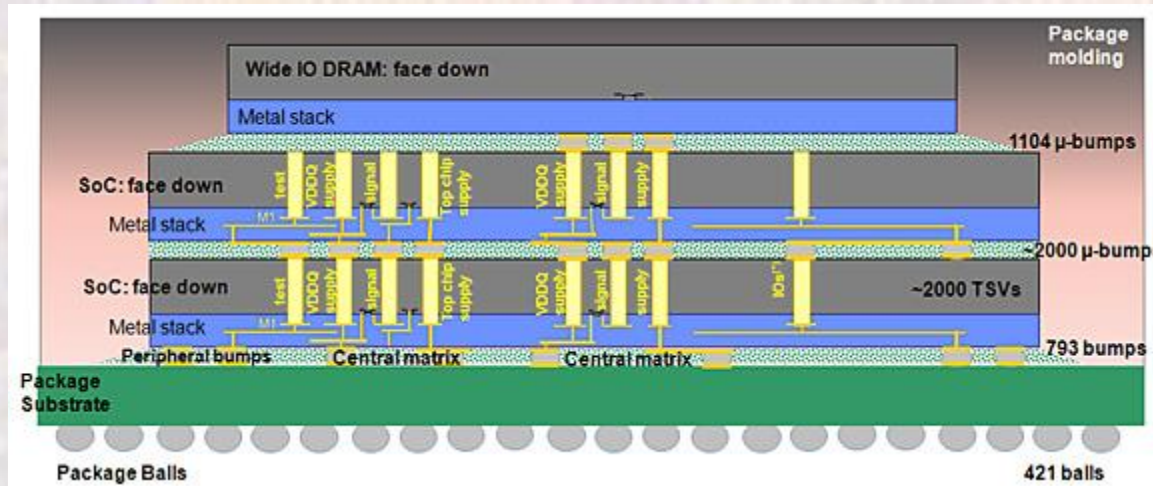
- SiP – System in Package





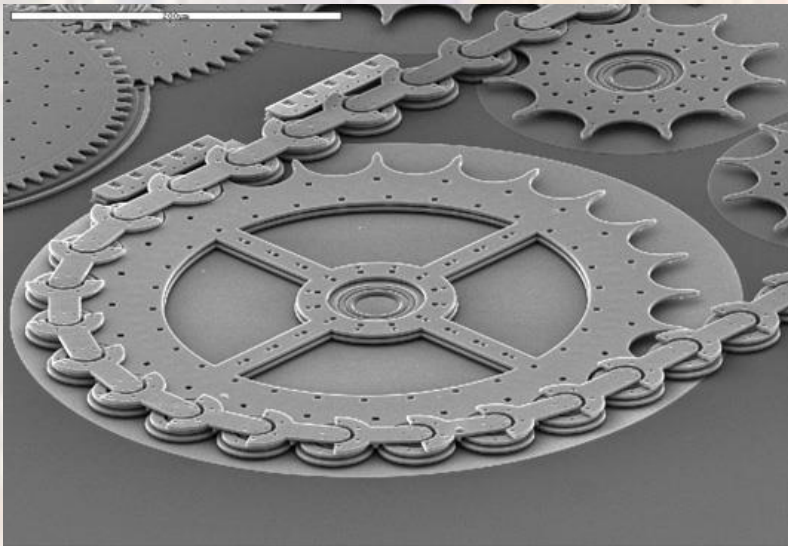
# Packaging

- Silicon Through Vias



# Packaging

- Micro-Electro-Mechanical Device



# Packaging

- SMT Carriers

