Universal Asynchronous Receiver / Transmitter Basics (UART)

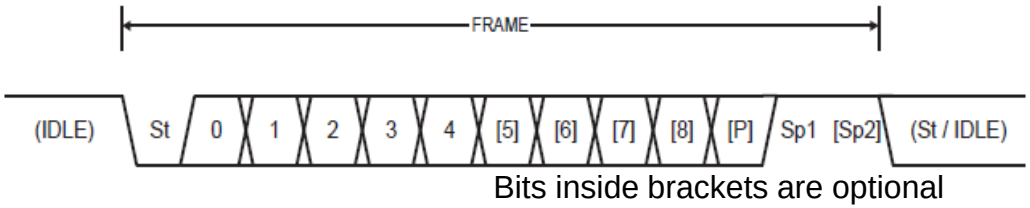
Last updated 6/30/21

UART Basics

- UART/USART
  - Serial receiver / transmitter
  - Asynchronous and Synchronous versions
  - Asynchronous
    - 2 pin interface
    - RxD – receive data pin
    - TxD – transmit data pin
    - Clock recovery system
  - Synchronous
    - 3 pin interface
    - RxD – receive data pin
    - TxD – transmit data pin
    - Xck – Clock – PD4

UART Basics

- Frame
  - 1 start bit
  - 5, 6, 7, 8, or 9 data bits – typically LSB first
  - none, even, or odd - parity bit
  - 1 or 2 stop bits,
  - Overflow, Framing, Parity – error detection

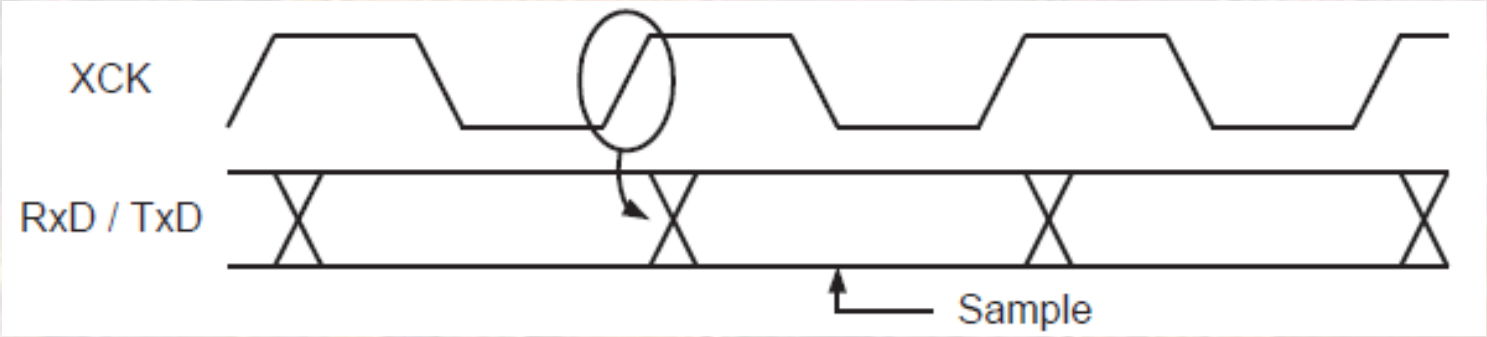


Bits inside brackets are optional

St	Start bit, always low.
(n)	Data bits (0 to 8).
P	Parity bit. Can be odd or even.
Sp	Stop bit, always high.
IDLE	No transfers on the communication line (RxDn or TxDn). An IDLE line must be high.

UART Basics

- Synchronous mode operation
  - Master creates clock signal
    - Xck max is typically $Clk_{system}/4$ for timing purposes
  - Master and Slave
    - Transmit on one clock edge
    - Receive (latch data) on the opposite clock edge

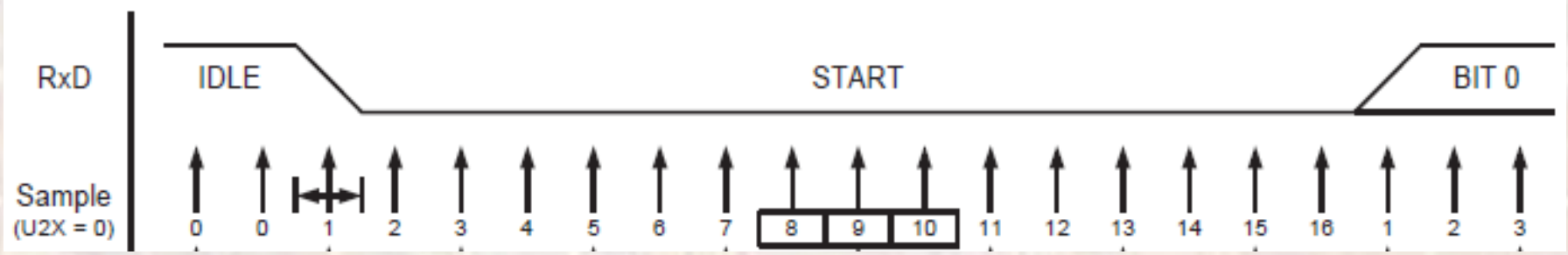


UART Basics

- Asynchronous mode operation
  - Transmit is unchanged
  - Xck is disabled
    - No Master or Slave
  - Must establish an agreed BAUD rate
    - Max BAUD rate is typically $Clk_{system}/16$
    - Limited by HW – clock selection options
    - Fixed in SW
    - Start at known BAUD rate and agree to go faster/slower
  - Receiver circuitry includes:
    - Clock recovery block
    - Data recovery block

UART Basics

- Asynchronous mode operation
  - Clock and Data recovery
    - Internal clock at 16x BAUD rate
    - Sample RxD signal with internal clock
    - Detect Start bit falling edge
    - Sample RxD after 8,9,10 internal clocks
    - Majority determines bit value
    - Assuming a valid start – all further bits sampled at multiples of 16 clocks



UART Basics

- Multi-processor mode
  - Multiple processors sharing the same USART signals
  - Use the last bit in the data (e.g. bit 9 when using 8 bit data) to indicate an address or data value is in the frame
  - If it is an address and it is your address, collect subsequent data frames
  - If it is not your address, ignore subsequent data frames

UART Basics

- Error detection
  - Parity
    - Create an error if parity is wrong
  - Overflow
    - Create an error if new data is ready to be sampled and the last data has not been read from the buffer yet
    - Double buffering is common
  - Frame error
    - Stop bit not detected when expected
    - Idle not detected when expected

UART Basics

- Common BAUD rates

BAUD Rate	Bit Width (us)	Frame Length start,8bit data, parity, 1 stop (us)	Data Rate (Bits/s)	(Bytes/s)
4800	208.33	2291.67	3,491	436
9600	104.17	1145.83	6,982	873
19200	52.08	572.92	13,964	1,745
38400	26.04	286.46	27,927	3,491
57600	17.36	190.97	41,891	5,236
115200	8.68	95.49	83,782	10,473