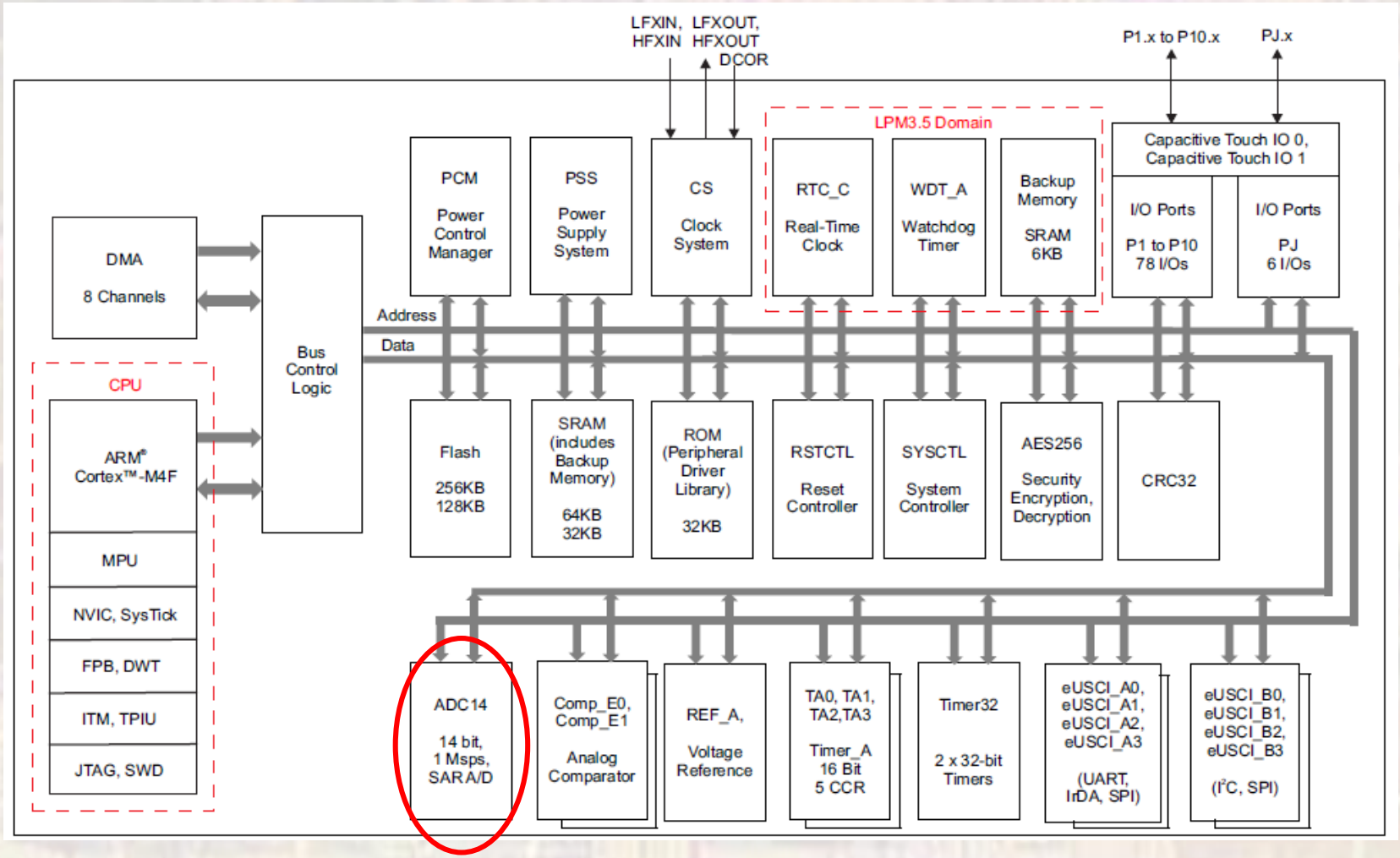
ADC 14

Last updated 10/4/19

ADC 14

- MSP432 ADC



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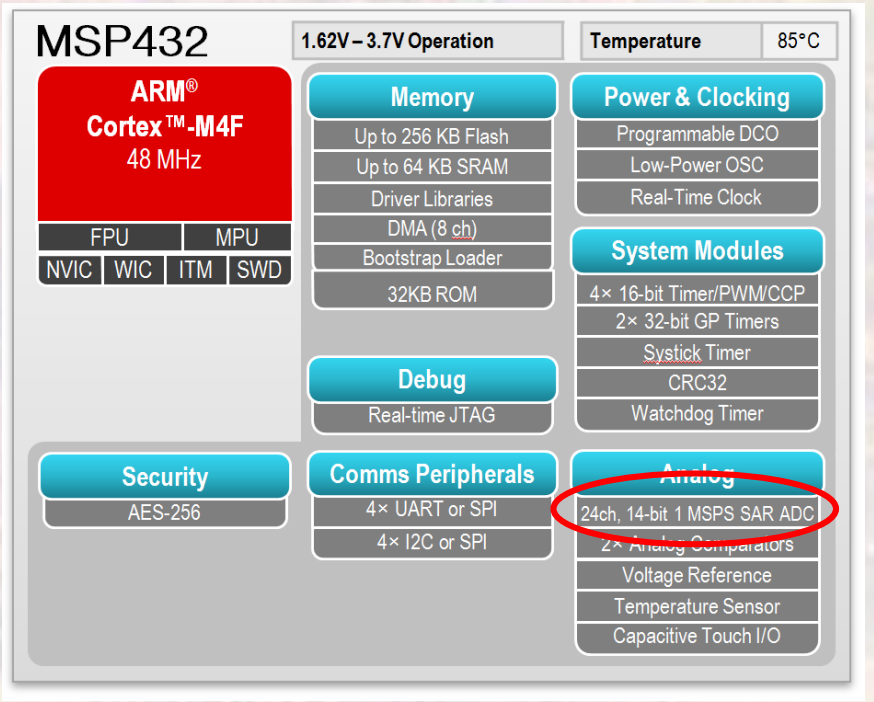
ADC 14

- MSP432 ADC
  - ARM (AMBA Compliant) ADC
  - 14 bit resolution
  - 1 MSPS conversion rate
  - Integrated S/H
  - 24 external input channels
  - 2 internal input channels
  - Single-ended and Differential conversions



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ADC 14

- MSP432 ADC

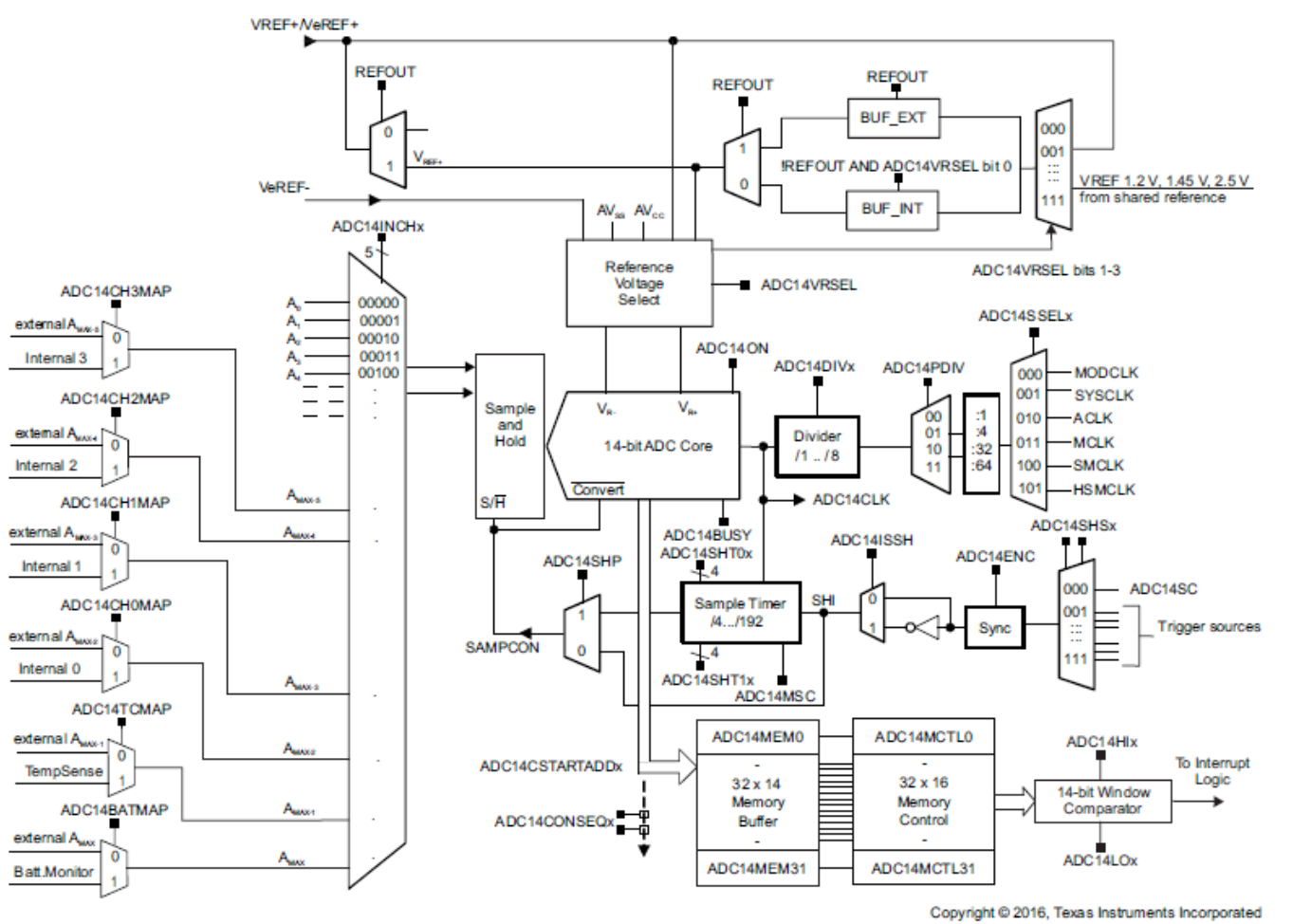

Figure 20-1. ADC14 Block Diagram

ADC 14

- MSP432 ADC

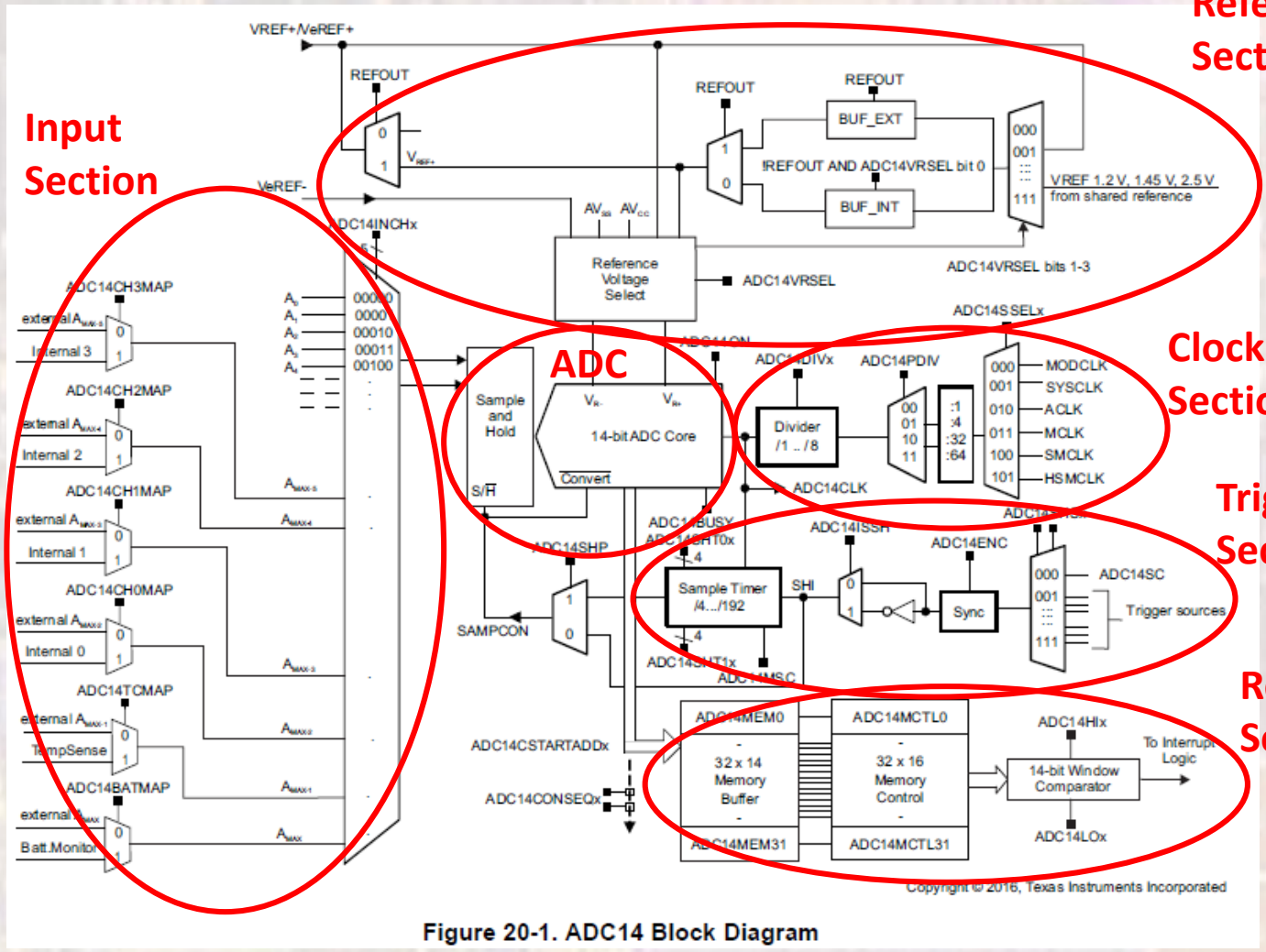

Figure 20-1. ADC14 Block Diagram

ADC 14

- MSP432 ADC
  - Core
    - 14 bit resolution
    - Digital output – 0x0000 to 0x3FFF
    - V_{R+} and V_{R-} set upper and lower limits for the conversion
    - Results – stored as binary – unsigned
      - Differential results add an offset of 8192
    - Single ended mode

$$1\ LSB = \frac{V_{R+} - V_{R-}}{16384} \qquad N_{ADC} = 16384 \times \frac{V_{in+} - V_{R-}}{V_{R+} - V_{R-}}$$

    - Differential mode

$$1\ LSB = \frac{V_{R+} - V_{R-}}{8192} \qquad N_{ADC} = \left\{8192 \times \frac{V_{in+} - V_{in-}}{V_{R+} - V_{R-}}\right\} + 8192$$

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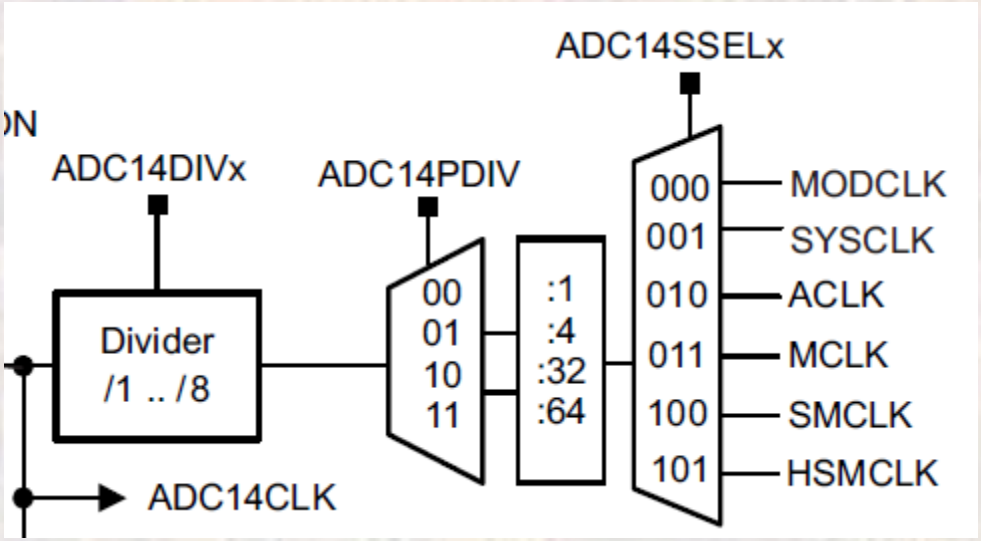
ADC 14

- MSP432 ADC
  - Clocks
    - Clock sources: MODCLK, SYSCLK, ACLK, MCLK, SMCLK, HSMCLK.
    - 2 levels of clock divider
      - ADC14PDIV – divide by 1, 4, 32, 64
      - ADC14DIV – divide by 1, 2, 3, 4, 5, 6, 7, 8



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ADC 14

- MSP432 ADC
  - Inputs
    - 24 external inputs
      - Multiplexed with I/Os – must be selected
      - Disable digital function to reduce parasitic currents
    - 2 internal inputs
      - Battery Monitor
      - Temperature Sensor
    - Isolated input pin structure

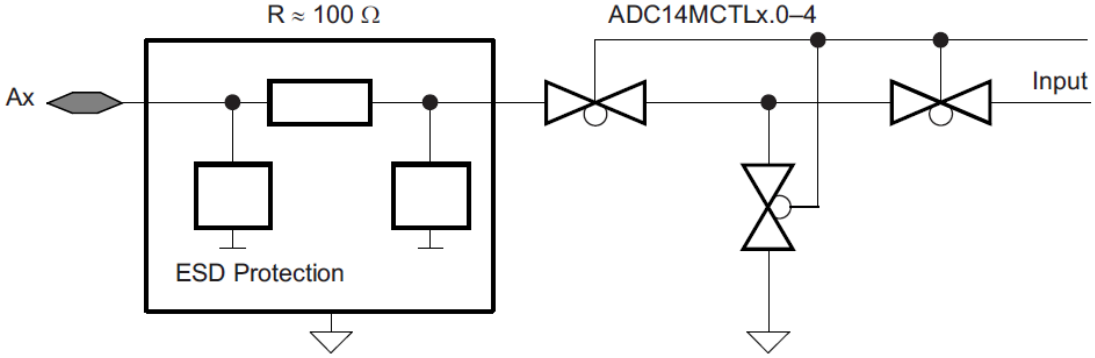

Figure 20-2. Analog Multiplexer

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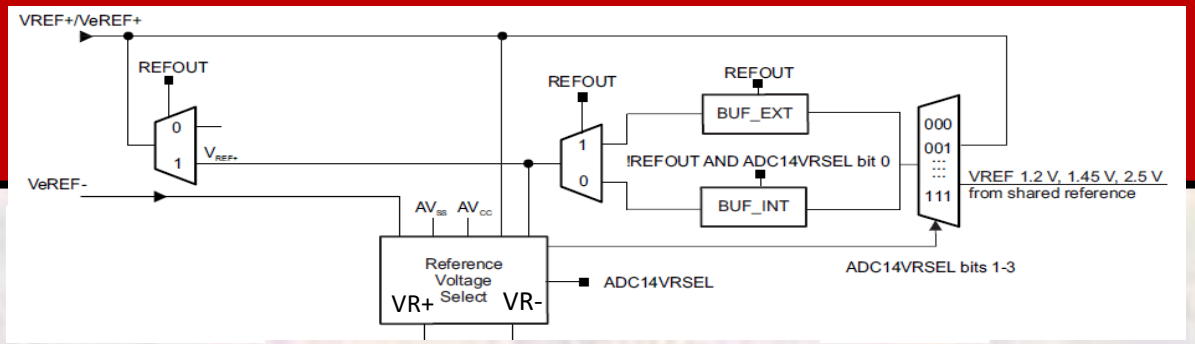
ADC 14



- MSP432 ADC
  - Voltage Reference
    - 3 internal reference levels
      - 1.2V, 1.45V, 2.5V
    - Support for external references
      - AVCC and AVSS
      - VREF+/VeREF+ and VeREF-
    - Each input channel can select a reference level
      - V(R+) = AVCC V(R-) = AVSS
      - V(R+) = VREF buffered V(R-) = AVSS
      - V(R+) = VeREF+ V(R-) = VeREF-
      - V(R+) = VeREF+ buffered V(R-) = VeREF

    - AVCC = 3.3V AVSS = 0V

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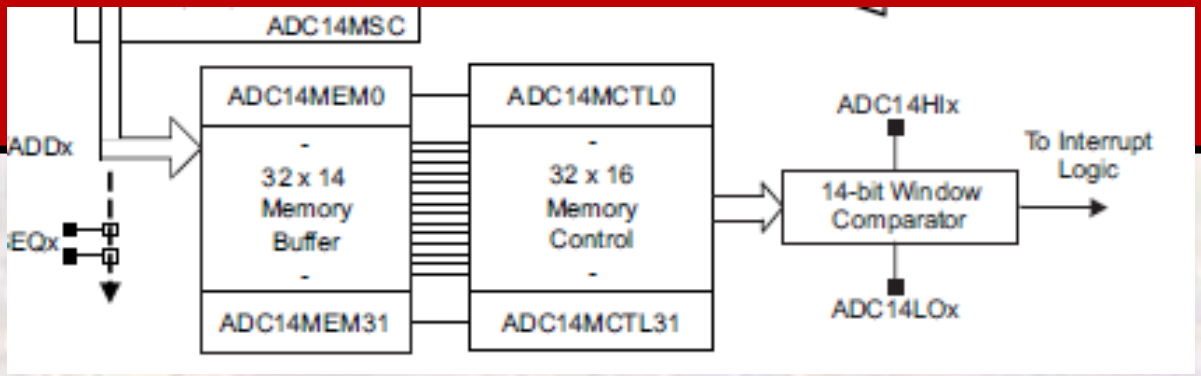
ADC 14



- MSP432 ADC
  - Memory Buffer
    - 32 – 14 bit buffer locations
    - Store the ADC conversion result
    - Each location can be assigned to any ADC input pin
    - Start address is set in control register
    - Each MEM_CTL register has an EOS (end of sequence) bit to indicate it is the last location in a sequence
    - Sequences are executed in numerical memory order

mem3 <- A4 start address set in ADC14->CTL1
mem4 <- A7
mem5 <- A0
mem6 <- A7 EOS bit set in ADC14->MCTL(6)
results in ADC14->MEM(3) through ADC14->MEM(6)

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ADC 14

- MSP432 ADC
  - Operation
    - 8 conversion start triggers
      - Software – Start Conversion Bit
      - Hardware – TA0_Cx, TA1_Cx, TA2_Cx, TA3_C1
    - 2 Sampling modes
      - Extended – sampling lasts as long as trigger is active
      - Pulse – programmable sampling time - ADC14SHT0x, ADC14SHT1x
    - Conversion starts as soon as sampling is complete
      - 14 bit conversion → 16 ADC clocks
      - 12 bit conversion → 14 ADC clocks
      - 10 bit conversion → 11 ADC clocks
      - 9 bit conversion → 10 ADC clocks
    - When complete – Flag is set

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ADC 14

- MSP432 ADC
  - Operation

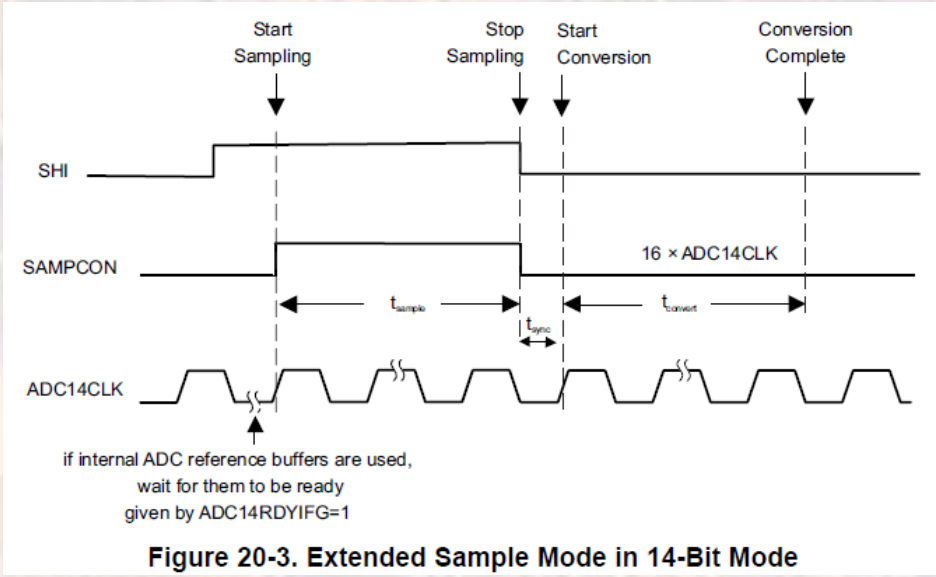

Figure 20-3. Extended Sample Mode in 14-Bit Mode

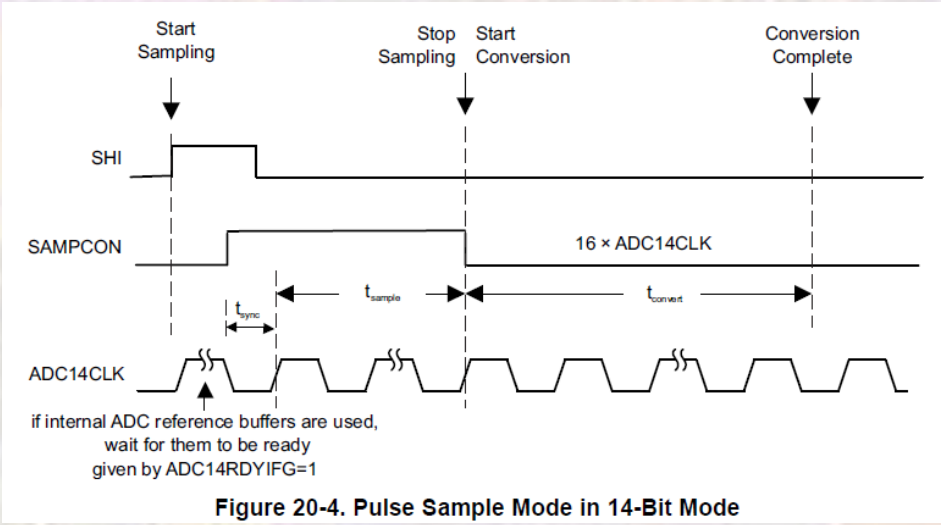

Figure 20-4. Pulse Sample Mode in 14-Bit Mode

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ADC 14

- MSP432 ADC
  - Conversion Modes
    - Single-channel single-conversion
      - A single channel is converted once
    - Sequence-of-channels (autoscan)
      - A sequence of channels is converted once
    - Repeat-single-channel
      - A single channel is converted repeatedly
    - Repeat-sequence-of-channels (repeated autoscan)
      - A sequence of channels is converted repeatedly.

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ADC 14

- MSP432 ADC
  - Conversion Modes
  - Single-channel single-conversion
    - Channel selected by CSTARTADDx
    - ADC result is written to the ADC14MEMx
    - Successive conversions can be triggered by the start conversion bit
    - Other trigger sources require the enable conversion bit to be toggled before the next conversion can occur

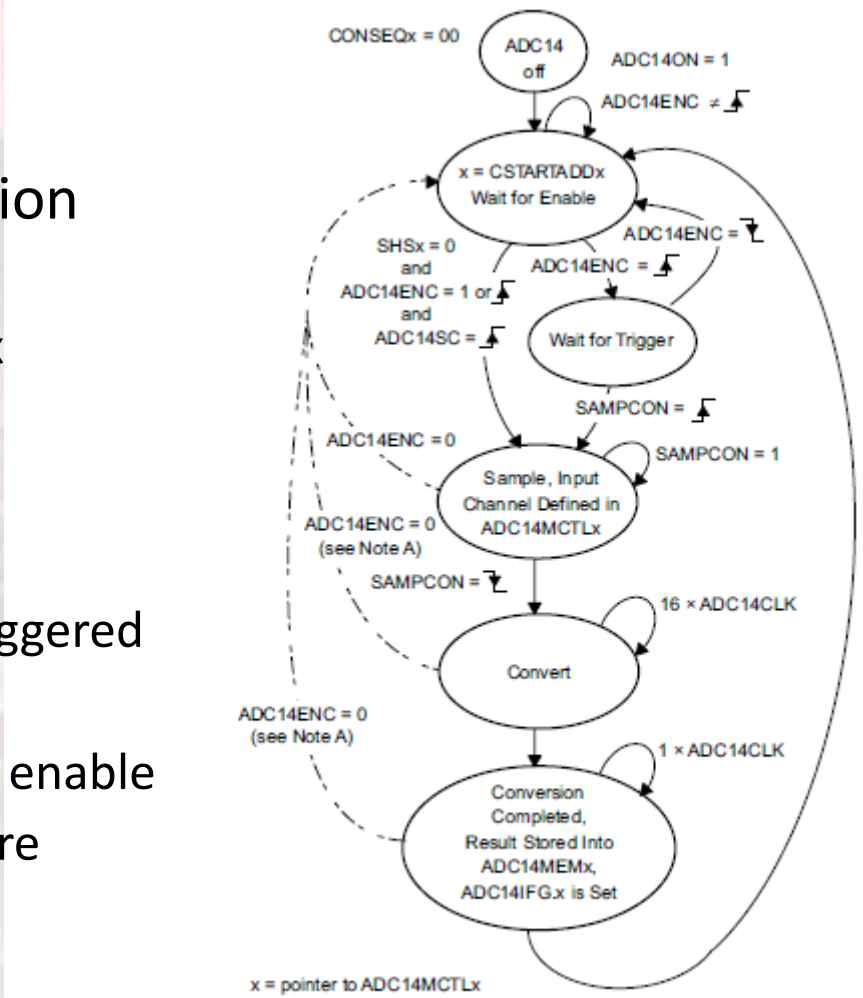

Figure 20-6. Single-Channel Single-Conversion Mode

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ADC 14

- MSP432 ADC
  - Conversion Modes
  - Sequence-of-channels (autoscan)
    - 1st Channel selected by CSTARTADDx
    - 1st ADC result is written to the ADC14MEMx
    - Last channel is the channel with its ADC14EOS bit set
    - Successive conversions can be triggered by the start conversion bit
    - Other trigger sources require the enable conversion bit to be toggled before the next conversion can occur

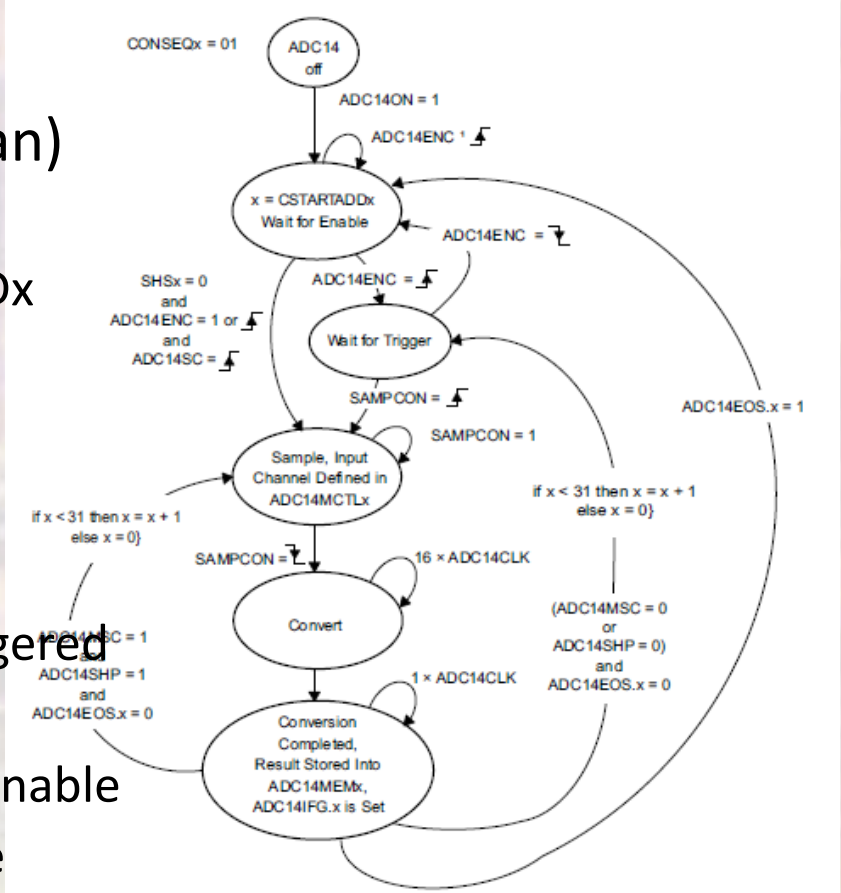

Figure 20-7. Sequence-of-Channels Mode

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ADC 14

- MSP432 ADC
  - Conversion Modes
  - Repeat-single-channel
    - Channel selected by CSTARTADDx
    - ADC result is written to the ADC14MEMx
    - Successive conversions are made automatically
    - Results are overwritten each conversion

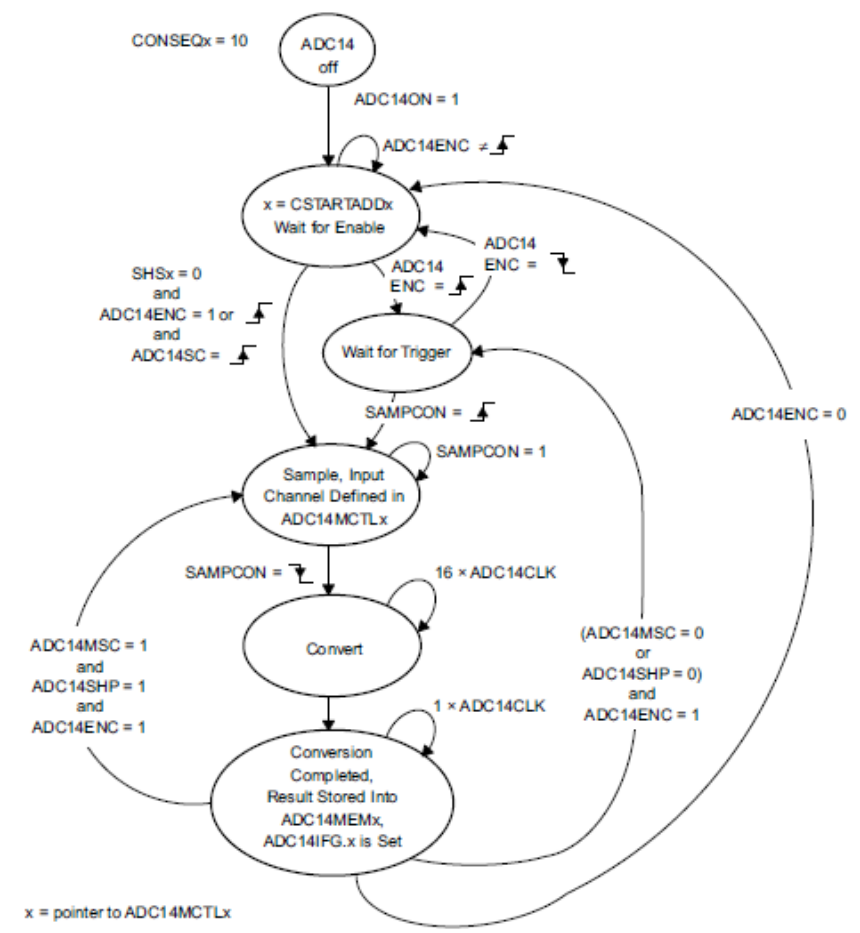

Figure 20-8. Repeat-Single-Channel Mode

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ADC 14

- MSP432 ADC
  - Conversion Modes
  - Sequence-of-channels (autoscan)
    - 1st Channel selected by CSTARTADDx
    - 1st ADC result is written to the ADC14MEMx
    - Last channel is the channel with its ADC14EOS bit set
    - Successive conversions are made automatically
    - Results are overwritten each conversion

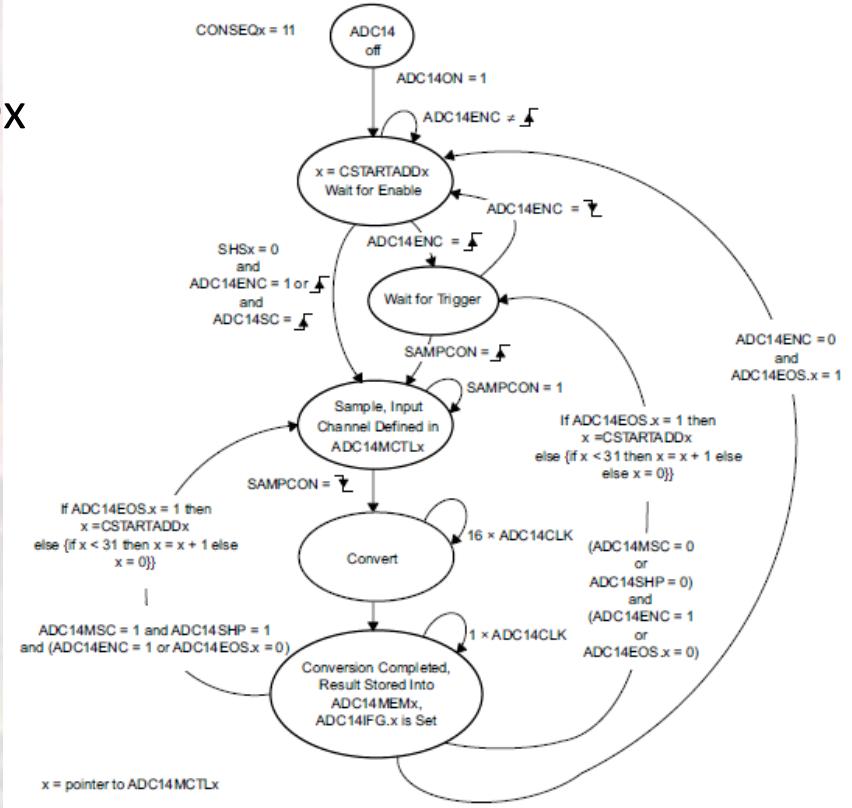

Figure 20-9. Repeat-Sequence-of-Channels Mode

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ADC 14

- MSP432 ADC
  - Window Comparator
    - Creates an interrupt based on the conversion memory value
      - less than lower threshold
      - greater than upper threshold
      - Between thresholds
    - 2 sets of threshold registers
      - ADC14LO0, ADC14HI0, ADC14LO1, ADC14HI1

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ADC 14

- MSP432 ADC Registers

ADC14->CTL0, CTL1, …
MCTL[0], MCTL[1]. …
MEM[0], MEM[1]. …

Table 20-3. ADC14 Registers

Offset	Acronym	Register Name	Type	Reset	Section
000h	ADC14CTL0	Control 0 Register	Read/write	00000000h	Section 20.3.1
004h	ADC14CTL1	Control 1 Register	Read/write	00000030h	Section 20.3.2
008h	ADC14LO0	Window Comparator Low Threshold 0 Register	Read/write	00000000h	Section 20.3.3
00Ch	ADC14HI0	Window Comparator High Threshold 0 Register	Read/write	00003FFFh	Section 20.3.4
010h	ADC14LO1	Window Comparator Low Threshold 1 Register	Read/write	00000000h	Section 20.3.5
014h	ADC14HI1	Window Comparator High Threshold 1 Register	Read/write	00003FFFh	Section 20.3.6
018h to 094h	ADC14MCTL0 to ADC14MCTL31	Memory Control 0 to Memory Control 31 Register	Read/write	00000000h	Section 20.3.7
098h to 114h	ADC14MEM0 to ADC14MEM31	Memory 0 to Memory 31 Register	Read/write	undefined	Section 20.3.8
13Ch	ADC14IER0	Interrupt Enable 0 Register	Read/write	00000000h	Section 20.3.9
140h	ADC14IER1	Interrupt Enable 1 Register	Read/write	00000000h	Section 20.3.10
144h	ADC14IFGR0	Interrupt Flag 0 Register	Read	00000000h	Section 20.3.11
148h	ADC14IFGR1	Interrupt Flag 1 Register	Read	00000000h	Section 20.3.12
14Ch	ADC14CLRIFGR0	Clear Interrupt Flag 0 Register	Write	00000000h	Section 20.3.13
150h	ADC14CLRIFGR1	Clear Interrupt Flag 1 Register	Write	00000000h	Section 20.3.14
154h	ADC14IV	Interrupt Vector Register	Read	00000000h	Section 20.3.15

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ADC 14

- MSP432 ADC Control Register 0

Figure 20-12. ADC14CTL0 Register

31	30	29	28	27	26	25	24
ADC14PDIV		ADC14SHSx			ADC14SHP	ADC14ISSH	ADC14DIVx
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
23	22	21	20	19	18	17	16
ADC14DIVx		ADC14SSELx			ADC14CONSEQx		ADC14BUSY
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r-0
15	14	13	12	11	10	9	8
ADC14SHT1x				ADC14SHT0x			
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ADC14MSC	Reserved		ADC14ON	Reserved		ADC14ENC	ADC14SC
rw-0	r-0	r-0	rw-0	r-0	r-0	rw-0	rw-0

Can be modified only when ADC14ENC = 0

Table 20-4. ADC14CTL0 Register Description

Bit	Field	Type	Reset	Description
31-30	ADC14PDIV	RW	0h	ADC14 predivider. This bit predivides the selected ADC14 clock source. Can be modified only when ADC14ENC = 0. 00b = Predivide by 1 01b = Predivide by 4 10b = Predivide by 32 11b = Predivide by 64
29-27	ADC14SHSx	RW	0h	ADC14 sample-and-hold source select. Can be modified only when ADC14ENC = 0. 000b = ADC14SC bit 001b = See device-specific data sheet for source 010b = See device-specific data sheet for source 011b = See device-specific data sheet for source 100b = See device-specific data sheet for source 101b = See device-specific data sheet for source 110b = See device-specific data sheet for source 111b = See device-specific data sheet for source

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ADC 14

- MSP432 ADC Control Register 0

Bit	Field	Type	Reset	Description
26	ADC14SHP	RW	0h	ADC14 sample-and-hold pulse-mode select. This bit selects the source of the sampling signal (SAMPCON) to be either the output of the sampling timer or the sample-input signal directly. Can be modified only when ADC14ENC = 0. 0b = SAMPCON signal is sourced from the sample-input signal. 1b = SAMPCON signal is sourced from the sampling timer.
25	ADC14ISSH	RW	0h	ADC14 invert signal sample-and-hold. Can be modified only when ADC14ENC = 0. 0b = The sample-input signal is not inverted. 1b = The sample-input signal is inverted. Setting ADC14ISSH = 1 and triggering a conversion using ADC14SC is not recommended. ADC14SC bit gets reset to 0 automatically at the end of conversion and if ADC14ISSH = 1, the 1->0 transition on ADC14SC triggers another conversion.
24-22	ADC14DIVx	RW	0h	ADC14 clock divider. Can be modified only when ADC14ENC = 0. 000b = /1 001b = /2 010b = /3 011b = /4 100b = /5 101b = /6 110b = /7 111b = /8
21-19	ADC14SSELx	RW	0h	ADC14 clock source select. Can be modified only when ADC14ENC = 0. 000b = MODCLK 001b = SYSCLK 010b = ACLK 011b = MCLK 100b = SMCLK 101b = HSMCLK 110b = Reserved 111b = Reserved
18-17	ADC14CONSEQx	RW	0h	ADC14 conversion sequence mode select Can be modified only when ADC14ENC = 0. 00b = Single-channel, single-conversion 01b = Sequence-of-channels 10b = Repeat-single-channel 11b = Repeat-sequence-of-channels
16	ADC14BUSY	R	0h	ADC14 busy. This bit indicates an active sample or conversion operation. 0b = No operation is active. 1b = A sequence, sample, or conversion is active.

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ADC 14

- MSP432 ADC Control Register 0

Bit	Field	Type	Reset	Description
15-12	ADC14SHT1x	RW	0h	ADC14 sample-and-hold time. These bits define the number of ADC14CLK cycles in the sampling period for registers ADC14MEM8 to ADC14MEM23. Can be modified only when ADC14ENC = 0. 0000b = 4 0001b = 8 0010b = 16 0011b = 32 0100b = 64 0101b = 96 0110b = 128 0111b = 192 1000b to 1111b = Reserved
11-8	ADC14SHT0x	RW	0h	ADC14 sample-and-hold time. These bits define the number of ADC14CLK cycles in the sampling period for registers ADC14MEM0 to ADC14MEM7 and ADC14MEM24 to ADC14MEM31. Can be modified only when ADC14ENC = 0. 0000b = 4 0001b = 8 0010b = 16 0011b = 32 0100b = 64 0101b = 96 0110b = 128 0111b = 192 1000b to 1111b = Reserved
7	ADC14MSC	RW	0h	ADC14 multiple sample and conversion. Valid only for sequence or repeated modes. 0b = The sampling timer requires a rising edge of the SHI signal to trigger each sample-and-convert. 1b = The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed.
6-5	Reserved	R	0h	Reserved. Always reads as 0.
4	ADC14ON	RW	0h	ADC14 on 0b = ADC14 off 1b = ADC14 on. ADC core is ready to power up when a valid conversion is triggered.
3-2	Reserved	R	0h	Reserved. Always reads as 0.
1	ADC14ENC	RW	0h	ADC14 enable conversion 0b = ADC14 disabled 1b = ADC14 enabled ADC14ENC low pulse width must be at-least 3 ADC14CLK cycles.
0	ADC14SC	RW	0h	ADC14 start conversion. Software-controlled sample-and-conversion start. ADC14SC and ADC14ENC may be set together with one instruction. ADC14SC is reset automatically. 0b = No sample-and-conversion-start 1b = Start sample-and-conversion

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ADC 14

- MSP432 ADC Control Register 1

Figure 20-13. ADC14CTL1 Register

31	30	29	28	27	26	25	24
Reserved				ADC14CH3MAP	ADC14CH2MAP	ADC14CH1MAP	ADC14CH0MAP
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0
23	22	21	20	19	18	17	16
ADC14TCMAP	ADC14BATMAP	Reserved	ADC14CSTARTADDx				
rw-0	rw-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved		ADC14RES		ADC14DF	ADC14REFBURST	ADC14PWRMD	
r-0	r-0	rw-1	rw-1	rw-0	rw-0	rw-0	rw-0

Can be modified only when ADC14ENC = 0

Table 20-5. ADC14CTL1 Register Description

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved. Always reads as 0.
27	ADC14CH3MAP	RW	0h	Controls internal channel 3 selection to ADC input channel MAX – 5 0b = ADC input channel internal 3 is not selected 1b = ADC input channel internal 3 is selected for ADC input channel MAX – 5
26	ADC14CH2MAP	RW	0h	Controls internal channel 2 selection to ADC input channel MAX – 4 0b = ADC input channel internal 2 is not selected 1b = ADC input channel internal 2 is selected for ADC input channel MAX – 4
25	ADC14CH1MAP	RW	0h	Controls internal channel 1 selection to ADC input channel MAX – 3 0b = ADC input channel internal 1 is not selected 1b = ADC input channel internal 1 is selected for ADC input channel MAX – 3
24	ADC14CH0MAP	RW	0h	Controls internal channel 0 selection to ADC input channel MAX – 2 0b = ADC input channel internal 0 is not selected 1b = ADC input channel internal 0 is selected for ADC input channel MAX – 2
23	ADC14TCMAP	RW	0h	Controls temperature sensor ADC input channel selection 0b = ADC internal temperature sensor channel is not selected for ADC 1b = ADC internal temperature sensor channel is selected for ADC input channel MAX – 1
22	ADC14BATMAP	RW	0h	Controls 1/2 AVCC ADC input channel selection 0b = ADC internal 1/2 x AVCC channel is not selected for ADC 1b = ADC internal 1/2 x AVCC channel is selected for ADC input channel MAX

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ADC 14

- MSP432 ADC Control Register 1

Bit	Field	Type	Reset	Description
23	ADC14TCMAP	RW	0h	Controls temperature sensor ADC input channel selection 0b = ADC internal temperature sensor channel is not selected for ADC 1b = ADC internal temperature sensor channel is selected for ADC input channel MAX – 1
22	ADC14BATMAP	RW	0h	Controls 1/2 AVCC ADC input channel selection 0b = ADC internal 1/2 x AVCC channel is not selected for ADC 1b = ADC internal 1/2 x AVCC channel is selected for ADC input channel MAX
21	Reserved	R	0h	Reserved. Always reads as 0.
20-16	ADC14CSTARTADDx	RW	0h	ADC14 conversion start address. These bits select which ADC14 conversion memory register is used for a single conversion or for the first conversion in a sequence. The value of CSTARTADDx is 0h to 1Fh, corresponding to ADC14MEM0 to ADC14MEM31
15-6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	ADC14RES	RW	3h	ADC14 resolution. This bit defines the conversion result resolution. Can be modified only when ADC14ENC = 0. 00b = 8 bit (9 clock cycle conversion time) 01b = 10 bit (11 clock cycle conversion time) 10b = 12 bit (14 clock cycle conversion time) 11b = 14 bit (16 clock cycle conversion time)
3	ADC14DF	RW	0h	ADC14 data read-back format. Data is always stored in the binary unsigned format. 0b = Binary unsigned. Theoretically, for ADC14DIF = 0 and 14-bit mode, the analog input voltage - V(REF) results in 0000h, and the analog input voltage + V(REF) results in 3FFFh. 1b = Signed binary (2s complement), left aligned. Theoretically, for ADC14DIF = 0 and 14-bit mode, the analog input voltage - V(REF) results in 8000h, and the analog input voltage + V(REF) results in 7FFCh.
2	ADC14REFBURST	RW	0h	ADC reference buffer burst. Can be modified only when ADC14ENC = 0. 0b = ADC reference buffer on continuously 1b = ADC reference buffer on only during sample-and-conversion
1-0	ADC14PWRMD	RW	0h	ADC power modes. Can be modified only when ADC14ENC = 0. 00b = Regular-power mode for use with any resolution setting. Sample rate can be up to 1 Msps. 01b = Reserved 10b = Low-power mode for 12-bit, 10-bit, and 8-bit resolution settings. Sample rate must not exceed 200 ksps. 11b = Reserved

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ADC 14

- MSP432 ADC Threshold Register 0

Figure 20-14. ADC14LO0 Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
ADC14LO0							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ADC14LO0							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 20-6. ADC14LO0 Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always reads as 0.
15-0	ADC14LO0	RW	0h	Low threshold 0. Can be modified only when ADC14ENC = 0. If ADC14DF = 0, unsigned binary format: The 14-bit threshold value must be right aligned. Bit 13 is the MSB. Bits 15-14 are 0 in 14-bit mode, bits 15-12 are 0 in 12-bit mode, bits 15-10 are 0 in 10-bit mode, and bits 15-8 are 0 in 8-bit mode. The reset value is: 0h If ADC14DF = 1, 2s-complement format: The 14-bit threshold value must be left aligned. Bit 15 is the MSB. Bits 1-0 are 0 in 14-bit mode, bits 3-0 are 0 in 12-bit mode, bits 5-0 are 0 in 10-bit mode, and bits 7-0 are 0 in 8-bit mode. The reset value is: 8000h

Figure 20-15. ADC14HI0 Register

30	29	28	27	26	25	24
Reserved						
r-0	r-0	r-0	r-0	r-0	r-0	r-0
22	21	20	19	18	17	16
Reserved						
r-0	r-0	r-0	r-0	r-0	r-0	r-0
14	13	12	11	10	9	8
ADC14HI0						
rw-0	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1
6	5	4	3	2	1	0
ADC14HI0						
rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1

Table 20-7. ADC14HI0 Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always reads as 0.
15-0	ADC14HI0	RW	3FFFh	High threshold 0. Can be modified only when ADC14ENC = 0. If ADC14DF = 0, unsigned binary format: The 14-bit threshold value must be right aligned. Bit 13 is the MSB. Bits 15-14 are 0 in 14-bit mode, bits 15-12 are 0 in 12-bit mode, bits 15-10 are 0 in 10-bit mode, and bits 15-8 are 0 in 8-bit mode. The reset value is: 3FFFh (14 bit), 0FFFh (12 bit), 03FFh (10 bit), or 00FFh (8 bit) If ADC14DF = 1, 2s-complement format: The 14-bit threshold value must be left aligned. Bit 15 is the MSB. Bits 1-0 are 0 in 14-bit mode, bits 3-0 are 0 in 12-bit mode, bits 5-0 are 0 in 10-bit mode, and bits 7-0 are 0 in 8-bit mode. The reset value is: 7FFCh (14 bit), 7FF0h (12 bit), 7FC0h (10 bit), or 7F00h (8 bit)

ADC 14

- MSP432 ADC Threshold Register 1

Figure 20-16. ADC14LO1 Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
ADC14LO1							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ADC14LO1							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 20-8. ADC14LO1 Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always reads as 0.
15-0	ADC14LO1	RW	0h	Low threshold 1. Can be modified only when ADC14ENC = 0. If ADC14DF = 0, unsigned binary format: The 14-bit threshold value must be right aligned. Bit 13 is the MSB. Bits 15-14 are 0 in 14-bit mode, bits 15-12 are 0 in 12-bit mode, bits 15-10 are 0 in 10-bit mode, and bits 15-8 are 0 in 8-bit mode. The reset value is: 0h If ADC14DF = 1, 2s-complement format: The 14-bit threshold value must be left aligned. Bit 15 is the MSB. Bits 1-0 are 0 in 14-bit mode, bits 3-0 are 0 in 12-bit mode, bits 5-0 are 0 in 10-bit mode, and bits 7-0 are 0 in 8-bit mode. The reset value is: 8000h

Figure 20-17. ADC14HI1 Register

29	28	27	26	25	24
Reserved					
r-0	r-0	r-0	r-0	r-0	r-0
21	20	19	18	17	16
Reserved					
r-0	r-0	r-0	r-0	r-0	r-0
13	12	11	10	9	8
ADC14HI1					
rw-1	rw-1	rw-1	rw-1	rw-1	rw-1
5	4	3	2	1	0
ADC14HI1					
rw-1	rw-1	rw-1	rw-1	rw-1	rw-1

Table 20-9. ADC14HI1 Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always reads as 0.
15-0	ADC14HI1	RW	3FFFh	High threshold 1. Can be modified only when ADC14ENC = 0. If ADC14DF = 0, unsigned binary format: The 14-bit threshold value must be right aligned. Bit 13 is the MSB. Bits 15-14 are 0 in 14-bit mode, bits 15-12 are 0 in 12-bit mode, bits 15-10 are 0 in 10-bit mode, and bits 15-8 are 0 in 8-bit mode. The reset value is: 3FFFh (14 bit), 0FFFh (12 bit), 03FFh (10 bit), or 00FFh (8 bit) If ADC14DF = 1, 2s-complement format: The 14-bit threshold value must be left aligned. Bit 15 is the MSB. Bits 1-0 are 0 in 14-bit mode, bits 3-0 are 0 in 12-bit mode, bits 5-0 are 0 in 10-bit mode, and bits 7-0 are 0 in 8-bit mode. The reset value is: 7FFCh (14 bit), 7FF0h (12 bit), 7FC0h (10 bit), or 7F00h (8 bit)

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ADC 14

- MSP432 ADC Memory Control Register 0-23

Figure 20-18. ADC14MCTL0 to ADC14MCTL31 Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
ADC14WINCTH	ADC14WINC	ADC14DIF	Reserved	ADC14VRSEL			
rw-0	rw-0	rw-0	r-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ADC14EOS	Reserved		ADC14INCHx				
rw-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0

Can be modified only when ADC14ENC = 0

Table 20-10. ADC14MCTL0 to ADC14MCTL31 Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always reads as 0.
15	ADC14WINCTH	RW	0h	Window comparator threshold register selection Can be modified only when ADC14ENC = 0. 0b = Use window comparator thresholds 0, ADC14LO0 and ADC14HI0 1b = Use window comparator thresholds 1, ADC14LO1 and ADC14HI1
14	ADC14WINC	RW	0h	Comparator window enable Can be modified only when ADC14ENC = 0. 0b = Comparator window disabled 1b = Comparator window enabled
13	ADC14DIF	RW	0h	Differential mode. Can be modified only when ADC14ENC = 0. 0b = Single-ended mode enabled 1b = Differential mode enabled
12	Reserved	R	0h	Reserved. Always reads as 0.

This register controls what gets converted

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ADC 14

- MSP432 ADC Memory Control Register 0-23

Table 20-10. ADC14MCTL0 to ADC14MCTL31 Register Description

Bit	Field	Type	Reset	Description
12	Reserved	R	0h	Reserved. Always reads as 0.
11-8	ADC14VRSEL	RW	0h	Selects combinations of V(R+) and V(R-) sources as well as the buffer selection and buffer on or off. When REFOUT = 1, VeREF+ buffered configuration is not available. Can be modified only when ADC14ENC = 0. 0000b = V(R+) = AVCC, V(R-) = AVSS 0001b = V(R+) = VREF buffered, V(R-) = AVSS 0010b to 1101b = Reserved 1110b = V(R+) = VeREF+, V(R-) = VeREF- 1111b = V(R+) = VeREF+ buffered, V(R-) = VeREF- It is recommended to connect VeREF- to on-board ground when VeREF- is selected for V(R-).
7	ADC14EOS	RW	0h	End of sequence. Indicates the last conversion in a sequence. Can be modified only when ADC14ENC = 0. 0b = Not end of sequence 1b = End of sequence
6-5	Reserved	R	0h	Reserved. Always reads as 0.
4-0	ADC14INCHx	RW	0h	Input channel select. If even channels are set as differential then odd channel configuration is ignored. Can be modified only when ADC14ENC = 0. 00000b = If ADC14DIF = 0: A0; If ADC14DIF = 1: Ain+ = A0, Ain- = A1 00001b = If ADC14DIF = 0: A1; If ADC14DIF = 1: Ain+ = A0, Ain- = A1 00010b = If ADC14DIF = 0: A2; If ADC14DIF = 1: Ain+ = A2, Ain- = A3 00011b = If ADC14DIF = 0: A3; If ADC14DIF = 1: Ain+ = A2, Ain- = A3 • • • 10100b = If ADC14DIF = 0: A20; If ADC14DIF = 1: Ain+ = A20, Ain- = A21 10101b = If ADC14DIF = 0: A21; If ADC14DIF = 1: Ain+ = A20, Ain- = A21 10110b = If ADC14DIF = 0: A22; If ADC14DIF = 1: Ain+ = A22, Ain- = A23 10111b = If ADC14DIF = 0: A23; If ADC14DIF = 1: Ain+ = A22, Ain- = A23

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ADC 14

- MSP432 ADC Memory Register 0-23

Figure 20-19. ADC14MEM0 to ADC14MEM31 Register

31	30	29	28	27	26	25	24
Reserved							
r	r	r	r	r	r	r	r
23	22	21	20	19	18	17	16
Reserved							
r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8
Conversion_Results							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Conversion_Results							
rw	rw	rw	rw	rw	rw	rw	rw

Table 20-11. ADC14MEM0 to ADC14MEM31 Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	Undefined	Reserved.
15-0	Conversion Results	RW	Undefined	If ADC14DF = 0, unsigned binary: The 14-bit conversion results are right aligned. Bit 13 is the MSB. Bits 15-14 are 0 in 14-bit mode, bits 15-12 are 0 in 12-bit mode, bits 15-10 are 0 in 10-bit mode, and bits 15-8 are 0 in 8-bit mode. If the user writes to the conversion memory registers, the results are corrupted. If ADC14DF = 1, 2s-complement format: The 14-bit conversion results are left aligned. Bit 15 is the MSB. Bits 1-0 are 0 in 14-bit mode, bits 3-0 are 0 in 12-bit mode, bits 5-0 are 0 in 10-bit mode, and bits 7-0 are 0 in 8-bit mode. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. If the user writes to the conversion memory registers, the results are corrupted. Reading this register clears the corresponding bit in ADC14IFG0.

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ADC 14

- MSP432 ADC Interrupt Enable Register 0

Figure 20-20. ADC14IER0 Register

31	30	29	28	27	26	25	24
ADC14IE31	ADC14IE30	ADC14IE29	ADC14IE28	ADC14IE27	ADC14IE26	ADC14IE25	ADC14IE24
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
23	22	21	20	19	18	17	16
ADC14IE23	ADC14IE22	ADC14IE21	ADC14IE20	ADC14IE19	ADC14IE18	ADC14IE17	ADC14IE16
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
15	14	13	12	11	10	9	8
ADC14IE15	ADC14IE14	ADC14IE13	ADC14IE12	ADC14IE11	ADC14IE10	ADC14IE9	ADC14IE8
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ADC14IE7	ADC14IE6	ADC14IE5	ADC14IE4	ADC14IE3	ADC14IE2	ADC14IE1	ADC14IE0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 20-12. ADC14IER0 Register Description (continued)

Bit	Field	Type	Reset	Description
23	ADC14IE23	RW	0h	Interrupt enable. Enables or disables the interrupt request for the ADC14IFG23 bit. 0b = Interrupt disabled 1b = Interrupt enabled
...				
0	ADC14IE0	RW	0h	Interrupt enable. Enables or disables the interrupt request for the ADC14IFG0 bit. 0b = Interrupt disabled 1b = Interrupt enabled

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ADC 14

- MSP432 ADC Interrupt Enable Register 1

Figure 20-21. ADC14IER1 Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved	ADC14RDYIE	ADC14TOVIE	ADC14OVIE	ADC14HIIE	ADC14LOIE	ADC14INIE	Reserved
r-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r-0

Table 20-13. ADC14IER1 Register Description

Bit	Field	Type	Reset	Description
31-7	Reserved	R	0h	Reserved. Always reads as 0.
6	ADC14RDYIE	RW	0h	ADC14 local buffered reference ready interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
5	ADC14TOVIE	RW	0h	ADC14 conversion-time-overflow interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
4	ADC14OVIE	RW	0h	ADC14MEMx overflow-interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
3	ADC14HIIE	RW	0h	Interrupt enable for the exceeding the upper limit interrupt of the window comparator for ADC14MEMx result register. 0b = Interrupt disabled 1b = Interrupt enabled
2	ADC14LOIE	RW	0h	Interrupt enable for the falling short of the lower limit interrupt of the window comparator for the ADC14MEMx result register. 0b = Interrupt disabled 1b = Interrupt enabled
1	ADC14INIE	RW	0h	Interrupt enable for the ADC14MEMx result register being greater than the ADC14LO threshold and below the ADC14HI threshold. 0b = Interrupt disabled 1b = Interrupt enabled
0	Reserved	R	0h	Reserved. Always reads as 0.

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ADC 14

- MSP432 ADC Interrupt Flag Register 0

Figure 20-22. ADC14IFGR0 Register

31	30	29	28	27	26	25	24
ADC14IFG31	ADC14IFG30	ADC14IFG29	ADC14IFG28	ADC14IFG27	ADC14IFG26	ADC14IFG25	ADC14IFG24
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
ADC14IFG23	ADC14IFG22	ADC14IFG21	ADC14IFG20	ADC14IFG19	ADC14IFG18	ADC14IFG17	ADC14IFG16
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
ADC14IFG15	ADC14IFG14	ADC14IFG13	ADC14IFG12	ADC14IFG11	ADC14IFG10	ADC14IFG9	ADC14IFG8
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
ADC14IFG7	ADC14IFG6	ADC14IFG5	ADC14IFG4	ADC14IFG3	ADC14IFG2	ADC14IFG1	ADC14IFG0
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

Table 20-14. ADC14IFGR0 Register Description (continued)

Bit	Field	Type	Reset	Description
24	ADC14IFG24	R	0h	ADC14MEM24 interrupt flag. This bit is set to 1 when ADC14MEM24 is loaded with a conversion result. This bit is reset to 0 when the ADC14MEM24 register is read, or when the corresponding bit in the ADC14CLRIFGR0 register is set to 1. 0b = No interrupt pending 1b = Interrupt pending
...				
0	ADC14IFG0	R	0h	ADC14MEM0 interrupt flag. This bit is set to 1 when ADC14MEM0 is loaded with a conversion result. This bit is reset to 0 when the ADC14MEM0 register is read, or when the corresponding bit in the ADC14CLRIFGR0 register is set to 1. 0b = No interrupt pending 1b = Interrupt pending

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ADC 14

- MSP432 ADC Interrupt Flag Register 1

Figure 20-23. ADC14IFGR1 Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved	ADC14RDYIFG	ADC14TOVIFG	ADC14OVIFG	ADC14HIIFG	ADC14LOIFG	ADC14INIFG	Reserved
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

Table 20-15. ADC14IFGR1 Register Description

Bit	Field	Type	Reset	Description
31-7	Reserved	R	0h	Reserved. Always reads as 0.
6	ADC14RDYIFG	R	0h	ADC14 local buffered reference ready interrupt flag. This bit is reset to 0 by IV register read or when corresponding bit in ADC14CLRIFGR1 is set to 1. 0b = No interrupt pending 1b = Interrupt pending
5	ADC14TOVIFG	R	0h	ADC14 conversion time overflow interrupt flag. This bit is reset to 0 by IV register read or when corresponding bit in ADC14CLRIFGR1 is set to 1. 0b = No interrupt pending 1b = Interrupt pending
4	ADC14OVIFG	R	0h	ADC14MEMx overflow interrupt flag. This bit is reset to 0 by IV register read or when corresponding bit in ADC14CLRIFGR1 is set to 1. 0b = No interrupt pending 1b = Interrupt pending
3	ADC14HIIFG	R	0h	Interrupt flag for exceeding the upper limit interrupt of the window comparator for ADC14MEMx result register. This bit is reset to 0 by IV register read or when corresponding bit in ADC14CLRIFGR1 is set to 1. 0b = No interrupt pending 1b = Interrupt pending
2	ADC14LOIFG	R	0h	Interrupt flag for falling short of the lower limit interrupt of the window comparator for the ADC14MEMx result register. This bit is reset to 0 by IV register read or when corresponding bit in ADC14CLRIFGR1 is set to 1. 0b = No interrupt pending 1b = Interrupt pending
1	ADC14INIFG	R	0h	Interrupt flag for the ADC14MEMx result register being greater than the ADC14LO threshold and below the ADC14HI threshold interrupt. This bit is reset to 0 by IV register read or when corresponding bit in ADC14CLRIFGR1 is set to 1. 0b = No interrupt pending 1b = Interrupt pending
0	Reserved	R	0h	Reserved. Always reads as 0.

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ADC 14

- MSP432 ADC Clear Flag Register 0

Figure 20-24. ADC14CLRIFGR0 Register

31	30	29	28	27	26	25	24
CLRADC14IFG 31	CLRADC14IFG 30	CLRADC14IFG 29	CLRADC14IFG 28	CLRADC14IFG 27	CLRADC14IFG 26	CLRADC14IFG 25	CLRADC14IFG 24
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0
23	22	21	20	19	18	17	16
CLRADC14IFG 23	CLRADC14IFG 22	CLRADC14IFG 21	CLRADC14IFG 20	CLRADC14IFG 19	CLRADC14IFG 18	CLRADC14IFG 17	CLRADC14IFG 16
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0
15	14	13	12	11	10	9	8
CLRADC14IFG 15	CLRADC14IFG 14	CLRADC14IFG 13	CLRADC14IFG 12	CLRADC14IFG 11	CLRADC14IFG 10	CLRADC14IFG 9	CLRADC14IFG 8
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
CLRADC14IFG 7	CLRADC14IFG 6	CLRADC14IFG 5	CLRADC14IFG 4	CLRADC14IFG 3	CLRADC14IFG 2	CLRADC14IFG 1	CLRADC14IFG 0
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

Bit	Field	Type	Reset	Description
23	CLRADC14IFG23	W	0h	clear ADC14IFG23 0b = no effect 1b = clear pending interrupt flag
...				
0	CLRADC14IFG0	W	0h	clear ADC14IFG0 0b = no effect 1b = clear pending interrupt flag

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ADC 14

- MSP432 ADC Clear Flag Register 1

Figure 20-25. ADC14CLRIFGR1 Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved	CLRADC14RDYIFG	CLRADC14TOVIFG	CLRADC14OVIFG	CLRADC14HIIFG	CLRADC14LOIFG	CLRADC14INIFG	Reserved
r-0	w-0	w-0	w-0	w-0	w-0	w-0	r-0

Table 20-17. ADC14CLRIFGR1 Register Description

Bit	Field	Type	Reset	Description
31-7	Reserved	R	0h	Reserved. Always reads as 0.
6	CLRADC14RDYIFG	W	0h	clear ADC14RDYIFG 0b = no effect 1b = clear pending interrupt flag
5	CLRADC14TOVIFG	W	0h	clear ADC14TOVIFG 0b = no effect 1b = clear pending interrupt flag
4	CLRADC14OVIFG	W	0h	clear ADC14OVIFG 0b = no effect 1b = clear pending interrupt flag
3	CLRADC14HIIFG	W	0h	clear ADC14HIIFG 0b = no effect 1b = clear pending interrupt flag
2	CLRADC14LOIFG	W	0h	clear ADC14LOIFG 0b = no effect 1b = clear pending interrupt flag
1	CLRADC14INIFG	W	0h	clear ADC14INIFG 0b = no effect 1b = clear pending interrupt flag
0	Reserved	R	0h	Reserved. Always reads as 0.

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ADC 14

- MSP432 ADC Interrupt Vector Register

Figure 20-26. ADC14IV Register

31	30	29	28	27	26	25	24
ADC14IVx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
23	22	21	20	19	18	17	16
ADC14IVx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
15	14	13	12	11	10	9	8
ADC14IVx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ADC14IVx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 20-18. ADC14IV Register Description

Bit	Field	Type	Reset	Description
31-0	ADC14IVx	RW	0h	ADC14 interrupt vector value. This register value is an encoded value of the highest pending interrupt in ADC14. Writing to this register clears all pending interrupt flags. 00h = No interrupt pending 02h = Interrupt Source: ADC14MEMx overflow; Interrupt Flag: ADC14OVIFG; Interrupt Priority: Highest 04h = Interrupt Source: Conversion time overflow; Interrupt Flag: ADC14TOVIFG 06h = Interrupt Source: ADC14 window high interrupt flag; Interrupt Flag: ADC14HIIFG 08h = Interrupt Source: ADC14 window low interrupt flag; Interrupt Flag: ADC14LOIFG 0Ah = Interrupt Source: ADC14 in-window interrupt flag; Interrupt Flag: ADC14INIFG 0Ch = Interrupt Source: ADC14MEM0 interrupt flag; Interrupt Flag: ADC14IFG0 0Eh = Interrupt Source: ADC14MEM1 interrupt flag; Interrupt Flag: ADC14IFG1 10h = Interrupt Source: ADC14MEM2 interrupt flag; Interrupt Flag: ADC14IFG2
				• • •
				36h = Interrupt Source: ADC14MEM21 interrupt flag; Interrupt Flag: ADC14IFG21 38h = Interrupt Source: ADC14MEM22 interrupt flag; Interrupt Flag: ADC14IFG22 3Ah = Interrupt Source: ADC14MEM23 interrupt flag; Interrupt Flag: ADC14IFG23

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ADC 14

- MSP432 ADC Info Sheet

ADC14 Info Sheet

x= 0:31

ADC14	->	CTL0	Control reg 0
		CTL1	Control reg 1
		LO0	Threshold Low - low
		HI0	Threshold Low - high
		LO1	Threshold High - low
		HI1	Threshold High - high
		MCTL[x]	Memory Control Registers
		MEM[x]	Memory registers
		IER0	Interrupt Enable reg 0
		IER1	Interrupt Enable reg 1
		IFGR0	Flag reg 0
		IFGR1	Flag reg 1
		CLRIFGR0	Clear Flag reg 0
		CLRIFGR1	Clear Flag reg 1
		IV	Interrupt Vector

ADC14_IRQHandler	INTISR[24]	ADC14	IFG[0-31], LO/IN/HI-IFG, RDYIFG, OVIFG, TOVIFG

PORT		DIR	PSEL[1:0]	PORT		DIR	PSEL[1:0]
P5.5	A 0		11	P4.1	A 12		11
P5.4	A 1		11	P4.0	A 13		11
P5.3	A 2		11	P6.1	A 14		11
P5.2	A 3		11	P6.0	A 15		11
P5.1	A 4		11	P9.1	A 16		11
P5.0	A 5		11	P9.0	A 17		11
P4.7	A 6		11	P8.7	A 18		11
P4.6	A 7		11	P8.6	A 19		11
P4.5	A 8		11	P8.5	A 20		11
P4.4	A 9		11	P8.4	A 21		11
P4.3	A 10		11	P8.3	A 22		11
P4.2	A 11		11	P8.2	A 23		11

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ADC 14

- Reading analog signals

1) Must use an Analog pin
   pins marked A0 – A15 in blue on the pinmap

2) Configure the pin to ADC mode
   PxSEL0 and PxSEL1 set to 1

3) Configure the A/D to run a conversion
   adc_setup()

4) Run the conversion
   adc_convert()

5) Read the results

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ADC 14

- Reading analog signals – single conversion
  - adc_setup()
    - Sets up ADC pin 0 (A0) to read from an analog input and perform a 12 bit conversion

```
void adc_setup(void){
    // using - A0 = P5.5
    //
    // keep enable low while making changes
    //
    // ctrl0
    // /4   sc_bit  timer  no_inv  /1   mod  singl   x  xxxx  16x   x  xx  on  xx  enb  scb
    // 01    000      1      0    000   000   00     0  0000  0010  0  00  1   00   0    0
    ADC14->CTL0 = 0x44000210;
    // ctrl1
    // xxxx   no_sel   x  mem0   xxxxxxxxxx  12b  unsigned  on  reg
    // 0000  00000000  0  00000  0000000000  10      0      0   00
    ADC14->CTL1 = 0x00000020;
    // mctl[0] - since using mem0
    // xxxx xxxx xxxx xxxx  x  enb  diffb  x  AVCC  x  xx  A0
    // 0000 0000 0000 0000  0   0     0    0  0000  0  00  00000
    ADC14->MCTL[0] = 0x00000000;
    // all others default
    // set enable
    ADC14->CTL0 |= 0x00000002;

    return;
}
```


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ADC 14

- Reading analog signals
  - adc_convert()
    - Samples the signal, does the conversion and returns a number (int) between 0 and 4095 (12 bits of resolution)

```
int adc_convert(void){
    // Start sampling/conversion
    ADC14->CTL0 |= 0x00000001;       //  start conversion

    // Wait for conversion to complete and grab value
    // Conversion is complete when ADC0 flag is set
    while (!ADC14->IFGR0){
        ;
    }

    // returning a full int instead of a uint16_t for simplicity
    return ADC14->MEM[0];
}
```


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ADC 14

- Reading a

```
/*
 * adc_example.c
 *
 *  Created on: Jul 30, 2018
 *      Author: johnsontimoj
 */
//////////////////////////////////
//
// use adc in non-interrupt mode
//
// input ADC input 0
//
// output - LCD
//
//////////////////////////////////

// includes
#include "msp.h"
#include <stdio.h>
#include "msoe_lib_all.h"

// prototypes
void pin_setup(void);
void lcd_setup(void);
void adc_setup(void);
int adc_convert(void);

int main(void){
    // setup routines
    pin_setup();
    lcd_setup();
    adc_setup();

    int val;
    while(1){
       val = adc_convert();
       LCD_goto_xy(0,0);
       LCD_print_udec10(val);
       __delay_cycles(1500000);
    } // end while

   return 0;
}
```

```
void pin_setup(void){
    // input pin - A0
    //
    P5->SEL0 |= 0x20;       // '11' pin functionality
    P5->SEL1 |= 0x20;

    return;
}

void adc_setup(void){
    // using - A0 = P5.5
    //
    // keep enable low while making changes
    //
    // ctrl0
    // /4   sc_bit  timer  no_inv  /1   mod  singl   x  xxxx  16x   x  xx  on  xx  enb  scb
    // 01    000      1      0    000   000   00     0  0000  0010  0  00  1   00   0    0
    ADC14->CTL0 = 0x44000210;
    // ctrl1
    // xxxx   no_sel   x  mem0   xxxxxxxxxx  12b  unsigned  on  reg
    // 0000  00000000  0  00000  0000000000  10      0      0   00
    ADC14->CTL1 = 0x00000020;
    // mctl[0] - since using mem0
    // xxxx xxxx xxxx xxxx  x  enb  diffb  x  AVCC  x  xx  A0
    // 0000 0000 0000 0000  0   0     0    0  0000  0  00  00000
    ADC14->MCTL[0] = 0x00000000;
    // all others default
    // set enable
    ADC14->CTL0 |= 0x00000002;

    return;
}

int adc_convert(void){
    // Start sampling/conversion
    ADC14->CTL0 |= 0x00000001;       //  start conversion

    // Wait for conversion to complete and grab value
    // Conversion is complete when ADC0 flag is set
    while (!ADC14->IFGR0){
        ;
    }

    // returning a full int instead of a uint16_t for simplicity
    return ADC14->MEM[0];
}
```

```
void lcd_setup(void){
    // setup LCD
    LCD_Config();
    LCD_clear();
    LCD_contrast(9);

    return;
}
```

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ADC 14

- Reading analog signals – interrupts, continuous
  - Sets up ADC pin 5.2 (A3)
  - Perform 12 bit conversion
  - Use mem location 5 for storage

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ADC 14

- Reading analog signals – interrupts, continuous
  - adc_setup()

```
void adc_setup(void){
    // using - A3 = P5.2
    //
    // keep enable low while making changes
    //
    // ctrl0
    // /4   sc_bit  timer  no_inv  /1   mod  rptS    x  xxxx  16x   cont  xx  on  xx  enb  scb
    // 01    000      1      0    000   000   10     0  0000  0010    1   00  1   00   0    0
    ADC14->CTL0 = 0x44040290;
    // ctrl1
    // xxxx   no_sel   x  mem5    xxxxxxxxxx  12b  unsigned  on  reg
    // 0000   000000   0  00101   0000000000  10      0      0   00
    ADC14->CTL1 = 0x00050020;
    // mctl[5] - since using mem5
    // xxxx xxxx xxxx xxxx  x  enb  diffb  x  AVCC  x  xx  A3
    // 0000 0000 0000 0000  0   0     0    0  0000  0  00  00011
    ADC14->MCTL[5] = 0x00000003;
    // ier0 - enable interrupts on channel 5
    // 0000 0000 0000 0000 0000 0000 0010 0000
    ADC14->IER0 |= 0x00000020;
    // all others default
    // set enable
    ADC14->CTL0 |= 0x00000002;

    return;
}
```


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ADC 14

- Reading analog signals
  - Interrupt service routine and setup

```
void ADC14_IRQHandler(void){
    int val;    // tmp variable - really not necessary
    val = ADC14->MEM[5];
    ADC14->CLRIFGR0 |= 0x00000020; // clr flg
    // need to put print in ISR otherwise it never
    // gets a chance to run
    LCD_goto_xy(0,0);
    LCD_print_udec10(val);

    return;
}

void NVIC_setup(void){
    // setup NVIC
    // Enable ADC
    // Note: ADC is INTISR(24)
    NVIC->IP[24] |= 0x20; // Set a priority
    NVIC->ISER[0] |= 0x01000000; // ISER0 starts at 0

    return;
}
```


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ADC 14

```
/*
 * adc_int_example.c
 *
 *  Created on: Jul 30, 2018
 *      Author: johnsontimoj
 */
//////////////////////////////////
//
// use adc in interrupt mode
//
// input ADC input 3, in mem location 5
//
// output - LCD
//
//////////////////////////////////

// includes
#include "msp.h"
#include <stdio.h>
#include "msoe_lib_all.h"

// prototypes
void pin_setup(void);
void lcd_setup(void);
void adc_setup(void);
void NVIC_setup(void);

int main(void){
    // setup routines
    pin_setup();
    lcd_setup();
    adc_setup();
    NVIC_setup();

    _enable_interrupts();

    // Start sampling/conversion
    ADC14->CTL0 |= 0x00000001;        //
start conversion

    // hang out
    while(1){
       __delay_cycles(1500000);
    } // end while

   return 0;
}
```

```
void pin_setup(void){
    // input pin - A3, p5.2
    //
    P5->SEL0 |= 0x04;       // '11' pin functionality
    P5->SEL1 |= 0x04;

    return;
}

void adc_setup(void){
    // using - A3 = P5.2
    //
    // keep enable low while making changes
    //
    // ctrl0
    // /4   sc_bit  timer  no_inv  /1   mod  rptS    x  xxxx  16x   cont  xx  on  xx  enb  scb
    // 01    000      1      0    000   000   10     0  0000  0010    1   00  1   00   0    0
    ADC14->CTL0 = 0x44040290;
    // ctrl1
    // xxxx   no_sel   x  mem5    xxxxxxxxxx  12b  unsigned  on  reg
    // 0000   000000   0  00101   0000000000  10      0      0   00
    ADC14->CTL1 = 0x00050020;
    // mctl[5] - since using mem5
    // xxxx xxxx xxxx xxxx  x  enb  diffb  x  AVCC  x  xx  A3
    // 0000 0000 0000 0000  0   0     0    0  0000  0  00  00011
    ADC14->MCTL[5] = 0x00000003;
    // ier0 - enable interrupts on channel 5
    // 0000 0000 0000 0000 0000 0000 0010 0000
    ADC14->IER0 |= 0x00000020;
    // all others default
    // set enable
    ADC14->CTL0 |= 0x00000002;

    return;
}

void lcd_setup(void){
    // setup LCD
    LCD_Config();
    LCD_clear();
    LCD_contrast(9);

    return;
}
```

```
void ADC14_IRQHandler(void){
    int val;    // tmp variable - really not necessary
    val = ADC14->MEM[5];
    ADC14->CLRIFGR0 |= 0x00000020; // clr flg
    // need to put print in ISR otherwise it never
    // gets a chance to run
    LCD_goto_xy(0,0);
    LCD_print_udec10(val);

    return;
}

void NVIC_setup(void){
    // setup NVIC
    // Enable ADC
    // Note: ADC is INTISR(24)
    NVIC->IP[24] |= 0x20; // Set a priority
    NVIC->ISER[0] |= 0x01000000; // ISER0 starts at 0

    return;
}
```


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