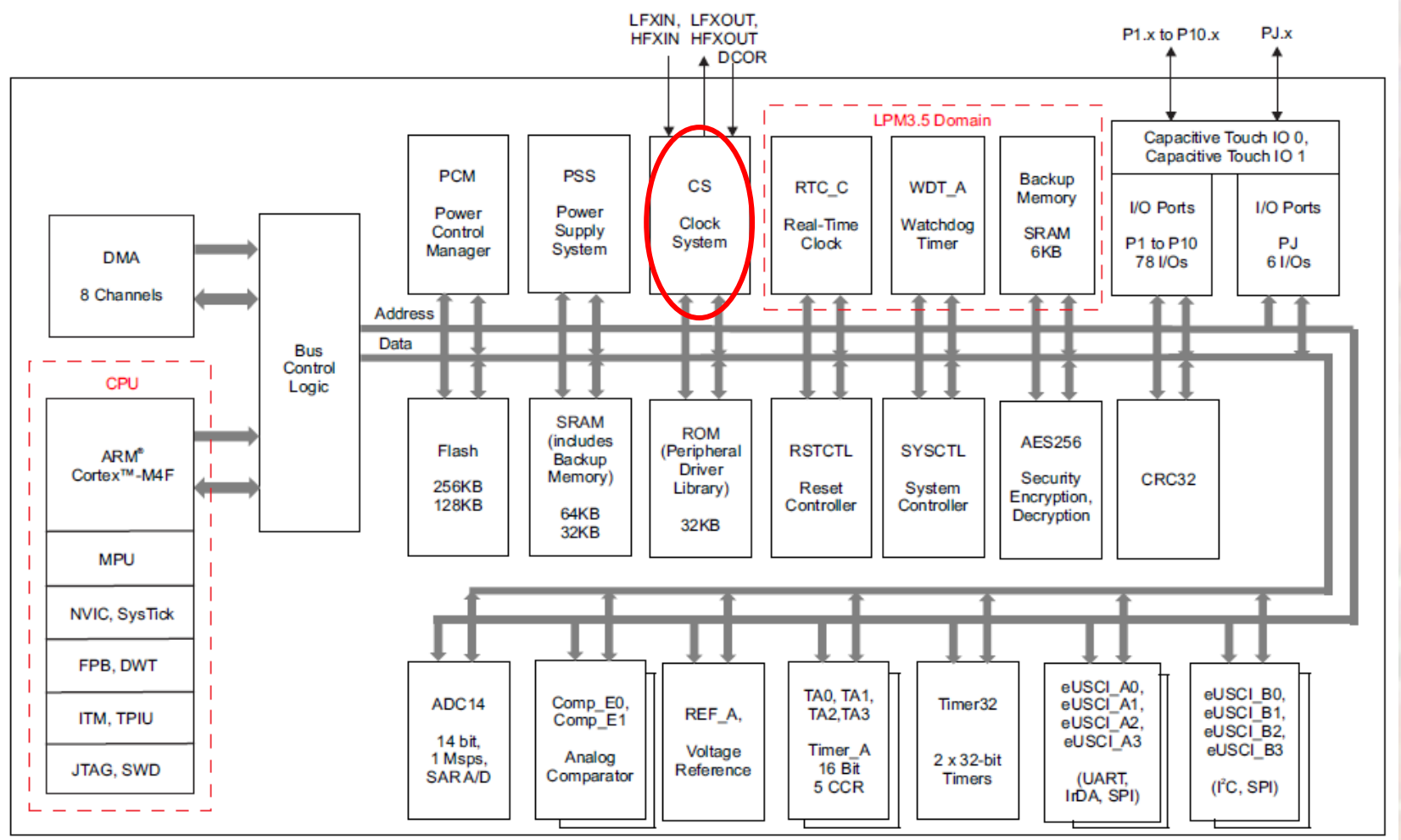
# Clock System

Last updated 5/21/19

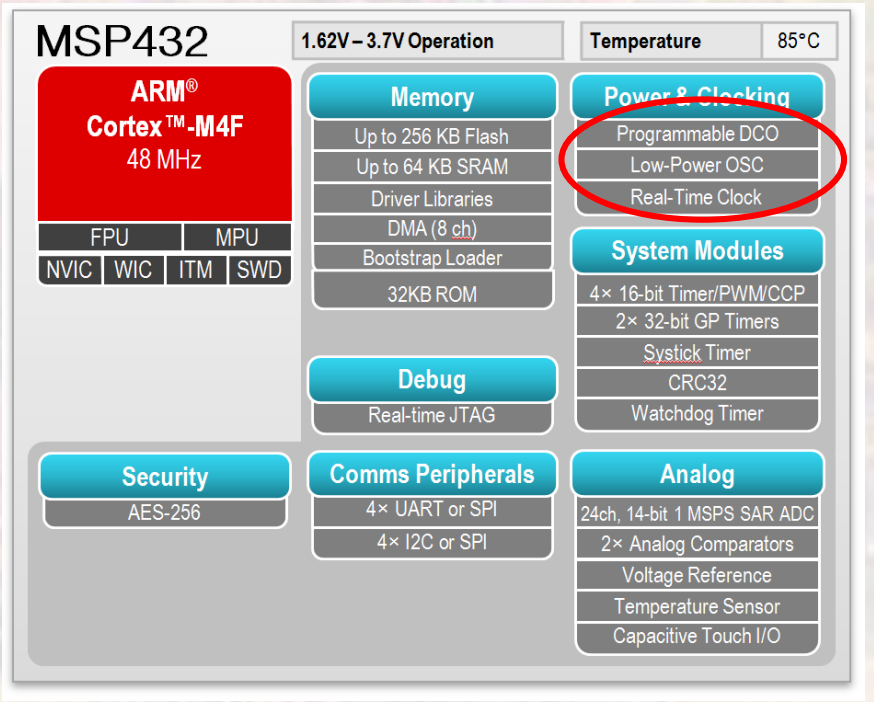
# Clock System

- MSP432 Clock System



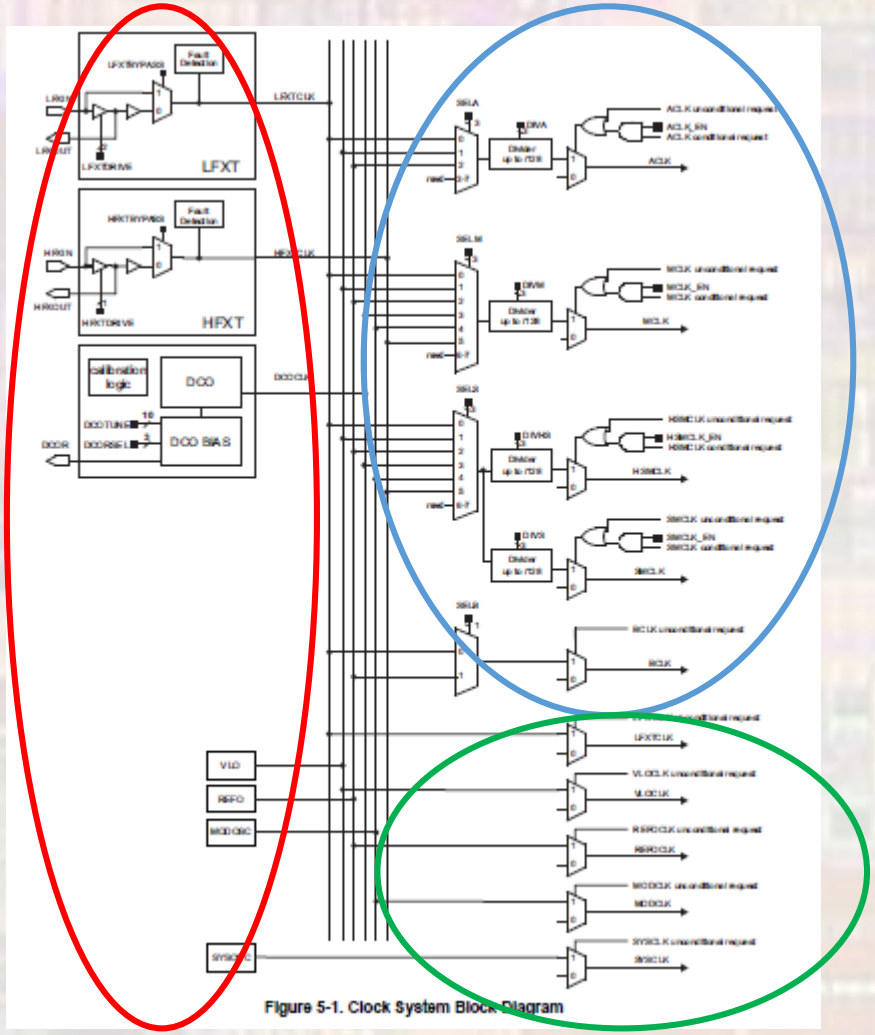
# Clock System

- MSP432 Clock System
  - 7 clock sources
  - 5 internal clock signals
  - 5 system clock signals
  - Low power
  - High power
  - Internal clock generation
  - High precision external clock generation



# Clock System

- MSP432 Clock System
  - 7 clock sources
  - 5 internal clock signals
  - 5 system clock signals



# Clock System

- MSP432 Clock System
  - Clock Module Sources
    - LFXT CLK – External low frequency crystal oscillator clock
      - Up to 32KHz
      - Bypass mode to allow square wave input
    - HFXT CLK – External high frequency crystal oscillator clock
      - 1MHz to 48MHz
      - Bypass mode to allow square wave input
    - DCO CLK – Internal digitally controlled clock - Default
      - 1MHz – 48MHz
      - Default power-up mode – 3MHz

# Clock System

- MSP432 Clock System
  - Clock Module Sources
    - VLO CLK – Internal Very low power/frequency oscillator clock
      - Typically 9.4KHz
    - REFO CLK – Internal low power/frequency oscillator clock
      - 32KHz to 128KHz
    - MOD OSC - Internal low power oscillator
      - Typically 25MHz
    - SYS OSC - Internal low frequency oscillator
      - Typically 5MHz

# Clock System

- MSP432 Clock System
  - Clock Module Outputs
    - MCLK - Master clock
      - Software selectable as LFXTCLK, VLOCLK, REFOCLK, DCOCLK, MODCLK, or HFXTCLK
      - Can be divided by 1, 2, 4, 8, 16, 32, 64, or 128
      - Used by the CPU and peripheral module interfaces
      - Used directly by some peripheral modules
    - HSMCLK - Subsystem master clock
      - Software selectable as LFXTCLK, VLOCLK, REFOCLK, DCOCLK, MODCLK, or HFXTCLK
      - Can be divided by 1, 2, 4, 8, 16, 32, 64, or 128
      - Used by individual peripheral modules

# Clock System

- MSP432 Clock System
  - Clock Module Outputs

    - SMCLK - Low-speed subsystem master clock
      - Uses the HSMCLK
      - Can be divided by 1, 2, 4, 8, 16, 32, 64, or 128
      - Limited to half of the maximum frequency of HSMCLK
      - Selectable by individual peripheral modules

    - ACLK - Auxiliary clock
      - Software selectable as LFXTCLK, VLOCLK, or REFOCLK
      - Can be divided by 1, 2, 4, 8, 16, 32, 64 or 128
      - Selectable by individual peripheral modules.
      - Limited to a maximum of 128 kHz.

# Clock System

- MSP432 Clock System
  - Clock Module Outputs
    - BCLK - Low-speed backup domain clock
      - Software selectable as LFXTCLK and REFOCLK
      - Primarily used in the backup domain
      - Limited to a maximum of 32.768 kHz.

# Clock System

- MSP432 Clock System Registers

**Table 5-2. CS Registers**

| Offset | Acronym | Register Name | Type | Access | Reset | Section |
|---|---|---|---|---|---|---|
| 00h | CSKEY | Key Register | Read/write | Word | 0000_A596h | Section 5.3.1 |
| 04h | CSCTL0 | Control 0 Register | Read/write | Word | 0001_0000h | Section 5.3.2 |
| 08h | CSCTL1 | Control 1 Register | Read/write | Word | 0000_0033h | Section 5.3.3 |
| 0Ch | CSCTL2 | Control 2 Register | Read/write | Word | 0001_0003h | Section 5.3.4 |
| 10h | CSCTL3 | Control 3 Register | Read/write | Word | 0000_00BBh | Section 5.3.5 |
| 30h | CSCLKEN | Clock Enable Register | Read/write | Word | 0000_000Fh | Section 5.3.6 |
| 34h | CSSTAT | Status Register | Read | Word | 0000_0003h | Section 5.3.7 |
| 40h | CSIE | Interrupt Enable Register | Read/write | Word | 0000_0000h | Section 5.3.8 |
| 48h | CSIFG | Interrupt Flag Register | Read | Word | 0000_0001h | Section 5.3.9 |
| 50h | CSCLRIFG | Clear Interrupt Flag Register | Write | Word | 0000_0000h | Section 5.3.10 |
| 58h | CSSETIFG | Set Interrupt Flag Register | Write | Word | 0000_0000h | Section 5.3.11 |
| 60h | CSDCOERCAL0 | DCO External Resistor Calibration 0 Register | Read/Write | Word | 0100_0000h | Section 5.3.12 |
| 64h | CSDCOERCAL1 | DCO External Resistor Calibration 1 Register | Read/Write | Word | 0000_0100h | Section 5.3.13 |

CS->KEY, CTL0, CTL1, … CS->DCOERCAL1

# Clock System

- MSP432 Clock System Registers

**Figure 5-5. CSKEY Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | | | |
| 23 | 22 | 21 | 20 | 19 | | | |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CSKEY | | | | | | | |
| rw-1 | rw-0 | rw-1 | rw-0 | rw-0 | rw-1 | rw-0 | rw-1 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CSKEY | | | | | | | |
| rw-1 | rw-0 | rw-0 | rw-1 | rw-0 | rw-1 | rw-1 | rw-0 |

Must write the correct Key value before any changes can be made to the clock system

**Table 5-3. CSKEY Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-16 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 15- 0 | CSKEY | RW | A596h | Write CSKEY = xxxx_695Ah to unlock CS registers. All 16 LSBs need to be written together.<br>Writing CSKEY with any other value causes CS registers to be locked and any writes to these registers are ignored, while reads are still performed. Always reads back A596h. |

# Clock System

- MSP432 Clock System Registers
  - Control Register 0

**Figure 5-6. CSCTL0 Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | Reserved |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | rw-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DCOEN | DCORES | Reserved | | | DCORSEL | | |
| rw-0 | rw-0 | r-0 | r-0 | r-0 | rw-0 | rw-0 | rw-1 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | Reserved | | | DCOTUNE | |
| r-0 | r-0 | r-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DCOTUNE | | | | | | | |
| rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 |

# Clock System

- MSP432 Clock System Registers
  - Control Register 0

**Table 5-4. CSCTL0 Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-25 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 24 | Reserved | RW | 0h | Reserved. Must be written as zero. |
| 23 | DCOEN | RW | 0h | Enables the DCO oscillator regardless if used as a clock resource.<br>0b = DCO is on if it is used as a source for MCLK, HSMCLK , or SMCLK and clock is requested , otherwise it is disabled.<br>1b = DCO is on. |
| 22 | DCORES | RW | 0h | Enables the DCO external resistor mode.<br>0b = Internal resistor mode<br>1b = External resistor mode |
| 21-19 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 18-16 | DCORSEL | RW | 1h | DCO frequency range select. Selects frequency range settings for the DCO.<br>000b = Nominal DCO Frequency (MHz): 1.5; Nominal DCO Frequency Range (MHz): 1 to 2<br>001b = Nominal DCO Frequency (MHz): 3; Nominal DCO Frequency Range (MHz): 2 to 4<br>010b = Nominal DCO Frequency (MHz): 6; Nominal DCO Frequency Range (MHz): 4 to 8<br>011b = Nominal DCO Frequency (MHz): 12; Nominal DCO Frequency Range (MHz): 8 to 16<br>100b = Nominal DCO Frequency (MHz): 24; Nominal DCO Frequency Range (MHz): 16 to 32<br>101b = Nominal DCO Frequency (MHz): 48; Nominal DCO Frequency Range (MHz): 32 to 64<br>110b to 111b = Nominal DCO Frequency (MHz): Reserved--defaults to 1.5 when selected; Nominal DCO Frequency Range (MHz): Reserved--defaults to 1 to 2 when selected. |
| 15-13 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 12-10 | Reserved | RW | 0h | Reserved. Must be written as zero. |
| 9-0 | DCOTUNE | RW | 0h | DCO frequency tuning select. 2s complement representation. Value represents an offset from the calibrated center frequency for the range selected by the DCORSEL bits. |

Default Power-on State
DCO – on, 3MHz clock

# Clock System

- MSP432 Clock System Registers
  - Control Register 1

**Figure 5-7. CSCTL1 Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | DIVS | | | Reserved | DIVA | | |
| r-0 | rw-0 | rw-0 | rw-0 | r-0 | rw-0 | rw-0 | rw-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | DIVHS | | | Reserved | DIVM | | |
| r-0 | rw-0 | rw-0 | rw-0 | r-0 | rw-0 | rw-0 | rw-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | Reserved | | SELB | Reserved | SELA | | |
| r-0 | r-0 | r-0 | rw-0 | r-0 | rw-0 | rw-0 | rw-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | SELS | | | Reserved | SELM | | |
| r-0 | rw-0 | rw-1 | rw-1 | r-0 | rw-0 | rw-1 | rw-1 |

# Clock System

- MSP432 Clock System Registers
  - Control Register 1

Table 5-5. CSCTL1 Register Description

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 30-28 | DIVS | RW | 0h | SMCLK source divider.<br>000b = f(SMCLK)/1<br>001b = f(SMCLK)/2<br>010b = f(SMCLK)/4<br>011b = f(SMCLK)/8<br>100b = f(SMCLK)/16<br>101b = f(SMCLK)/32<br>110b = f(SMCLK)/64<br>111b = f(SMCLK)/128 |
| 27 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 26-24 | DIVA | RW | 0h | ACLK source divider.<br>000b = f(ACLK)/1<br>001b = f(ACLK)/2<br>010b = f(ACLK)/4<br>011b = f(ACLK)/8<br>100b = f(ACLK)/16<br>101b = f(ACLK)/32<br>110b = f(ACLK)/64<br>111b = f(ACLK)/128 |
| 23 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 22-20 | DIVHS | RW | 0h | HSMCLK source divider.<br>000b = f(HSMCLK)/1<br>001b = f(HSMCLK)/2<br>010b = f(HSMCLK)/4<br>011b = f(HSMCLK)/8<br>100b = f(HSMCLK)/16<br>101b = f(HSMCLK)/32<br>110b = f(HSMCLK)/64<br>111b = f(HSMCLK)/128 |
| 19 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 18-16 | DIVM | RW | 0h | MCLK source divider.<br>000b = f(MCLK)/1<br>001b = f(MCLK)/2<br>010b = f(MCLK)/4<br>011b = f(MCLK)/8<br>100b = f(MCLK)/16<br>101b = f(MCLK)/32<br>110b = f(MCLK)/64<br>111b = f(MCLK)/128 |

Clock Dividers

# Clock System

- MSP432 Clock System Registers
  - Control Register 1

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 12 | SELB | RW | 0h | Selects the BCLK source.<br>0b = LFXTCLK<br>1b = REFOCLK |
| 11 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 10-8 | SELA | RW | 0h | Selects the ACLK source.<br>000b = LFXTCLK<br>001b = VLOCLK<br>010b = REFOCLK<br>011b-111b = Reserved for future use. Defaults to REFOCLK. Not recommended for use to ensure future compatibilities. |
| 7 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 6-4 | SELS | RW | 3h | Selects the SMCLK and HSMCLK source.<br>000b = LFXTCLK<br>001b = VLOCLK<br>010b = REFOCLK<br>011b = DCOCLK<br>100b = MODOSC<br>101b = HFXTCLK<br>110b-111b = Reserved for future use. Defaults to DCOCLK. Not recommended for use to ensure future compatibilities. |
| 3 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 2-0 | SELM | RW | 3h | Selects the MCLK source.<br>000b = LFXTCLK<br>001b = VLOCLK<br>010b = REFOCLK<br>011b = DCOCLK<br>100b = MODOSC<br>101b = HFXTCLK<br>110b-111b = Reserved for future use. Defaults to DCOCLK. Not recommended for use to ensure future compatibilities. |

Clock Selectors

# Clock System

- MSP432 Clock System Registers
  - Control Register 2

**Figure 5-8. CSCTL2 Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | HFXTBYPASS | HFXT_EN |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | rw-0 | rw-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | HFXTFREQ | | | Reserved | | Reserved | HFXTDRIVE |
| r-0 | rw-0 | rw-0 | rw-0 | r-0 | rw-0 | rw-0 | rw-1 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | LFXTBYPASS | LFXT_EN |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | rw-0 | rw-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | | | | | LFXTDRIVE | |
| rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-1 | rw-1 |

# Clock System

- MSP432 Clock System Registers
  - Control Register 2

**Table 5-6. CSCTL2 Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-26 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 25 | HFXTBYPASS | RW | 0h | HFXT bypass select.<br>0b = HFXT sourced by external crystal.<br>1b = HFXT sourced by external square wave. |
| 24 | HFXT_EN | RW | 0h | Turns on the HFXT oscillator regardless if used as a clock resource.<br>0b = HFXT is on if it is used as a source for MCLK, HSMCLK , or SMCLK and is selected via the port selection and not in bypass mode of operation.<br>1b = HFXT is on if HFXT is selected via the port selection and HFXT is not in bypass mode of operation. |
| 23 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 22-20 | HFXTFREQ | RW | 0h | HFXT frequency selection. These bits must be set to the appropriate value based on the frequency of the crystal connected. These bits are don't care in the HFXT bypass mode of operation.<br>000b = 1 MHz to 4 MHz<br>001b = >4 MHz to 8 MHz<br>010b = >8 MHz to 16 MHz<br>011b = >16 MHz to 24 MHz<br>100b = >24 MHz to 32 MHz<br>101b = >32 MHz to 40 MHz<br>110b = >40 MHz to 48 MHz<br>111b = Reserved for future use. |
| 19 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 18-17 | Reserved | RW | 0h | Reserved. |
| 16 | HFXTDRIVE | RW | 1h | HFXT oscillator drive selection. Reset value is 1h when HFXT available, and 0h when HFXT not available. This bit is a don't care in the HFXT bypass mode of operation.<br>0b = To be used for HFXTFREQ setting 000b<br>1b = To be used for HFXTFREQ settings 001b to 110b |
| 15-10 | Reserved | R | 0h | Reserved. Always reads as 0. |

HFXT Configuration

# Clock System

- MSP432 Clock System Registers
  - Control Register 2

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 9 | LFXTBYPASS | RW | 0h | LFXT bypass select.<br>0b = LFXT sourced by external crystal.<br>1b = LFXT sourced by external square wave. |
| 8 | LFXT_EN | RW | 0h | Turns on the LFXT oscillator regardless if used as a clock resource.<br>0b = LFXT is on if it is used as a source for ACLK, MCLK, HSMCLK , or SMCLK and is selected via the port selection and not in bypass mode of operation.<br>1b = LFXT is on if LFXT is selected via the port selection and LFXT is not in bypass mode of operation. |
| 7 | Reserved | RW | 0h | Reserved. Must be written as zero. |
| 6-3 | Reserved | RW | 0h | Reserved. Must be written as zero. |
| 2 | Reserved | RW | 0h | Reserved. |
| 1-0 | LFXTDRIVE | RW | 3h | The LFXT oscillator current can be adjusted to its drive needs.<br>0h = Lowest drive strength and current consumption LFXT oscillator.<br>1h = Increased drive strength LFXT oscillator.<br>2h = Increased drive strength LFXT oscillator.<br>3h = Maximum drive strength and maximum current consumption LFXT oscillator. |

LFXT Configuration

# Clock System

- MSP432 Clock System Registers
  - Control Register 3

**Figure 5-9. CSCTL3 Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FCNTHF_EN | RFCNTHF | FCNTHF | | FCNTLF_EN | RFCNTLF | FCNTLF | |
| rw-(1) | w-0 | rw-(1) | rw-(1) | rw-(1) | w-0 | rw-(1) | rw-(1) |

**Table 5-7. CSCTL3 Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-8 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 7 | FCNTHF_EN | RW | 1h | Enable start fault counter for HFXT.<br>0b = Startup fault counter disabled. Counter is cleared.<br>1b = Startup fault counter enabled |
| 6 | RFCNTHF | W | 0h | Reset start fault counter for HFXT. Write 1 only. Self clears once written.<br>0b = Not applicable. Always reads as zero due to self clearing.<br>1b = Restarts the counter immediately. |
| 5-4 | FCNTHF | RW | 3h | Start flag counter for HFXT. Selects number of HFXT cycles before HFXTIFG can be cleared.<br>00b = 2048 cycles<br>01b = 4096 cycles<br>10b = 8192 cycles<br>11b = 16384 cycles |
| 3 | FCNTLF_EN | RW | 1h | Enable start fault counter for LFXT.<br>0b = Startup fault counter disabled. Counter is cleared.<br>1b = Startup fault counter enabled |
| 2 | RFCNTLF | W | 0h | Reset start fault counter for LFXT. Write 1 only. Self clears once written.<br>0b = Not applicable. Always reads as zero due to self clearing.<br>1b = Restarts the counter immediately. |
| 0-1 | FCNTLF | RW | 3h | Start flag counter for LFXT. Selects number of LFXT cycles before LFXTIFG can be cleared.<br>00b = 4096 cycles<br>01b = 8192 cycles<br>10b = 16384 cycles<br>11b = 32768 cycles |

# Clock System

- MSP432 Clock System Registers
  - Enable Register

**Figure 5-10. CSCLKEN Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| REFOFSEL | Reserved | | | | MODOSC_EN | REFO_EN | VLO_EN |
| rw-0 | r-0 | r-0 | r-0 | r-0 | rw-0 | rw-0 | rw-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | | | SMCLK_EN | HSMCLK_EN | MCLK_EN | ACLK_EN |
| r-0 | r-0 | r-0 | r-0 | rw-1 | rw-1 | rw-1 | rw-1 |

# Clock System

- MSP432 Clock System Registers
  - Enable Register

Table 5-8. CSCLKEN Register Description

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-16 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 15 | REFOFSEL | RW | 0h | Selects REFO nominal frequency.<br>0b = 32.768 kHz<br>1b = 128 kHz |
| 14-11 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 10 | MODOSC_EN | RW | 0h | Turns on the MODOSC oscillator regardless if used as a clock resource.<br>0b = MODOSC is on only if it is used as a source for ACLK, MCLK, HSMCLK , or SMCLK.<br>1b = MODOSC is on |
| 9 | REFO_EN | RW | 0h | Turns on the REFO oscillator regardless if used as a clock resource.<br>0b = REFO is on only if it is used as a source for ACLK, MCLK, HSMCLK , or SMCLK.<br>1b = REFO is on |
| 8 | VLO_EN | RW | 0h | Turns on the VLO oscillator regardless if used as a clock resource.<br>0b = VLO is on only if it is used as a source for ACLK, MCLK, HSMCLK , or SMCLK.<br>1b = VLO is on |
| 7-4 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 3 | SMCLK_EN | RW | 1h | SMCLK system clock conditional request enable<br>0b = SMCLK disabled regardless of conditional clock requests<br>1b = SMCLK enabled based on any conditional clock requests. |
| 2 | HSMCLK_EN | RW | 1h | HSMCLK system clock conditional request enable<br>0b = HSMCLK disabled regardless of conditional clock requests<br>1b = HSMCLK enabled based on any conditional clock requests. |
| 1 | MCLK_EN | RW | 1h | MCLK system clock conditional request enable<br>0b = MCLK disabled regardless of conditional clock requests<br>1b = MCLK enabled based on any conditional clock requests. |
| 0 | ACLK_EN | RW | 1h | ACLK system clock conditional request enable<br>0b = ACLK disabled regardless of conditional clock requests<br>1b = ACLK enabled based on any conditional clock requests. |

# Clock System

- MSP432 Clock System Registers
  - Status Register

**Figure 5-11. CSSTAT Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | BCLK_READY | SMCLK_READY | HSMCLK_READY | MCLK_READY | ACLK_READY |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| REFOCLK_ON | LFXTCLK_ON | VLOCLK_ON | MODCLK_ON | SMCLK_ON | HSMCLK_ON | MCLK_ON | ACLK_ON |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REFO_ON | LFXT_ON | VLO_ON | MODOSC_ON | Reserved | HFXT_ON | DCOBIAS_ON | DCO_ON |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-1 | r-1 |

# Clock System

- MSP432 Clock System Registers
  - Status Register

Table 5-9. CSSTAT Register Description

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-29 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 28 | BCLK_READY | R | 0h | BCLK Ready status. This bit indicates whether the clock is stable after a change in the frequency settings.<br>0b = Not ready<br>1b = Ready |
| 27 | SMCLK_READY | R | 0h | SMCLK Ready status. This bit indicates whether the clock is stable after a change in the frequency/divider settings.<br>0b = Not ready<br>1b = Ready |
| 26 | HSMCLK_READY | R | 0h | HSMCLK Ready status. This bit indicates whether the clock is stable after a change in the frequency/divider settings.<br>0b = Not ready<br>1b = Ready |
| 25 | MCLK_READY | R | 0h | MCLK Ready status. This bit indicates whether the clock is stable after a change in the frequency/divider settings.<br>0b = Not ready<br>1b = Ready |
| 24 | ACLK_READY | R | 0h | ACLK Ready status. This bit indicates whether the clock is stable after a change in the frequency/divider settings.<br>0b = Not ready<br>1b = Ready |
| 23 | REFOCLK_ON | R | 0h | REFOCLK system clock status<br>0b = Inactive<br>1b = Active |
| 22 | LFXTCLK_ON | R | 0h | LFXTCLK system clock status<br>0b = Inactive<br>1b = Active |
| 21 | VLOCLK_ON | R | 0h | VLOCLK system clock status<br>0b = Inactive<br>1b = Active |
| 20 | MODCLK_ON | R | 0h | MODCLK system clock status<br>0b = Inactive<br>1b = Active |

# Clock System

- MSP432 Clock System Registers
  - Status Register

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 19 | SMCLK_ON | R | 0h | SMCLK system clock status<br>0b = Inactive<br>1b = Active |
| 18 | HSMCLK_ON | R | 0h | HSMCLK system clock status<br>0b = Inactive<br>1b = Active |
| 17 | MCLK_ON | R | 0h | MCLK system clock status<br>0b = Inactive<br>1b = Active |
| 16 | ACLK_ON | R | 0h | ACLK system clock status<br>0b = Inactive<br>1b = Active |
| 15-8 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 7 | REFO_ON | R | 0h | REFO status<br>0b = Inactive<br>1b = Active |
| 6 | LFXT_ON | R | 0h | LFXT status.<br>0b = Inactive<br>1b = Active |
| 5 | VLO_ON | R | 0h | VLO status<br>0b = Inactive<br>1b = Active |
| 4 | MODOSC_ON | R | 0h | MODOSC status<br>0b = Inactive<br>1b = Active |
| 3 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 2 | HFXT_ON | R | 0h | HFXT status.<br>0b = Inactive<br>1b = Active |
| 1 | DCOBIAS_ON | R | 1h | DCO bias status<br>0b = Inactive<br>1b = Active |
| 0 | DCO_ON | R | 1h | DCO status<br>0b = Inactive<br>1b = Active |

# Clock System

- MSP432 Clock System Registers
  - Interrupt Enable Register

**Figure 5-12. CSIE Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | FCNTHFIE | FCNTLFIE |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | rw-0 | rw-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | DCOR_OPNIE | Reserved | Reserved | Reserved | Reserved | HFXTIE | LFXTIE |
| r-0 | rw-0 | rw-0 | rw-0 | r-0 | r-0 | rw-0 | rw-0 |

**Table 5-10. CSIE Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-10 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 9 | FCNTHFIE | RW | 0h | Start fault counter interrupt enable HFXT.<br>0b = Interrupt disabled<br>1b = Interrupt enabled |
| 8 | FCNTLFIE | RW | 0h | Start fault counter interrupt enable LFXT.<br>0b = Interrupt disabled<br>1b = Interrupt enabled |
| 7 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 6 | DCOR_OPNIE | RW | 0h | DCO external resistor open circuit fault flag interrupt enable.<br>0b = Interrupt disabled<br>1b = Interrupt enabled |
| 5 | Reserved | RW | 0h | Reserved. |
| 4 | Reserved | RW | 0h | Reserved. |
| 3 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 2 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 1 | HFXTIE | RW | 0h | HFXT oscillator fault flag interrupt enable.<br>0b = Interrupt disabled<br>1b = Interrupt enabled |
| 0 | LFXTIE | RW | 0h | LFXT oscillator fault flag interrupt enable.<br>0b = Interrupt disabled<br>1b = Interrupt enabled |

# Clock System

- MSP432 Clock System Registers
  - Interrupt Flag Register

**Figure 5-13. CSIFG Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | FCNTHFIFG | FCNTLFIFG |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-(0) | r-(0) |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | DCOR_OPNIFG | DCOR_SHTIFG | Reserved | Reserved | Reserved | HFXTIFG | LFXTIFG |
| r-0 | r-(0) | r-(0) | r-(0) | r-0 | r-0 | r-(0) | r-(1) |

# Clock System

- MSP432 Clock System Registers
  - Interrupt Flag Register

Table 5-11. CSIFG Register Description

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-10 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 9 | FCNTHFIFG | R | 0h | Start fault counter interrupt flag HFXT. If this bit is set, the FCNTIFG flag is also set.<br>0b = Start counter not expired.<br>1b = Start counter expired. |
| 8 | FCNTLFIFG | R | 0h | Start fault counter interrupt flag LFXT. If this bit is set, the FCNTIFG flag is also set.<br>0b = Start counter not expired.<br>1b = Start counter expired. |
| 7 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 6 | DCOR_OPNIFG | R | 0h | DCO external resistor open circuit fault flag. DCOR_OPNIFG can be cleared via software by CLR_DCORIFG. If the fault condition still remains, DCOR_OPNIFG is set again.<br>0b = DCO external resistor present<br>1b = DCO external resistor open circuit fault |
| 5 | DCOR_SHTIFG | R | 0h | DCO external resistor short circuit fault flag. DCOR_SHTIFG can be cleared via software by CLR bit in the RSTCTL_CSRESET_CLR register. If the fault condition still remains, DCOR_SHTIFG is set again.<br>0b = DCO external resistor present<br>1b = DCO external resistor short circuit fault |
| 4 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 3 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 2 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 1 | HFXTIFG | R | 0h | HFXT oscillator fault flag. HFXTIFG is set if a HFXT fault condition exists. HFXTIFG can be cleared via software by CLR_HFXTIFG. If the HFXT fault condition still remains, HFXTIFG is set again.<br>0b = No fault condition occurred after the last reset.<br>1b = HFXT fault. A HFXT fault occurred after the last reset. |
| 0 | LFXTIFG | R | 1h | LFXT oscillator fault flag. LFXTIFG is set if a LFXT fault condition exists. LFXTIFG can be cleared via software by CLR_LFXTIFG. If the LFXT fault condition still remains, LFXTIFG is set again.<br>0b = No fault condition occurred after the last reset.<br>1b = LFXT fault. A LFXT fault occurred after the last reset. |

# Clock System

- MSP432 Clock System Registers
  - Clear Interrupt Flag Register

**Figure 5-14. CSCLRIFG Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | CLR_FCNTHFIFG | CLR_FCNTLFIFG |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | CLR_DCOR_OPNIFG | Reserved | Reserved | Reserved | Reserved | CLR_HFXTIFG | CLR_LFXTIFG |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |

**Table 5-12. CSCLRIFG Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-10 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 9 | CLR_FCNTHFIFG | W | 0h | Start fault counter clear interrupt flag HFXT. Does not clear FCNTIFG.<br>0b = No effect<br>1b = Clear pending interrupt flag |
| 8 | CLR_FCNTLFIFG | W | 0h | Start fault counter clear interrupt flag LFXT. Does not clear FCNTIFG.<br>0b = No effect<br>1b = Clear pending interrupt flag |
| 7 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 6 | CLR_DCOR_OPNIFG | W | 0h | Clear DCO external resistor open circuit fault interrupt flag.<br>0b = No effect<br>1b = Clear pending interrupt flag |
| 5 | Reserved | W | 0h | Reserved. Always read as 0. |
| 4 | Reserved | W | 0h | Reserved. Always read as 0. |
| 3 | Reserved | W | 0h | Reserved. Always read as 0. |
| 2 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 1 | CLR_HFXTIFG | W | 0h | Clear HFXT oscillator fault interrupt flag.<br>0b = No effect<br>1b = Clear pending interrupt flag |
| 0 | CLR_LFXTIFG | W | 0h | Clear LFXT oscillator fault interrupt flag.<br>0b = No effect<br>1b = Clear pending interrupt flag |

# Clock System

- MSP432 Clock System Registers
  - Set Interrupt Flag Register

**Figure 5-15. CSSETIFG Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | SET_FCNTHFIFG | SET_FCNTLFIFG |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | SET_DCOR_OPNIFG | Reserved | Reserved | Reserved | Reserved | SET_HFXTIFG | SET_LFXTIFG |
| w1 | w1 | w1 | w1 | w1 | w1 | w1 | w1 |

**Table 5-13. CSSETIFG Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-10 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 9 | SET_FCNTHFIFG | W | 0h | Start fault counter set interrupt flag HFXT.<br>0b = No effect<br>1b = Set pending interrupt flag |
| 8 | SET_FCNTLFIFG | W | 0h | Start fault counter set interrupt flag LFXT.<br>0b = No effect<br>1b = Set pending interrupt flag |
| 7 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 6 | SET_DCOR_OPNIFG | W | 0h | Set DCO external resistor open circuit fault interrupt flag.<br>0b = No effect<br>1b = Set pending interrupt flag |
| 5 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 4 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 3 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 2 | Reserved | W | 0h | Reserved. Always reads as 0. |
| 1 | SET_HFXTIFG | W | 0h | Set HFXT oscillator fault interrupt flag.<br>0b = No effect<br>1b = Set pending interrupt flag |
| 0 | SET_LFXTIFG | W | 0h | Set LFXT oscillator fault interrupt flag.<br>0b = No effect<br>1b = Set pending interrupt flag |

# Clock System

- MSP432 Clock System Registers
  - DCO Calibration Register 0

External Resistor ONLY

**Figure 5-16. CSDCOERCAL0 Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | DCO_FCAL_RSEL04 | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | rw-<0> | rw-<1> |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DCO_FCAL_RSEL04 | | | | | | | |
| rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | DCO_TCCAL | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | rw-<0> | rw-<0> |

**Table 5-14. CSDCOERCAL0 Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-26 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 25-16 | DCO_FCAL_RSEL04 | RW | 100h | DCO frequency calibration for DCO frequency range (DCORSEL) 0 to 4. |
| 15-2 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 1-0 | DCO_TCCAL | RW | 0h | DCO Temperature compensation calibration. |

# Clock System

- MSP432 Clock System Registers
  - DCO Calibration Register 1

External Resistor ONLY

**Figure 5-17. CSDCOERCAL1 Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | DCO_FCAL_RSEL5 | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | rw-<0> | rw-<1> |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DCO_FCAL_RSEL5 | | | | | | | |
| rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> | rw-<0> |

**Table 5-15. CSDCOERCAL1 Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-10 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 9-0 | DCO_FCAL_RSEL5 | RW | 100h | DCO frequency calibration for DCO frequency range (DCORSEL) 5. |

# Clock System

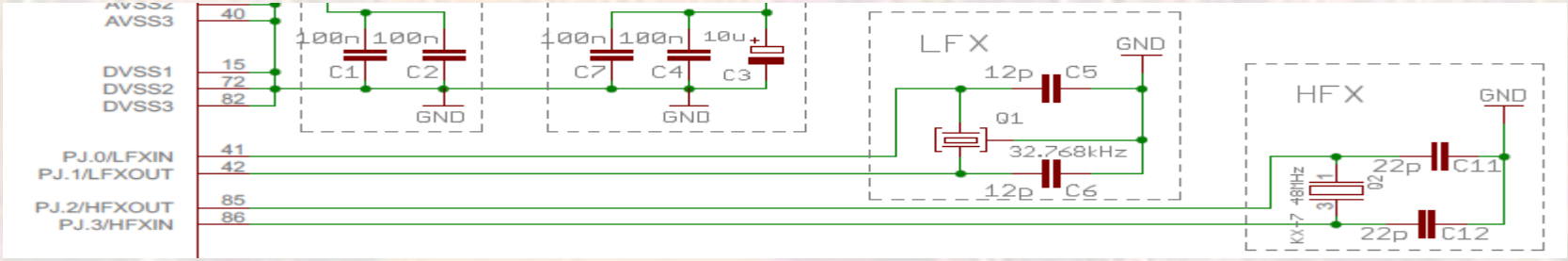
- Clock System Setup
  - Default mode is DCO at 3MHz
  - Put Power System into appropriate mode
    - e.g 48MHZ operation requires VCORE1 mode
  - Configure the clock source
    - If external – pins, enables
  - Configure the Clock System
    - Enter change code
    - Setup source selection
    - Setup frequency selection/dividers/interrupts
    - Setup output clocks
    - Clear the change code

# Clock System

- Clock System Setup
  - Configure the clock source

**Table 6-82. Port PJ (PJ.2 and PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS (1) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.2 | PJSEL0.2 | PJSEL1.3 | PJSEL0.3 | HFXT BYPASS |
| PJ.3/HFXIN | 3 | PJ.3 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | N/A | 0 | X | X | 1 | X | X |
| | | DVSS | 1 | | | | | |
| | | HFXIN crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | HFXIN bypass mode (2) | X | X | X | 0 | 1 | 1 |
| PJ.2/HFXOUT | 2 | PJ.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1(3) |
| | | N/A | 0 | see(4) | see(4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1(3) |
| | | DVSS | 1 | see(4) | see(4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1(3) |
| | | HFXOUT crystal mode (2) | X | X | X | 0 | 1 | 0 |




```
// The crystal oscillator pins default to HFXT mode but the oscillator is not active
// until these pins are configured
// Port J, bits 2,3 - set to select mode 01
PJ->SEL0 |= 0x0C;
PJ->SEL1 &= ~0x0C;
```

# Clock System

- Clock System Setup
  - Configure the clock system

**Table 5-3. CSKEY Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-16 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 15- 0 | CSKEY | RW | A596h | Write CSKEY = xxxx_695Ah to unlock CS registers. All 16 LSBs need to be written together.<br>Writing CSKEY with any other value causes CS registers to be locked and any writes to these registers are ignored, while reads are still performed. Always reads back A596h. |

```
// The Clock Source module requires a special value (Key) to be written to
// to change the clock source. Default DCO mode does not support 48MHz operation.
// Key is 0x695A (top bits are reserved) and loads into CSKEY
CS->KEY = 0x695A;
```

# Clock System

- Clock System Setup
  - Configure the clock source

| | | | | |
|---|---|---|---|---|
| 25 | HFXTBYPASS | RW | 0h | HFXT bypass select.<br>0b = HFXT sourced by external crystal.<br>1b = HFXT sourced by external square wave. |
| 24 | HFXT_EN | RW | 0h | Turns on the HFXT oscillator regardless if used as a clock resource.<br>0b = HFXT is on if it is used as a source for MCLK, HSMCLK , or SMCLK and is selected via the port selection and not in bypass mode of operation.<br>1b = HFXT is on if HFXT is selected via the port selection and HFXT is not in bypass mode of operation. |
| 22-20 | HFXTFREQ | RW | 0h | HFXT frequency selection. These bits must be set to the appropriate value based on the frequency of the crystal connected. These bits are don't care in the HFXT bypass mode of operation.<br>110b = >40 MHz to 48 MHz |
| 16 | HFXTDRIVE | RW | 1h | HFXT oscillator drive selection. Reset value is 1h when HFXT available, and 0h when HFXT not available. This bit is a don't care in the HFXT bypass mode of operation.<br>0b = To be used for HFXTFREQ setting 000b<br>1b = To be used for HFXTFREQ settings 001b to 110b |

```
// 48MHz operation requires the following in CSCTL2
//
// HFXTBYPASS to be cleared (bit 25) - not bypassing the crystal
// HFXTFREQ set to 110 (bits 22:20) - 40-48 MHz
// HFXT_EN set to 1 (bit 24)
// HFXTDRIVE set to 1 (bit 16) - based on HFXTDRIVE value
// xxxx xx01 x110 xxx1 xxxx xxxx xxxx xxxx
//                       force 0s        force 1s
CS->CTL2 = (CS->CTL2 & ~0x02100000) | 0x01610000;
```

# Clock System

- Clock System Setup
  - Configure the clock source

CSIFG

| | | | | |
|---|---|---|---|---|
| 1 | HFXTIFG | R | 0h | HFXT oscillator fault flag. HFXTIFG is set if a HFXT fault condition exists. HFXTIFG can be cleared via software by CLR_HFXTIFG. If the HFXT fault condition still remains, HFXTIFG is set again.<br>0b = No fault condition occurred after the last reset.<br>1b = HFXT fault. A HFXT fault occurred after the last reset. |

CSCLRIFG

| | | | | |
|---|---|---|---|---|
| 1 | CLR_HFXTIFG | W | 0h | Clear HFXT oscillator fault interrupt flag.<br>0b = No effect<br>1b = Clear pending interrupt flag |

```
// Check to make sure HFXT mode is stable
// The interrupt flag is set if there is a fault (not stable)
// The flag will not clear itself so you need to clear the flag
// and re-check - flag:CSIFG bit 1 (HFXTIFG), clearFlag:CSCLRIFG bit 1 (CLR_HFXTIFG)
uint32_t HFXT_fail = 100000; // set # of attempts
while(CS->IFG & 0x00000002){
  CS->CLRIFG = 0x00000002;
  HFXT_fail--;
  if(HFXT_fail == 0)// Attempt Failed - return 5
    return -5;
} // end while
```

# Clock System

- Clock System Setup
  - Configure the clock outputs

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 12 | SELB | RW | 0h | Selects the BCLK source.<br>0b = LFXTCLK<br>1b = REFOCLK |
| 11 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 10-8 | SELA | RW | 0h | Selects the ACLK source.<br>000b = LFXTCLK<br>001b = VLOCLK<br>010b = REFOCLK<br>011b-111b = Reserved for future use. Defaults to REFOCLK. Not recommended for use to ensure future compatibilities. |
| 7 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 6-4 | SELS | RW | 3h | Selects the SMCLK and HSMCLK source.<br>000b = LFXTCLK<br>001b = VLOCLK<br>010b = REFOCLK<br>011b = DCOCLK<br>100b = MODOSC<br>101b = HFXTCLK<br>110b-111b = Reserved for future use. Defaults to DCOCLK. Not recommended for use to ensure future compatibilities. |
| 3 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 2-0 | SELM | RW | 3h | Selects the MCLK source.<br>000b = LFXTCLK<br>001b = VLOCLK<br>010b = REFOCLK<br>011b = DCOCLK<br>100b = MODOSC<br>101b = HFXTCLK<br>110b-111b = Reserved for future use. Defaults to DCOCLK. Not recommended for use to ensure future compatibilities. |

Table 5-5. CSCTL1 Register Description

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 30-28 | DIVS | RW | 0h | SMCLK source divider.<br>000b = f(SMCLK)/1<br>001b = f(SMCLK)/2<br>010b = f(SMCLK)/4<br>011b = f(SMCLK)/8<br>100b = f(SMCLK)/16<br>101b = f(SMCLK)/32<br>110b = f(SMCLK)/64<br>111b = f(SMCLK)/128 |
| 27 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 26-24 | DIVA | RW | 0h | ACLK source divider.<br>000b = f(ACLK)/1<br>001b = f(ACLK)/2<br>010b = f(ACLK)/4<br>011b = f(ACLK)/8<br>100b = f(ACLK)/16<br>101b = f(ACLK)/32<br>110b = f(ACLK)/64<br>111b = f(ACLK)/128 |
| 23 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 22-20 | DIVHS | RW | 0h | HSMCLK source divider.<br>000b = f(HSMCLK)/1<br>001b = f(HSMCLK)/2<br>010b = f(HSMCLK)/4<br>011b = f(HSMCLK)/8<br>100b = f(HSMCLK)/16<br>101b = f(HSMCLK)/32<br>110b = f(HSMCLK)/64<br>111b = f(HSMCLK)/128 |
| 19 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 18-16 | DIVM | RW | 0h | MCLK source divider.<br>000b = f(MCLK)/1<br>001b = f(MCLK)/2<br>010b = f(MCLK)/4<br>011b = f(MCLK)/8<br>100b = f(MCLK)/16<br>101b = f(MCLK)/32<br>110b = f(MCLK)/64<br>111b = f(MCLK)/128 |

```
// Configure the system clocks (CSCTL1)
//
// MCLK --> HFXTCLK - bits 2:0 = 101
// SMCLK/HSMCLK --> HFXTCLK - bits 6:4 = 101
// ACLK --> REFOCLK - bits 10:8 = 010
// BCLK --> REFOCLK - bit 12 = 1
// MCLK /1 - bits 18:16 = 000
// HSMCLK /2 - bits 22:20 = 001  (max allowed is 24MHz)
// ACLK /1 - bits 26:24 = 000
// SMCLK /4 - bits 30:28 = 010 (max allowed is 12MHz
// x010 x000 x001 x000 x001 x010 x101 x101
CS->CTL1 = 0x20101255;// direct write
```

# Clock System

- Clock System Setup
  - Configure the clock outputs

```
// Clock mode change is complete
// Clear the change key to prevent unintended changes
CS->KEY = 0;
```

# Clock System

- Clock System Setup
  - Check the clock system

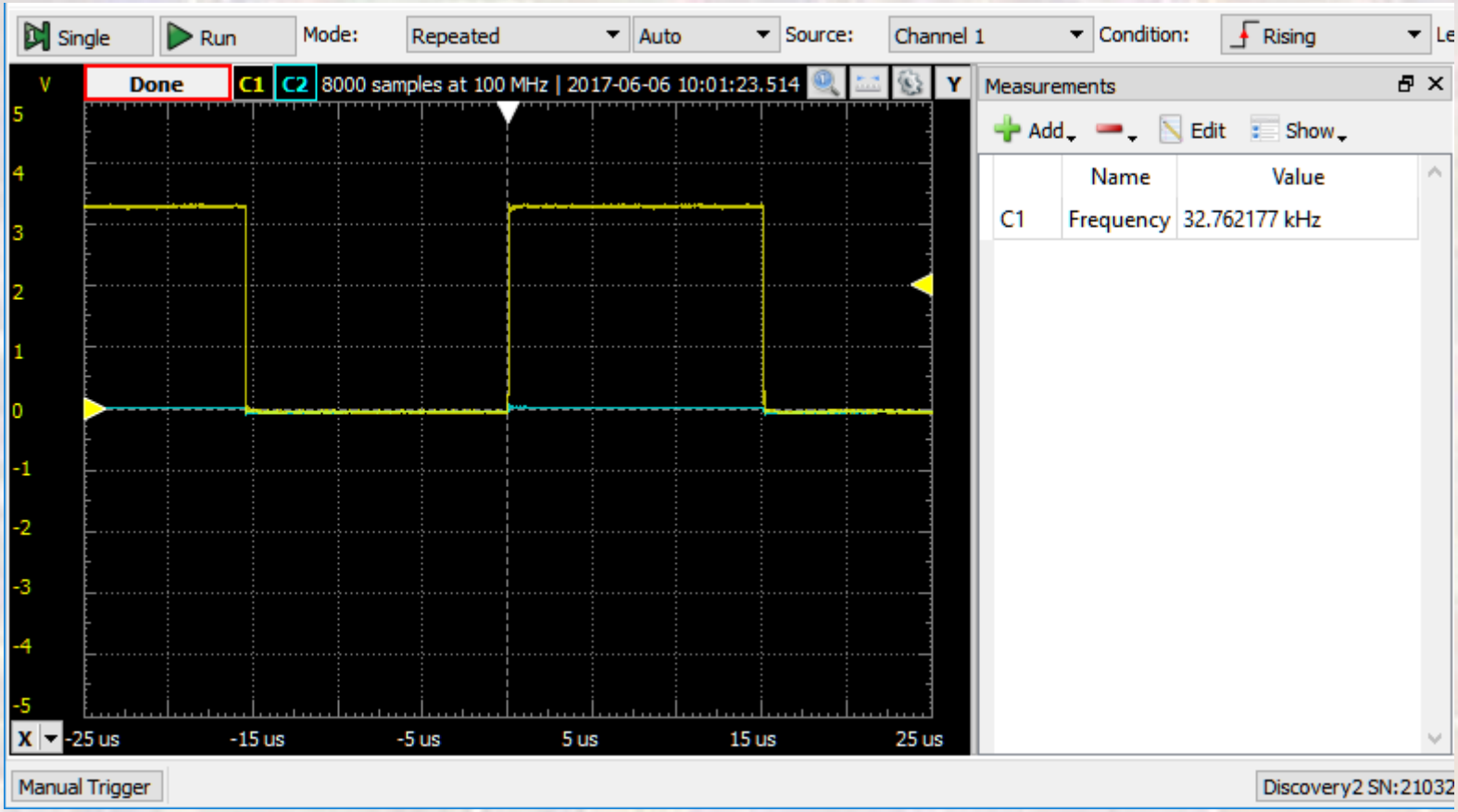
**Figure 5-11. CSSTAT Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | BCLK_READY | SMCLK_READY | HSMCLK_READY | MCLK_READY | ACLK_READY |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| REFOCLK_ON | LFXTCLK_ON | VLOCLK_ON | MODCLK_ON | SMCLK_ON | HSMCLK_ON | MCLK_ON | ACLK_ON |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REFO_ON | LFXT_ON | VLO_ON | MODOSC_ON | Reserved | HFXT_ON | DCOBIAS_ON | DCO_ON |
| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-1 | r-1 |

```
// Make sure all clocks are working properly
// Use the Status register
// HFXT_ON, MCLK_ON, SMCLK_ON, HSMCLK_ON, ACLK_ON
// MCLK_READY, HSMCLK_READY, SMCLK_READY, ACLK_READY
// xxxx 1111 xxxx 1111 xxxx xxxx xxxx x1xx
// normally would test: 0x0F020004
//     but with no other peripherals enabled, only MCLK is on, test: 0x0F020004
uint32_t CLK_fail = 100000; // set # of attempts
while((CS->STAT & 0x0F020004) != 0x0F020004){
  CLK_fail--;
  if(CLK_fail == 0)// Attempt Failed - return 6
    return -6;// some clock not working
}
```

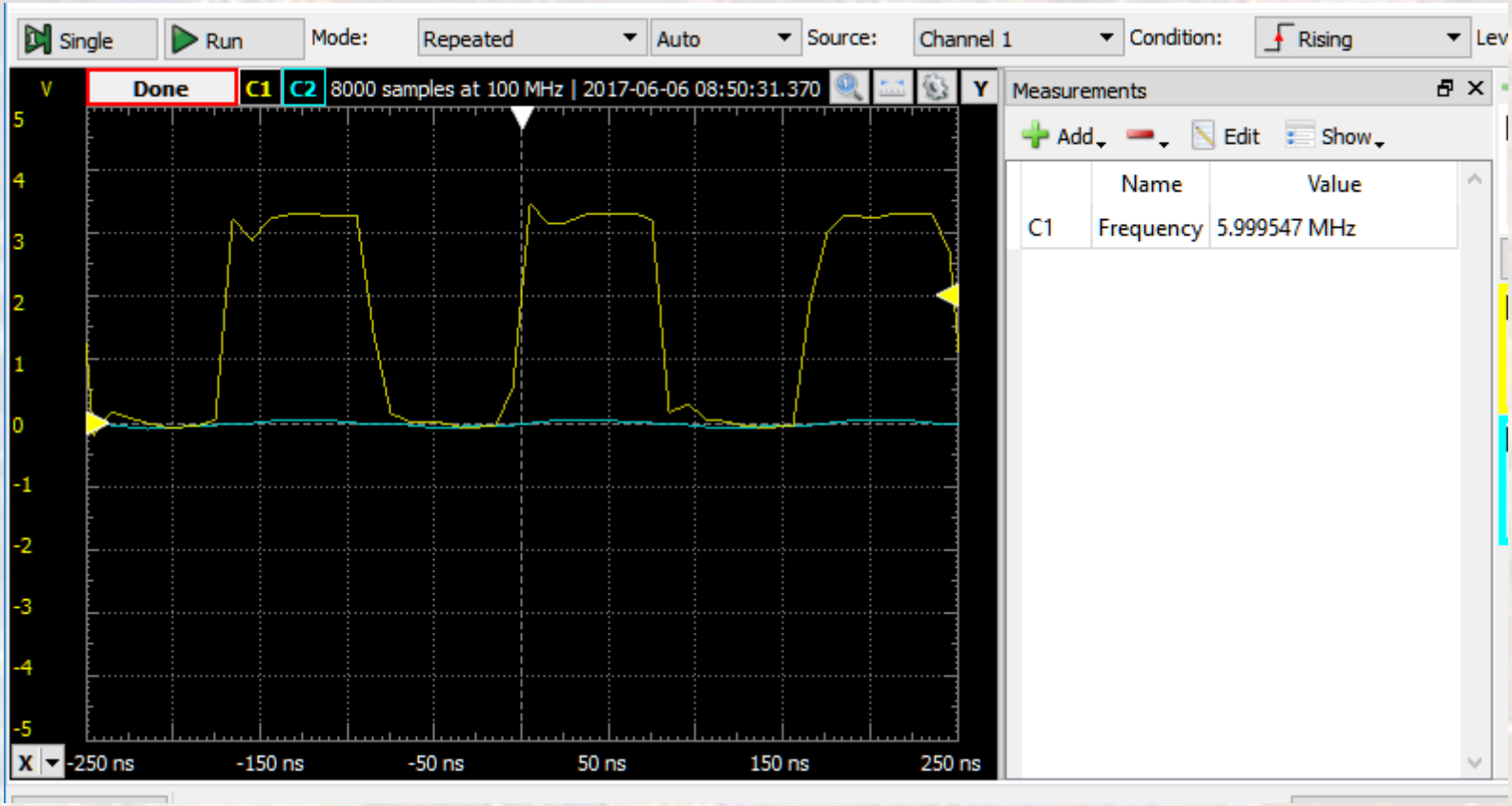
# Clock System

- Clock System Setup
  - Check the clock system – 48MHz with divide by 8
  - ACLK – 32.768KHz (REFOCLK)



# Clock System

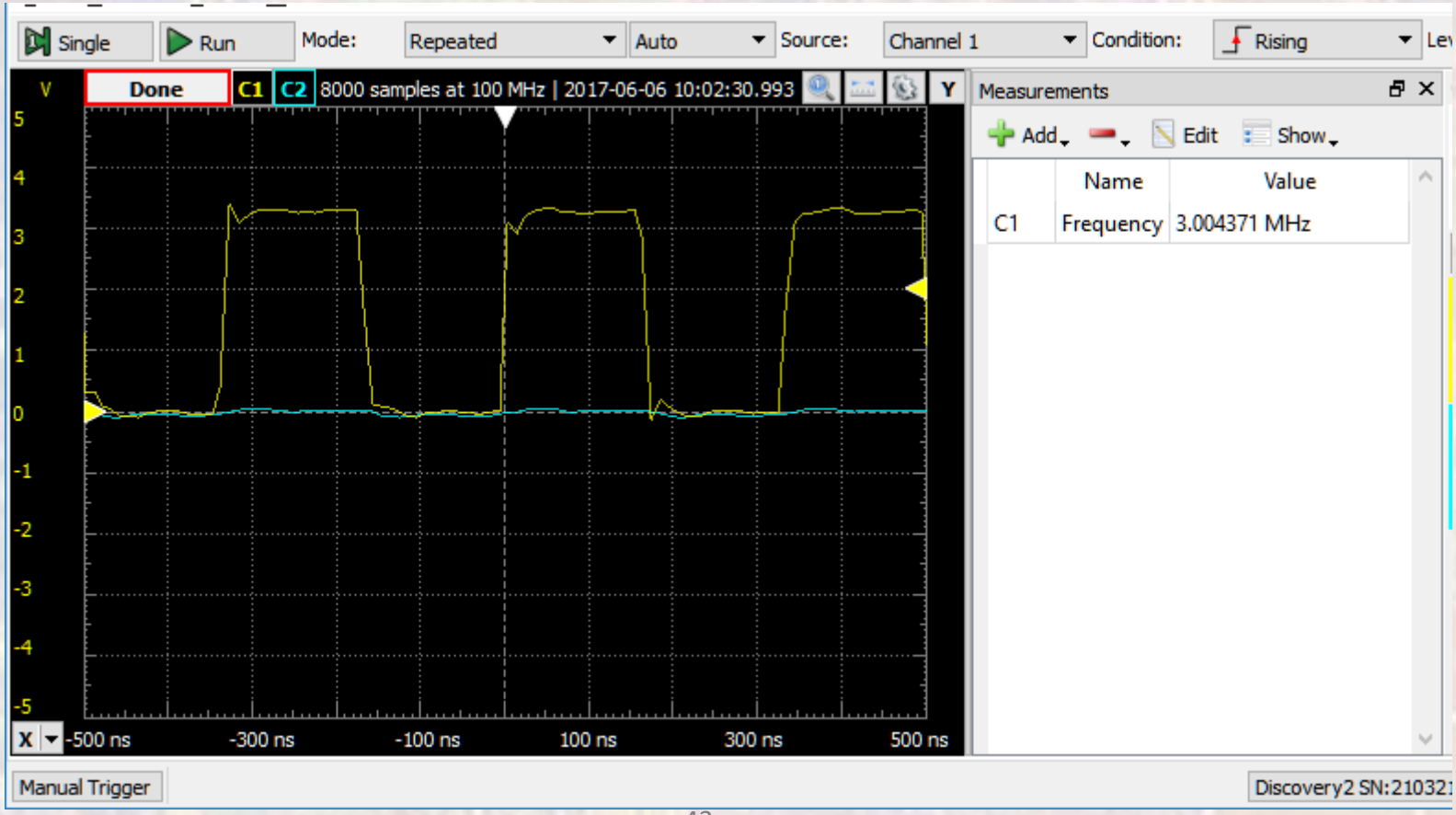
- Clock System Setup
  - Check the clock system – 48MHz with divide by 8
  - MCLK - 6MHz (HFXTCLK)



# Clock System

- Clock System Setup
  - Check the clock system – 48MHz with divide by 8
  - HSMCLK – 3MHz (HFXTCLK/2)



# Clock System

- Clock System Setup
  - Check the clock system – 48MHz with divide by 8
  - SMCLK – 1.5MHz (HFXTCLK/4)