Digital to Analog Converter / Comparator

Last updated 5/21/19

D/A

- Digital to Analog Converter
  - Converts a digital word to a fixed analog voltage level
  - Many applications
    - Electronic music
    - Audio conversion – cell phones
    - Video conversion – digital TV
    - Mechanical conversion – valve opening

D/A

- Digital to Analog Converter
  - Converts a digital word to a fixed analog voltage level
  - Many types of D/A converters
    - Resistor DAC
    - Current DAC
    - Switched Capacitor DAC
    - Delta-sigma DAC
    - Pulse width modulator

D/A

- Digital to Analog Converter Performance
  - Resolution
    - n-bit digital word can represent 2^n levels
    - 8-bit DAC → 256 levels
  - Frequency
    - Outputs are provided at a fixed rate – sampling rate
  - Accuracy
    - Linearity
    - Noise
    - Many others

D/A

- Digital to Analog Converter Performance
  - 4 bit DAC, 5v range
    - 5v / 2^4 → 0.3125v/step

Code	Output
0000	0.0v
0001	0.3125v
0010	0.625v
0011	0.9375v
…	
1101	4.0625v
1110	4.375v
1111	4.6875v

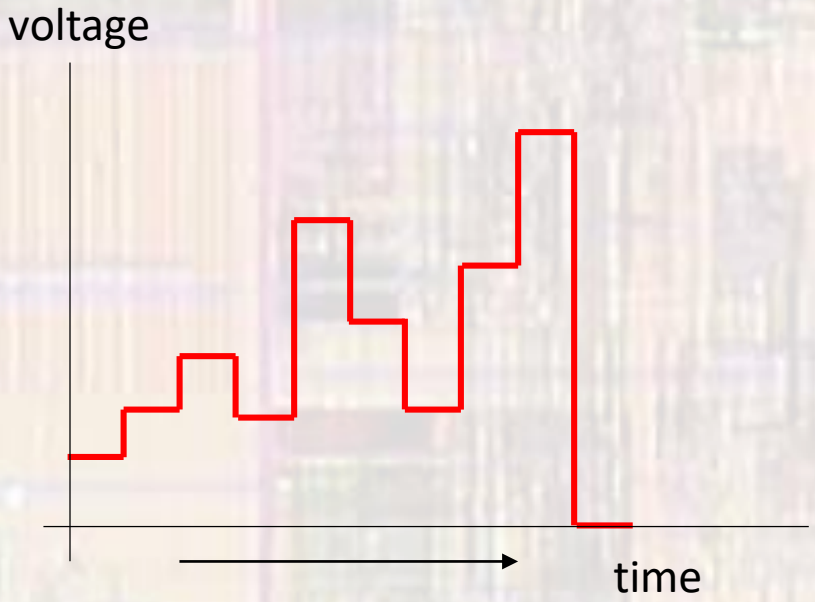
D/A

- Digital to Analog Converter Performance
  - 4 bit DAC, 5v range

Code

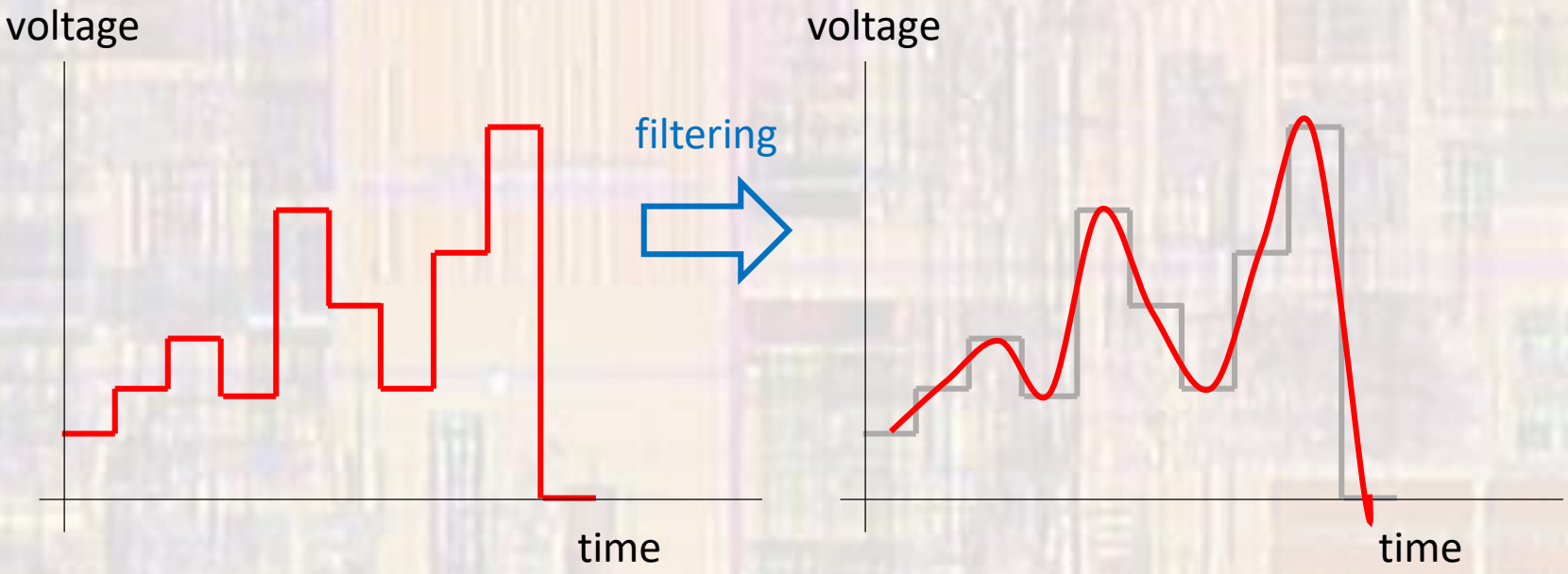
0010
0011
0100
0011
0111
0101
0011
0110
1001
0000

Time



D/A

- Digital to Analog Converter Performance
  - Typically additional signal conditioning is required to ‘clean up’ the output



D/A

- D to A Converter
  - Converts a digital word to a fixed voltage level
  - example: 4 bit code

0000 → Vout = VrefL

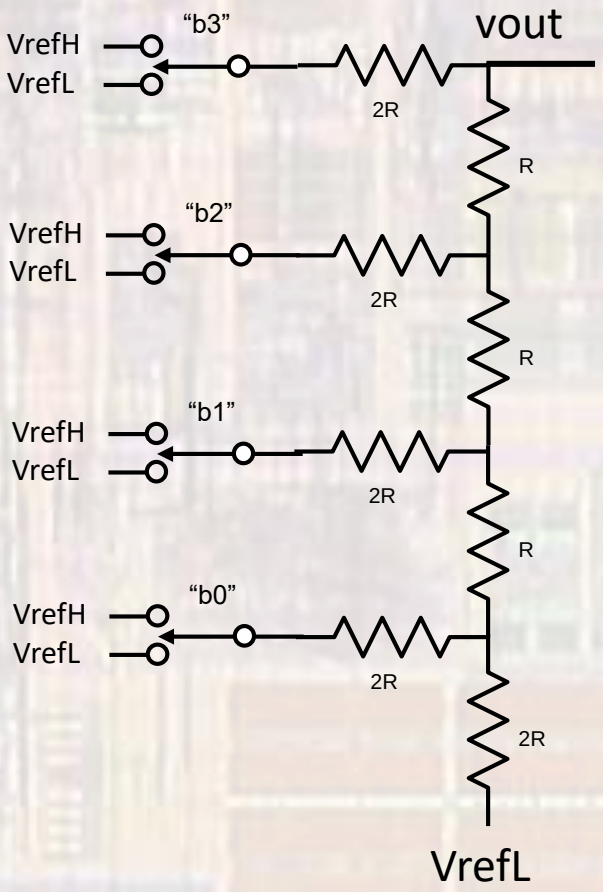
1111 → Vout = VrefL+(VrefH-VrefL)$(\frac{15}{16})$

b0 contributes 1/16
b1 contributes 1/8
b2 contributes ¼
b3 contributes ½

Let VrefL be gnd

0110 → Vout = VrefL+(VrefH-VrefL)$(\frac{1}{4}+\frac{1}{8})$

1000 → Vout = VrefL+(VrefH-VrefL)$(\frac{1}{2})$



D/A

- D to A Converter
  - Converts a digital word to a fixed voltage level
  - example: 4 bit code

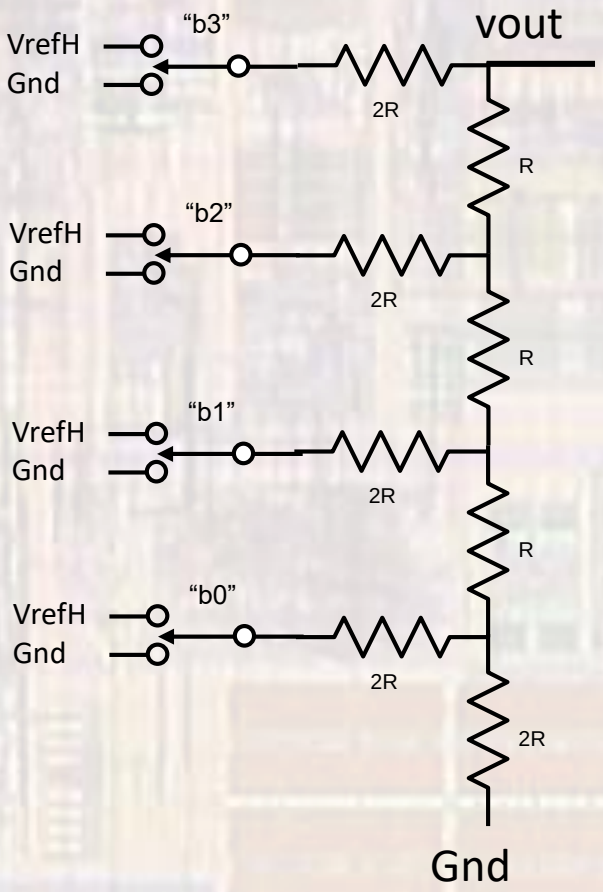
    0000 → Vout = 0

    1111 → Vout = VrefH*$(\frac{15}{16})$

    b0 contributes 1/16
    b1 contributes 1/8
    b2 contributes ¼
    b3 contributes ½

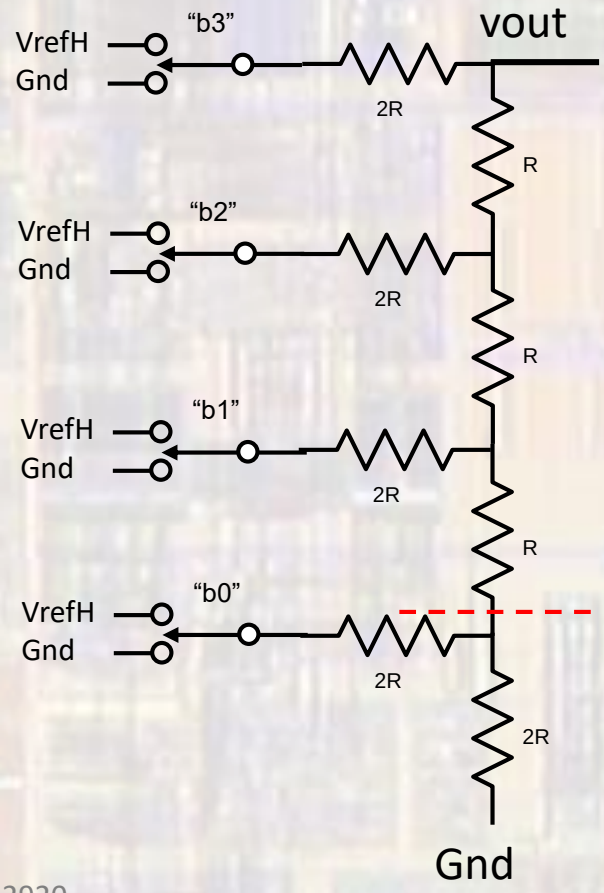
    0110 → Vout = VrefH$(\frac{1}{4}+\frac{1}{8})$

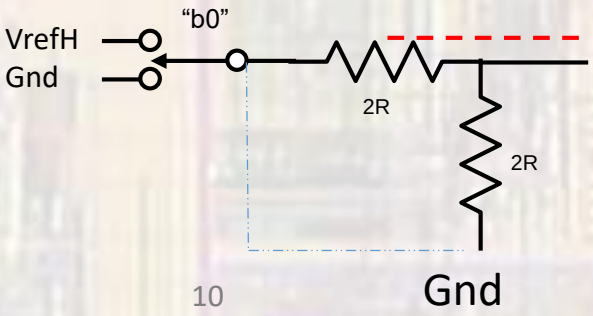
    1000 → Vout = VrefH$(\frac{1}{2})$

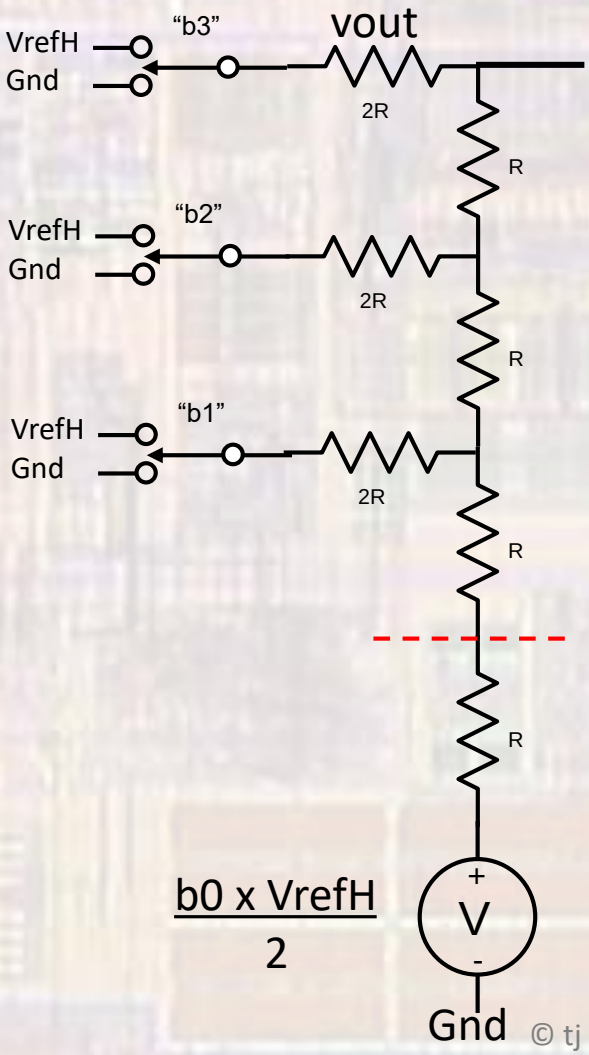


D/A

- D to A Converter
  - Superposition and Thevenin Equivalents

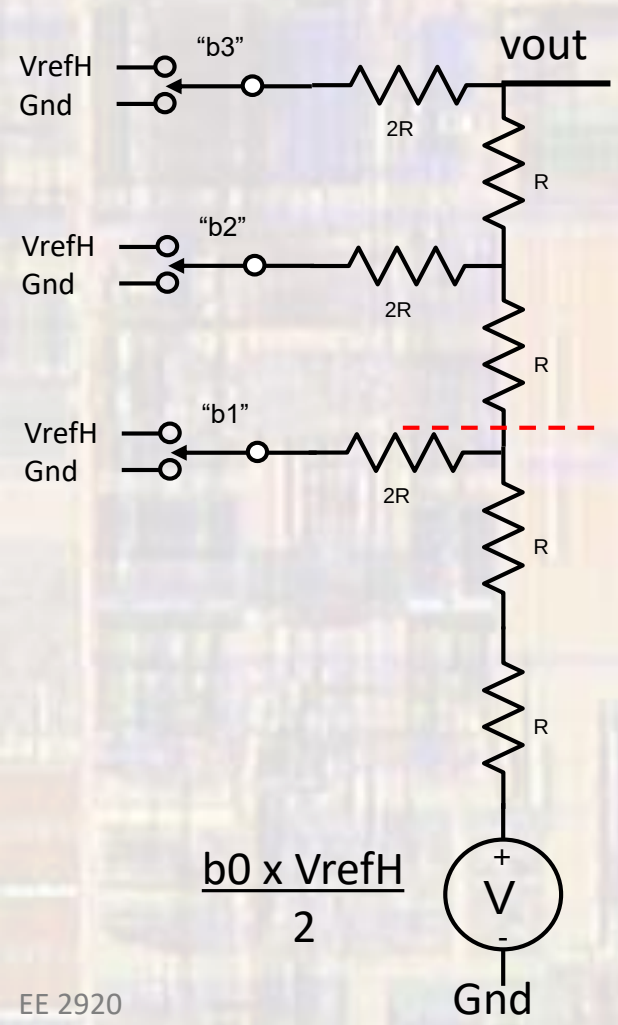


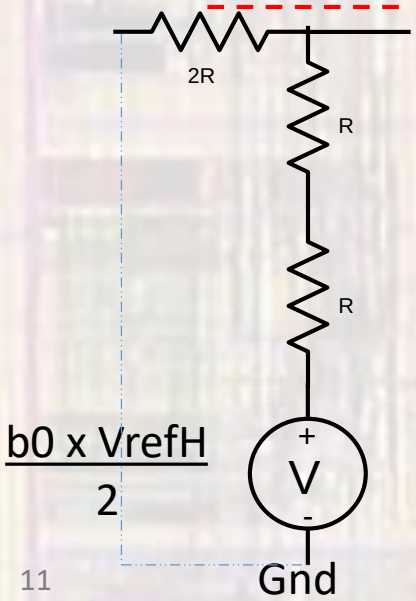


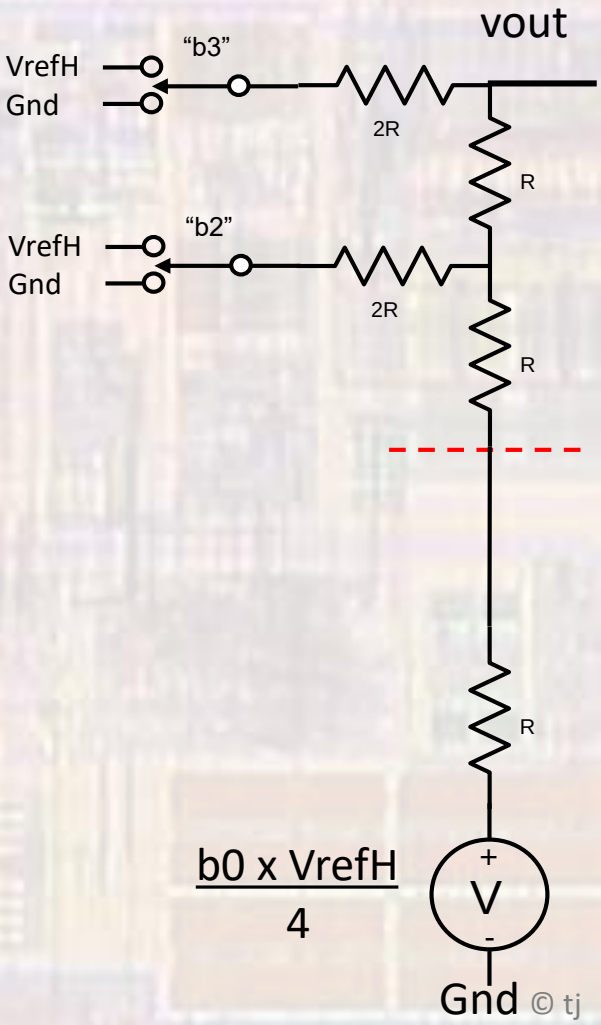


D/A

- D to A Converter

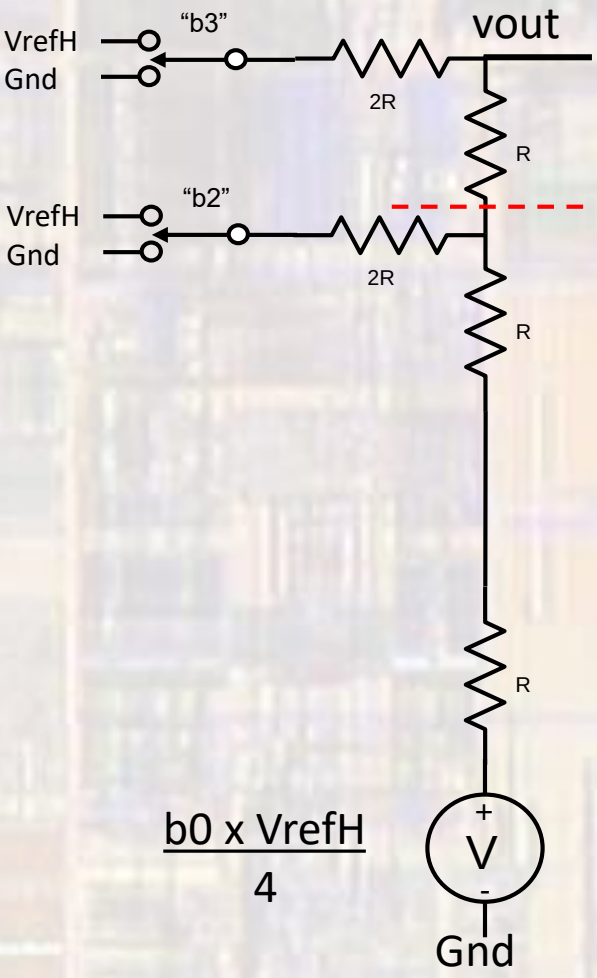


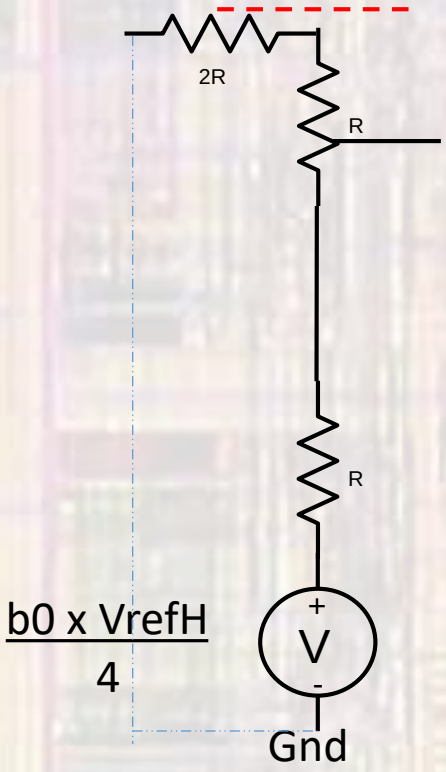


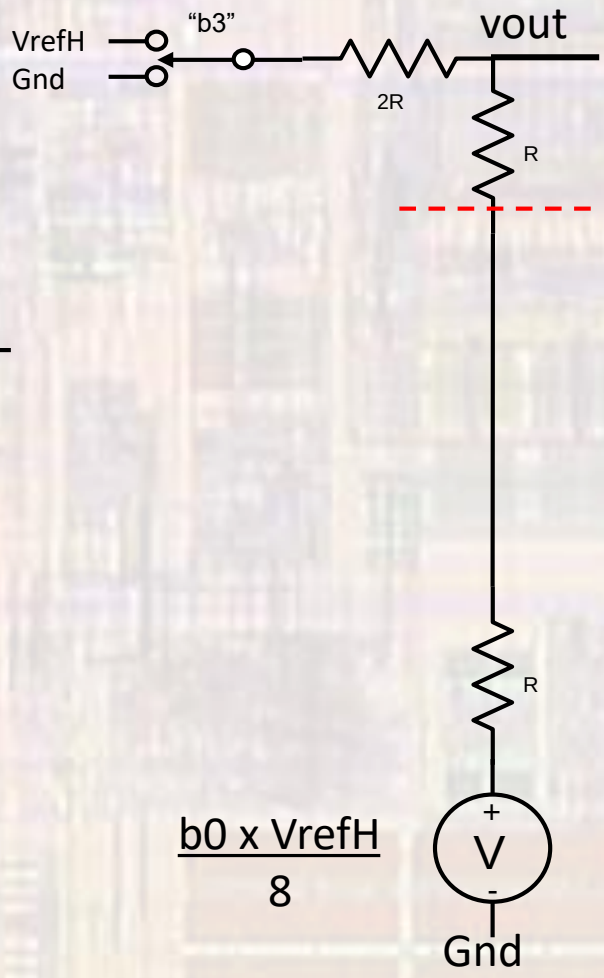


D/A

- D to A Converter

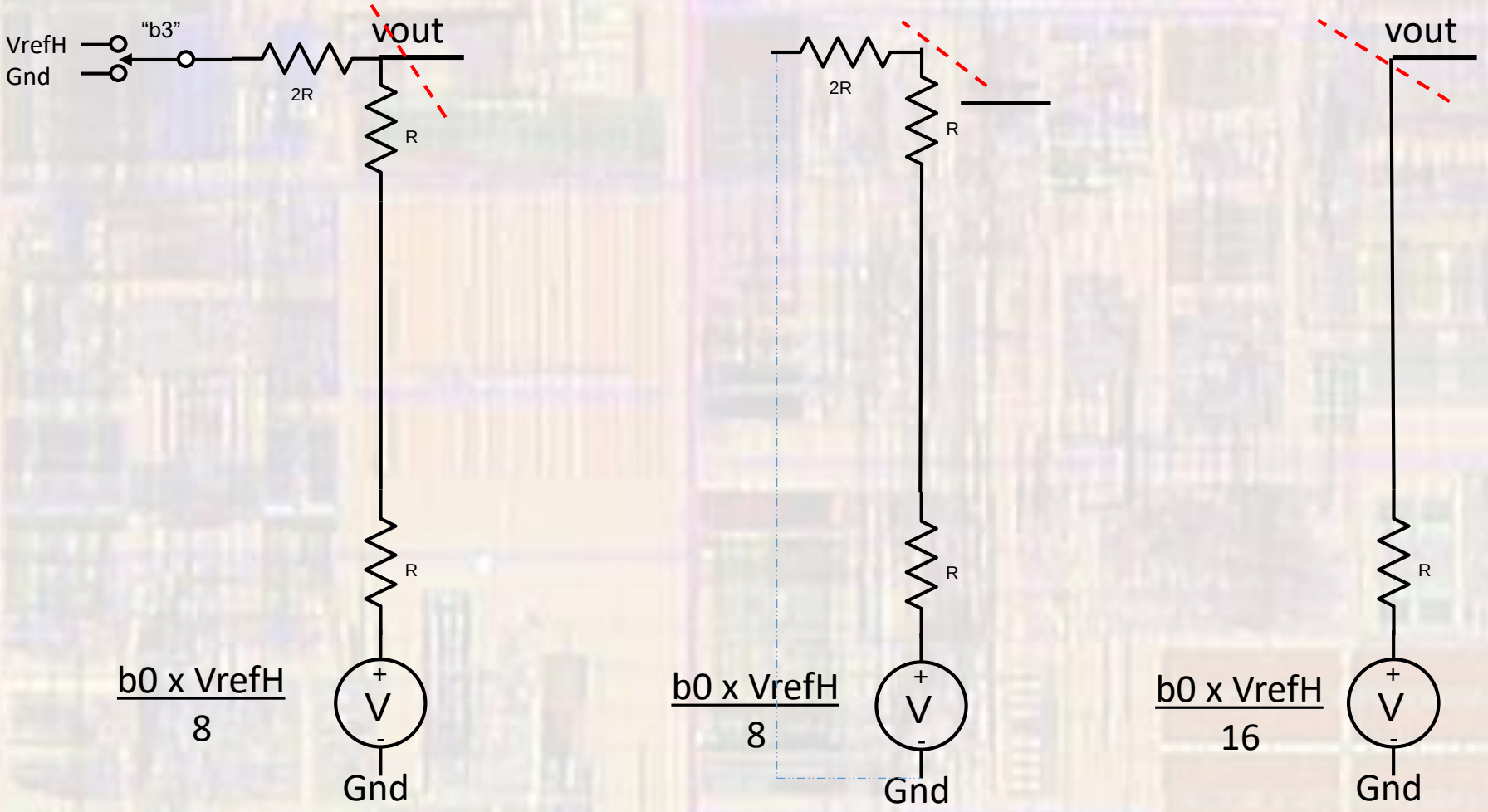






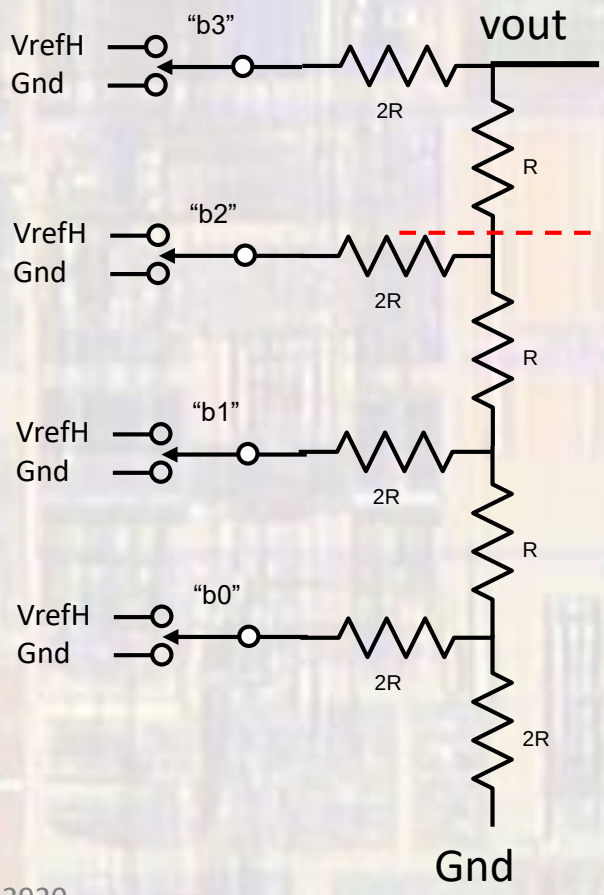
D/A

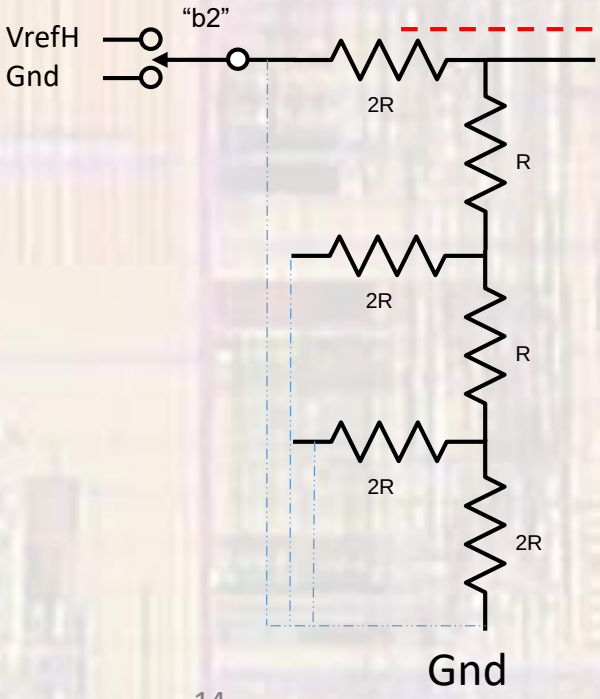
- D to A Converter



D/A

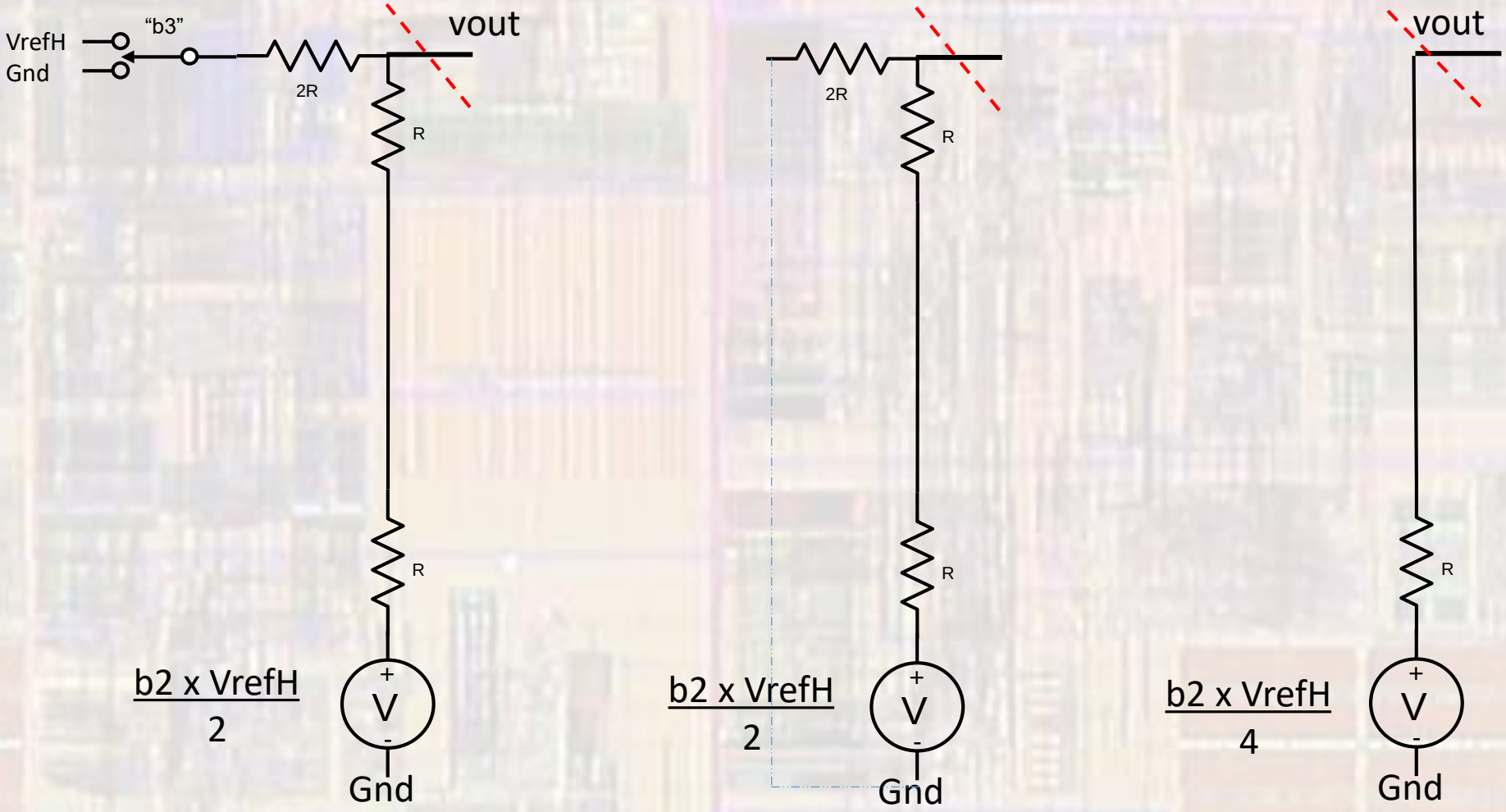
- D to A Converter
  - b2 analysis





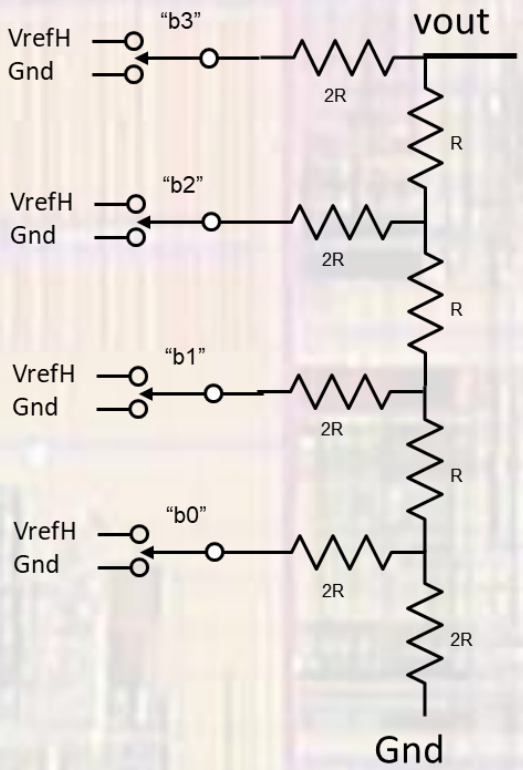
D/A

- D to A Converter



D/A

- D to A Converter
  - Vout = ((b0)/16 + (b1)/8 + (b2)/4 + (b3)/2) * VrefH



D/A

- Example

3.3V Vref
8 bit convertor

Code	Steps	Volts
0000 0000	0	0
0000 0001	1	0.013
0001 0000	16	0.206
0111 1111	127	1.637
1000 0000	128	1.650
1100 0000	192	2.475
1111 1111	255	3.287

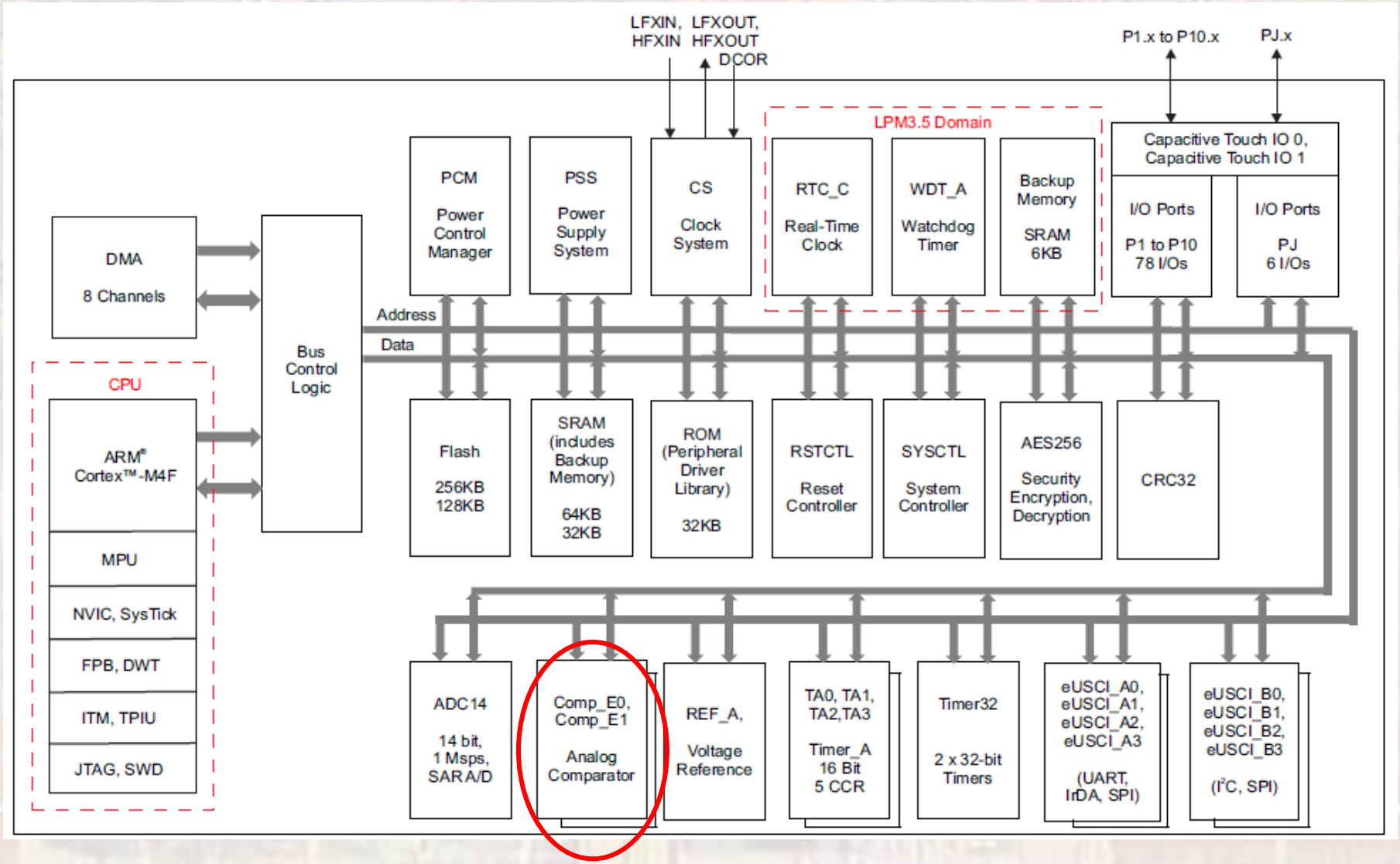
3.3v / 2^8 steps
= 12.89mv/step

Comparator

Comparator

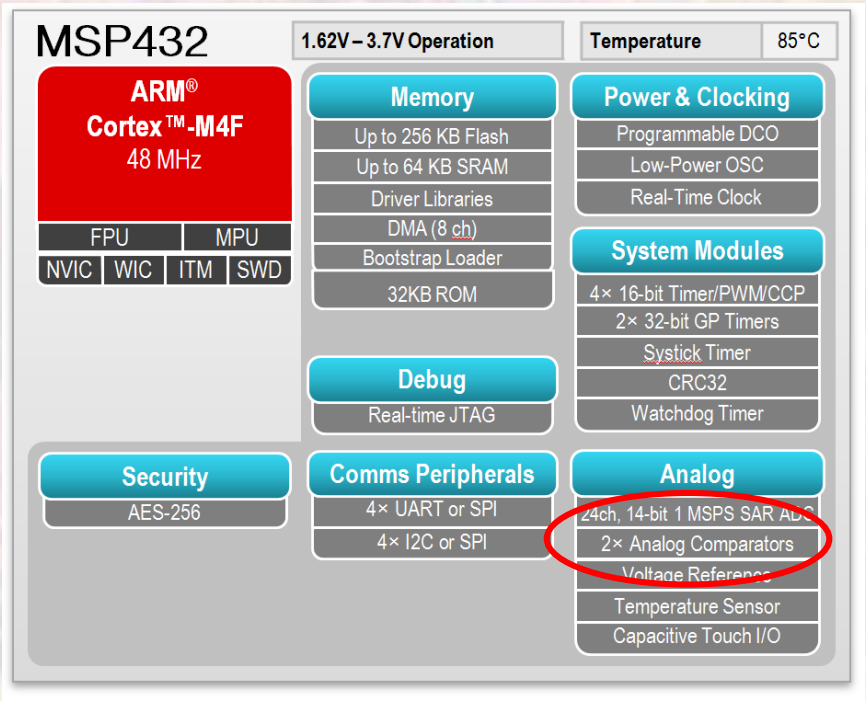
- Comparator
  - Compare the voltage of two inputs and generate
    - ‘0’ if minus input > plus input
    - ‘1’ if minus input < plus input
  - Open Loop OpAmp

MSP432P401R



Comparator

- MSP432 Comparators
  - Analog Comparator
    - 2 blocks
    - Input Multiplexing (8)
    - Hysteresis Generator
    - Programmable RC filter
    - Can Generate Interrupt



Comparator

- Comparator

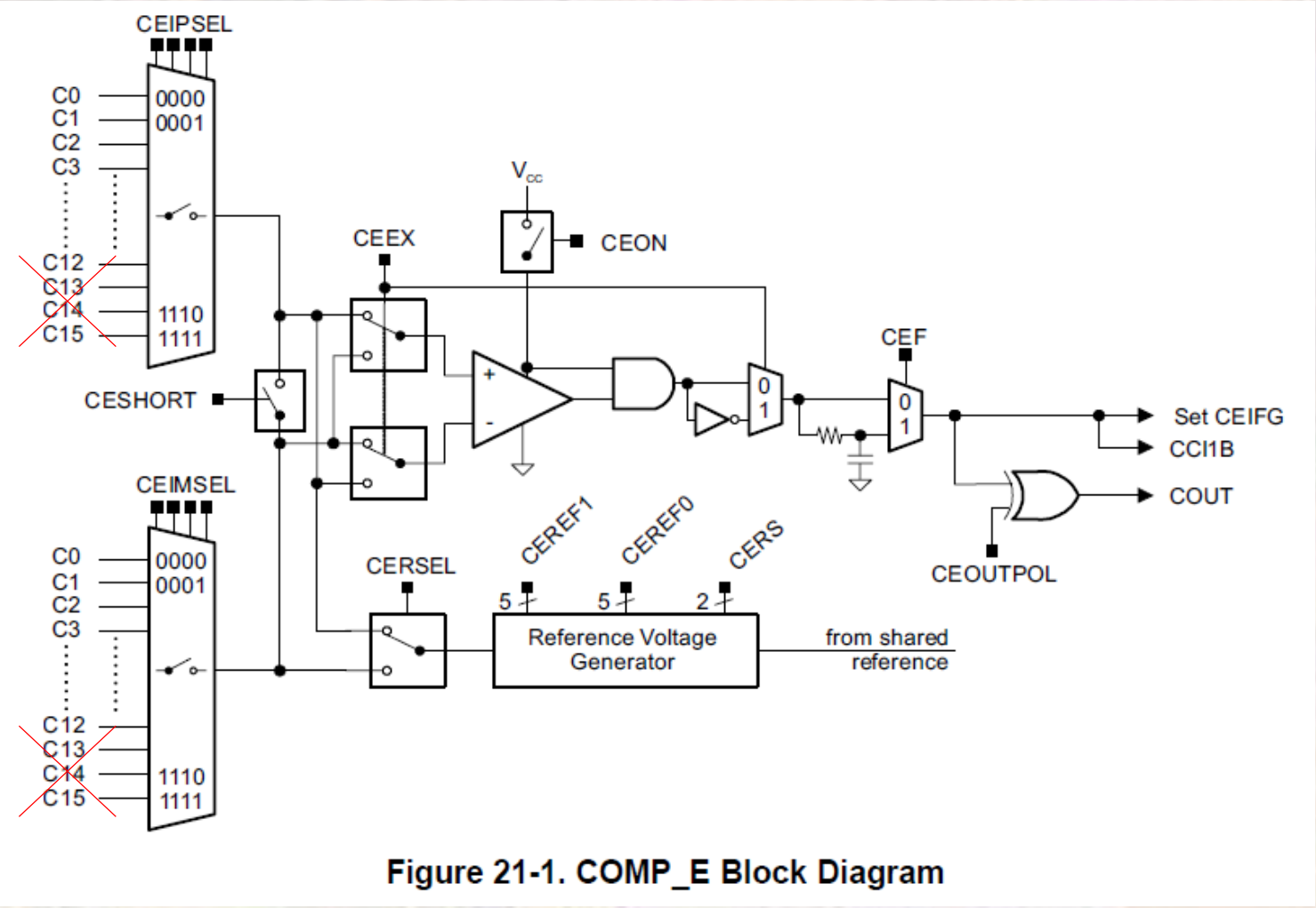


Figure 21-1. COMP_E Block Diagram

Comparator

- Comparator

COMP_E0->CTL0, …
COMP_E1->CTL0, …

Table 21-1. COMP_E Registers

Offset	Acronym	Register	Type	Access	Reset	Section
00h	CExCTL0	Comparator_E control 0	Read/write	Half-word	0000h	Section 21.3.1
02h	CExCTL1	Comparator_E control 1	Read/write	Half-word	0000h	Section 21.3.2
04h	CExCTL2	Comparator_E control 2	Read/write	Half-word	0000h	Section 21.3.3
06h	CExCTL3	Comparator_E control 3	Read/write	Half-word	0000h	Section 21.3.4
0Ch	CExINT	Comparator_E interrupt	Read/write	Half-word	0000h	Section 21.3.5
0Eh	CExIV	Comparator_E interrupt vector word	Read	Half-word	0000h	Section 21.3.6

NOTE: This is a 16-bit module and must be accessed ONLY through byte (8 bit) or half-word (16 bit) access. 32-bit read or write access to this module causes a bus error.

Comparator

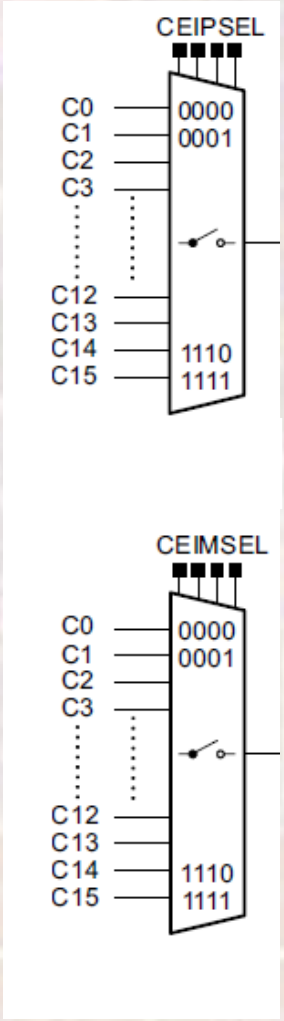
- Comparator

Figure 21-8. CExCTL0 Register

15	14	13	12	11	10	9	8
CEIMEN	Reserved			CEIMSEL			
rw-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
CEIPEN	Reserved			CEIPSEL			
rw-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0

Table 21-2. CExCTL0 Register Description

Bit	Field	Type	Reset	Description
15	CEIMEN	RW	0h	Channel input enable for the V- terminal of the comparator. 0b = Selected analog input channel for V- terminal is disabled. 1b = Selected analog input channel for V- terminal is enabled.
14-12	Reserved	R	0h	Reserved. Always reads as 0.
11-8	CEIMSEL	RW	0h	Channel input selected for the V- terminal of the comparator if CEIMEN is set to 1.
7	CEIPEN	RW	0h	Channel input enable for the V+ terminal of the comparator. 0b = Selected analog input channel for V+ terminal is disabled. 1b = Selected analog input channel for V+ terminal is enabled.
6-4	Reserved	R	0h	Reserved. Always reads as 0.
3-0	CEIPSEL	RW	0h	Channel input selected for the V+ terminal of the comparator if CEIPEN is set to 1.



Comparator

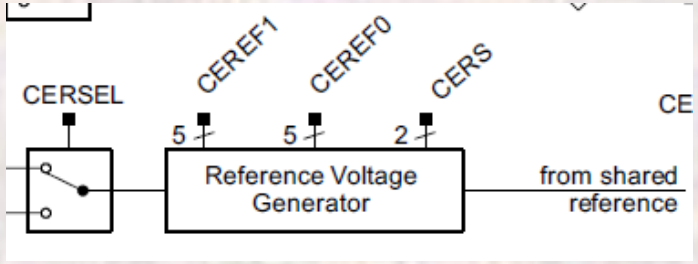
- Comparator

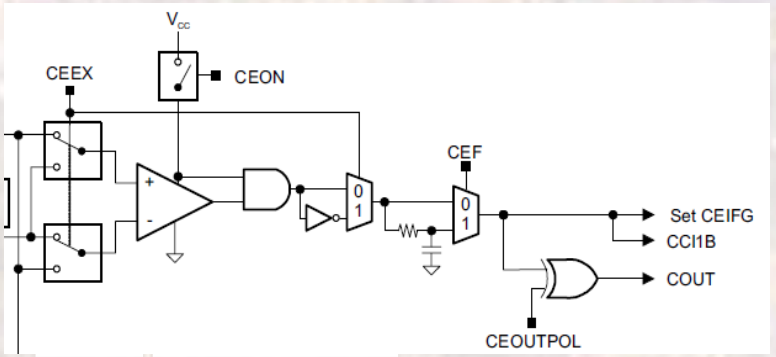
Figure 21-9. CExCTL1 Register

15	14	13	12	11	10	9	8
Reserved			CEMRVS	CEMRVL	CEON	CEPWRMD	
r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
CEFDLY		CEEX	CESHORT	CEIES	CEF	CEOUTPOL	CEOUT
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r-0

Table 21-3. CExCTL1 Register Description

Bit	Field	Type	Reset	Description
15-13	Reserved	R	0h	Reserved. Always reads as 0.
12	CEMRVS	RW	0h	This bit defines if the comparator output selects between VREF0 or VREF1 if CERS = 00, 01, or 10. 0b = Comparator output state selects between VREF0 or VREF1. 1b = CEMRVL selects between VREF0 or VREF1.
11	CEMRVL	RW	0h	This bit is valid if CEMRVS is set to 1. 0b = VREF0 is selected if CERS = 00, 01, or 10 1b = VREF1 is selected if CERS = 00, 01, or 10
10	CEON	RW	0h	On. This bit turns the comparator on. When the comparator is turned off the Comparator consumes no power. 0b = Off 1b = On
9-8	CEPWRMD	RW	0h	Power Mode 00b = High-speed mode 01b = Normal mode 10b = Ultra-low power mode 11b = Reserved
7-6	CEFDLY	RW	0h	Filter delay. The filter delay can be selected in four steps. See the device-specific data sheet for details. 00b = Typical filter delay of 500 ns 01b = Typical filter delay of 800 ns 10b = Typical filter delay of 1500 ns 11b = Typical filter delay of 3000 ns
5	CEEX	RW	0h	Exchange. This bit permutes the comparator 0 inputs and inverts the comparator 0 output.





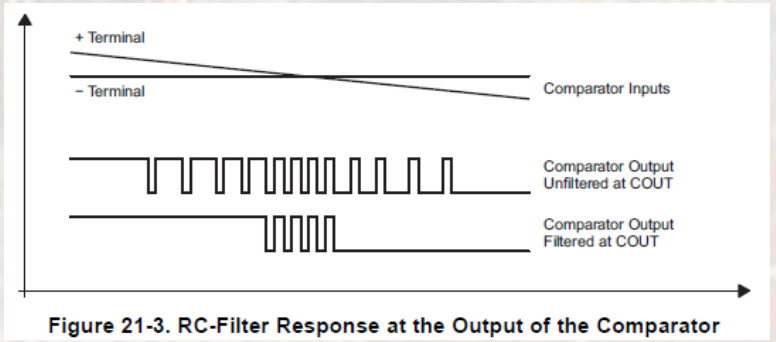


Figure 21-3. RC-Filter Response at the Output of the Comparator

Comparator

- Comparator

Figure 21-9. CExCTL1 Register

15	14	13	12	11	10	9	8
Reserved			CEMRVS	CEMRVL	CEON	CEPWRMD	
r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
CEFDLY		CEEX	CESHORT	CEIES	CEF	CEOUTPOL	CEOUT
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r-0

4	CESHORT	RW	0h	Input short. This bit shorts the + and – input terminals. 0b = Inputs not shorted 1b = Inputs shorted

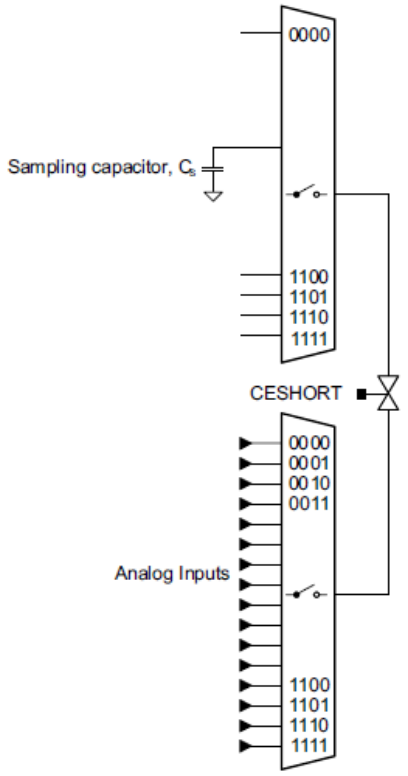


Figure 21-2. COMP_E Sample-And-Hold

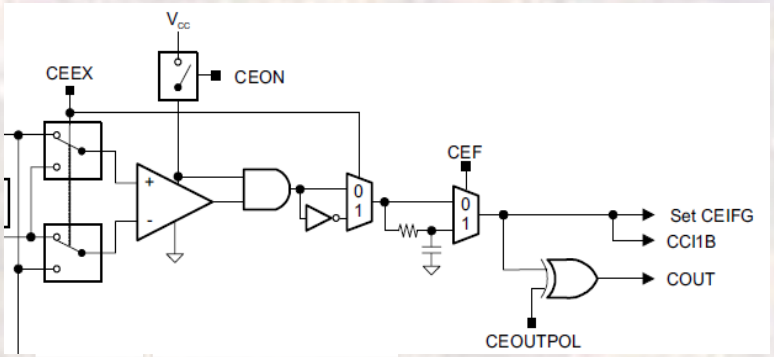
$\tau = R \times C$

8-10 τ recommended for sample time

Comparator

- Comparator

3	CEIES	RW	0h	Interrupt edge select for CEIIFG and CEIFG 0b = Rising edge for CEIFG, falling edge for CEIIFG 1b = Falling edge for CEIFG, rising edge for CEIIFG
2	CEF	RW	0h	Output filter. Available if CEPWRMD = 00, 01. 0b = Comparator output is not filtered 1b = Comparator output is filtered
1	CEOUTPOL	RW	0h	Output polarity. This bit defines the CEOUT polarity. 0b = Noninverted 1b = Inverted
0	CEOUT	RW	0h	Output value. This bit reflects the value of the Comparator output. Writing this bit has no effect on the comparator output.



Comparator

- Comparator

Figure 21-10. CExCTL2 Register

15	14	13	12	11	10	9	8
CEREFACC	CEREFL		CEREF1				
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
CERS		CERSEL	CEREF0				
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 21-4. CExCTL2 Register Description

Bit	Field	Type	Reset	Description
15	CEREFACC	RW	0h	Reference accuracy. A reference voltage is requested only if CEREFL > 0. 0b = Static mode 1b = Clocked (low power, low accuracy) mode
14-13	CEREFL	RW	0h	Reference voltage level 00b = Reference amplifier is disabled. No reference voltage is requested. 01b = 1.2 V is selected as shared reference voltage input 10b = 2.0 V is selected as shared reference voltage input 11b = 2.5 V is selected as shared reference voltage input
12-8	CEREF1	RW	0h	Reference resistor tap 1. This register defines the tap of the resistor string while CEOUT = 1.
7-6	CERS	RW	0h	Reference source. This bit defines if the reference voltage is derived from VCC or from the precise shared reference. 00b = No current is drawn by the reference circuitry. 01b = VCC applied to the resistor ladder 10b = Shared reference voltage applied to the resistor ladder. 11b = Shared reference voltage supplied to V(CREF). Resistor ladder is off.
5	CERSEL	RW	0h	Reference select. This bit selects which terminal the V_{CCREF} is applied to. 0b = When CEEX = 0, VREF is applied to the V+ terminal; When CEEX = 1, VREF is applied to the V- terminal 1b = When CEEX = 0, VREF is applied to the V- terminal; When CEEX = 1, VREF is applied to the V+ terminal
4-0	CEREF0	RW	0h	Reference resistor tap 0. This register defines the tap of the resistor string while CEOUT = 0.

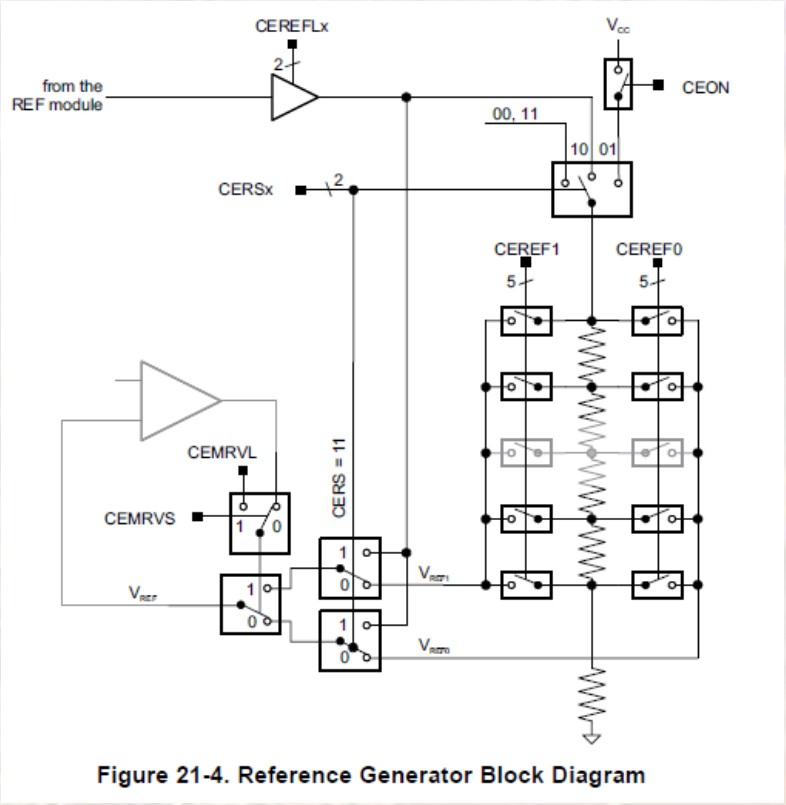


Figure 21-4. Reference Generator Block Diagram

Comparator

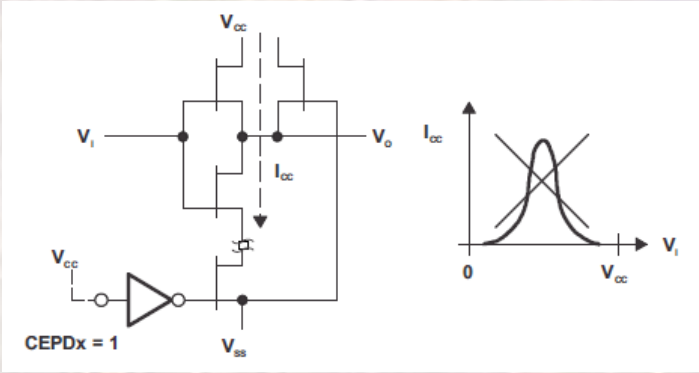
- Comparator

Figure 21-11. CExCTL3 Register

15	14	13	12	11	10	9	8
CEPD15	CEPD14	CEPD13	CEPD12	CEPD11	CEPD10	CEPD9	CEPD8
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
CEPD7	CEPD6	CEPD5	CEPD4	CEPD3	CEPD2	CEPD1	CEPD0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Table 21-5. CExCTL3 Register Description

Bit	Field	Type	Reset	Description
15	CEPD15	RW	0h	Port disable. These bits individually disable the input buffer for the pins of the port associated with Comparator_E. The bit CEPD15 disables the port of the comparator channel 15. 0b = The input buffer is enabled. 1b = The input buffer is disabled.
14	CEPD14	RW	0h	Port disable. These bits individually disable the input buffer for the pins of the port associated with Comparator_E. The bit CEPD14 disables the port of the comparator channel 14. 0b = The input buffer is enabled. 1b = The input buffer is disabled.
1	CEPD1	RW	0h	Port disable. These bits individually disable the input buffer for the pins of the port associated with Comparator_E. The bit CEPD1 disables the port of the comparator channel 1. 0b = The input buffer is enabled. 1b = The input buffer is disabled.
0	CEPD0	RW	0h	Port disable. These bits individually disable the input buffer for the pins of the port associated with Comparator_E. The bit CEPD0 disables the port of the comparator channel 0. 0b = The input buffer is enabled. 1b = The input buffer is disabled.



Comparator

- Comparator

Figure 21-12. CExINT Register

15	14	13	12	11	10	9	8
Reserved			CERDYIE	Reserved		CEIIE	CEIE
r-0	r-0	r-0	rw-0	r-0	r-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved			CERDYIFG	Reserved		CEIIFG	CEIFG
r-0	r-0	r-0	rw-0	r-0	r-0	rw-0	rw-0

Table 21-6. CExINT Register Description

Bit	Field	Type	Reset	Description
15-13	Reserved	R	0h	Reserved. Always reads as 0.
12	CERDYIE	RW	0h	Comparator ready interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
11-10	Reserved	R	0h	Reserved. Always reads as 0.
9	CEIIE	RW	0h	Comparator output interrupt enable inverted polarity 0b = Interrupt disabled 1b = Interrupt enabled
8	CEIE	RW	0h	Comparator output interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
7-5	Reserved	R	0h	Reserved. Always reads as 0.
4	CERDYIFG	RW	0h	Comparator ready interrupt flag. This bit is set if the Comparator reference sources are settled and the Comparator module is operational. This bit has to be cleared by software. 0b = No interrupt pending 1b = Interrupt pending
3-2	Reserved	R	0h	Reserved. Always reads as 0.
1	CEIIFG	RW	0h	Comparator output inverted interrupt flag. The bit CEIES defines the transition of the output setting this bit. 0b = No interrupt pending 1b = Interrupt pending
0	CEIFG	RW	0h	Comparator output interrupt flag. The bit CEIES defines the transition of the output setting this bit. 0b = No interrupt pending 1b = Interrupt pending

Comparator

- Comparator

Figure 21-13. CExIV Register

15	14	13	12	11	10	9	8
CEIV							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
CEIV							
r0	r0	r0	r0	r0	r-(0)	r-(0)	r0

Table 21-7. CExIV Register Description

Bit	Field	Type	Reset	Description
15-0	CEIV	R	0h	Comparator interrupt vector word register. The interrupt vector register reflects only interrupt flags whose interrupt enable bit are set. Reading the CEIV register clears the pending interrupt flag with the highest priority. 00h = No interrupt pending 02h = Interrupt Source: CEOUT interrupt; Interrupt Flag: CEIFG; Interrupt Priority: Highest 04h = Interrupt Source: CEOUT interrupt inverted polarity; Interrupt Flag: CEIIFG 06h = Reserved 08h = Reserved 0Ah = Interrupt Source: Comparator ready interrupt; Interrupt Flag: CERDYIFG; Interrupt Priority: Lowest

Comparator

- Comparator

Comparator Info Sheet

x= 0:1

COMP_Ex	->	CTL0	Control reg 0
		CTL1	Control reg 1
		CTL2	Control reg 2
		CTL3	Control reg 3
		INT	Interrupt Register
		IV	Interrupt Vector

COMP_E0_IRQHandler	INTISR[6]	COMP_E0	CERDYIFG, CEIIFG, CEIFG
COMP_E1_IRQHandler	INTISR[7]	COMP_E1	CERDYIFG, CEIIFG, CEIFG

INPUTS

PORT		DIR	PSEL[1:0]	PORT		DIR	PSEL[1:0]
P8.1	C 0 . 0		11	P6.7	C 1 . 0		11
P8.0	C 0 . 1		11	P6.6	C 1 . 1		11
P7.7	C 0 . 2		11	P6.5	C 1 . 2		11
P7.6	C 0 . 3		11	P6.4	C 1 . 3		11
P7.5	C 0 . 4		11	P6.3	C 1 . 4		11
P7.4	C 0 . 5		11	P6.2	C 1 . 5		11
P10.5	C 0 . 6		11	P5.7	C 1 . 6		11
P10.4	C 0 . 7		11	P5.6	C 1 . 7		11

OUTPUTS

PORT			DIR	PSEL[1:0]	PORT			DIR	PSEL[1:0]
P7.1	COUT	E0	1	01	P7.2	COUT	E1	1	01

Comparator

- Comparator Example

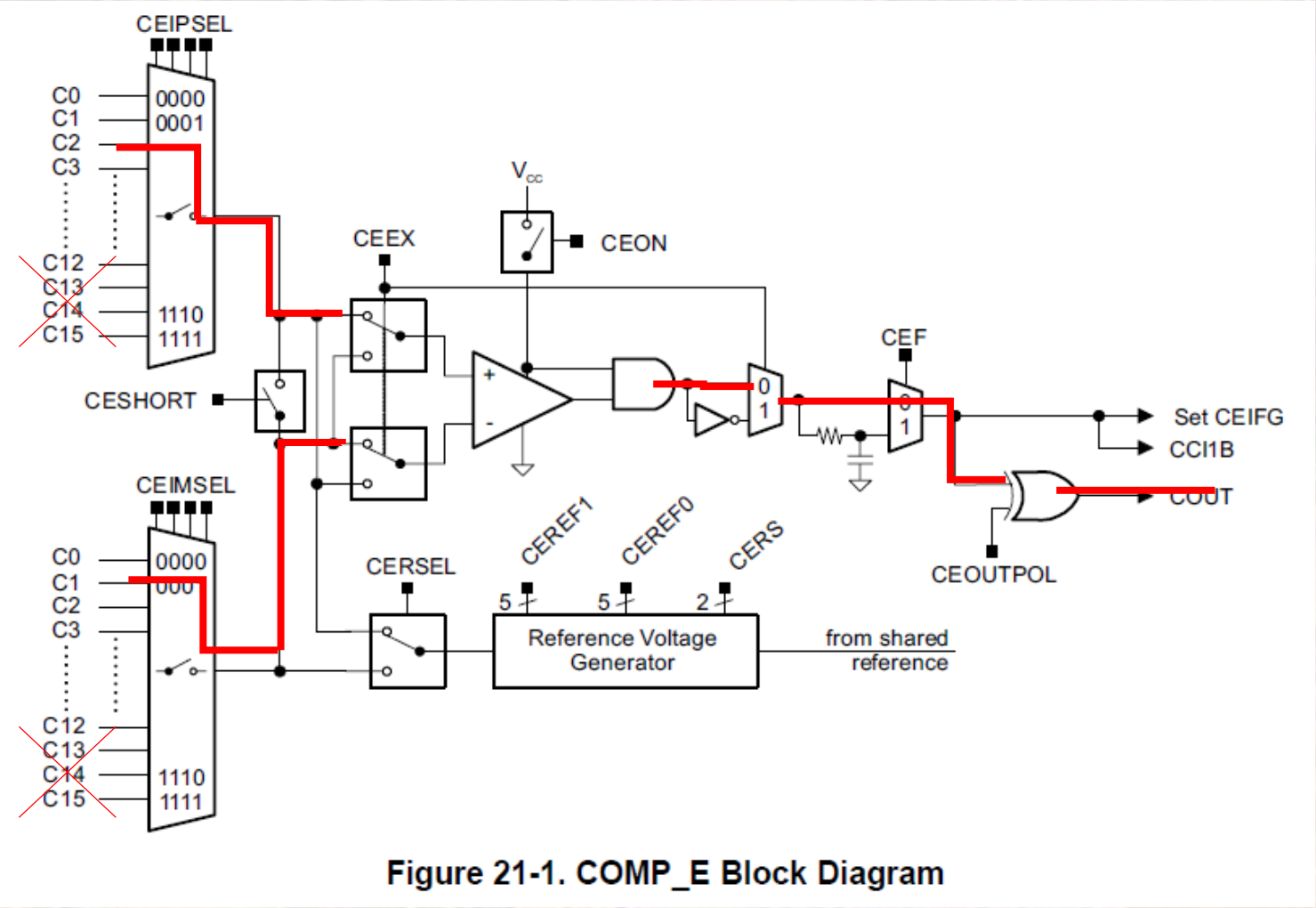


Figure 21-1. COMP_E Block Diagram

Comparator

- Comparator Example

```
/*
 * comparator_example.c
 *
 *  Created on: Jul 27, 2018
 *      Author: johnsontimoj
 */
//////////////////////////////////
//
// use port 7.7 as + input (C02)
// use port 8.0 as - input (C01)
//
// use port 7.1 as output
//
// use a potentiometer to sweep + input
// use a fixed divider for – input
//
// toggle an LED with the output
//
//////////////////////////////////

// includes
#include "msp.h"
#include <stdio.h>

// prototypes
void pin_setup(void);
void comp_setup(void);
```

```
int main(void){
    // setup routines
    pin_setup();
    comp_setup();

    while(1){
       ;    // do nothing in the main program
    } // end while

   return 0;
}

void pin_setup(void){
    // setup pins
    // Port 8 pins 0 and Port 7 pin 7 "11" select mode
    // Port 7 pin 1 is output, mode '01'
    P8->SEL0 |= 0x01;       // '11' pin functionality
    P8->SEL1 |= 0x01;
    P7->SEL0 |= 0x80;       // '11' pin functionality
    P7->SEL1 |= 0x80;

    P7->SEL0 |= 0x02;       // '01' pin functionality
    P7->SEL1 &= ~0x02;
    P7->DIR |= 0x02;

    return;
}
```

Comparator

- Comparator Example

```
void comp_setup(void){
    // setup Comparator E0

    // en - in   xxx   in1   en + in   xxx  in2
    //    1      000   0001      1     000  0010
    COMP_E0->CTL0 = 0x8182;

    // xxx x x on normal xx no_ex no_sht no_int no_filt no_inv x
    // 000 0 0 1    01   00   0     0      0      0       0    0
    COMP_E0->CTL1 = 0x0500;

    // no_ref
    // 0 00 00000 00 0 0000
    COMP_E0->CTL2 = 0x0000;

    // disable buffer inputs 0 and 2
    // 0000 0000 0000 0101
    COMP_E0->CTL3 = 0x0005;

    // no interrupts
    // xxx 0 xx 0 0 xxx x xx x x
    COMP_E0->INT = 0x0000;

    return;
}
```