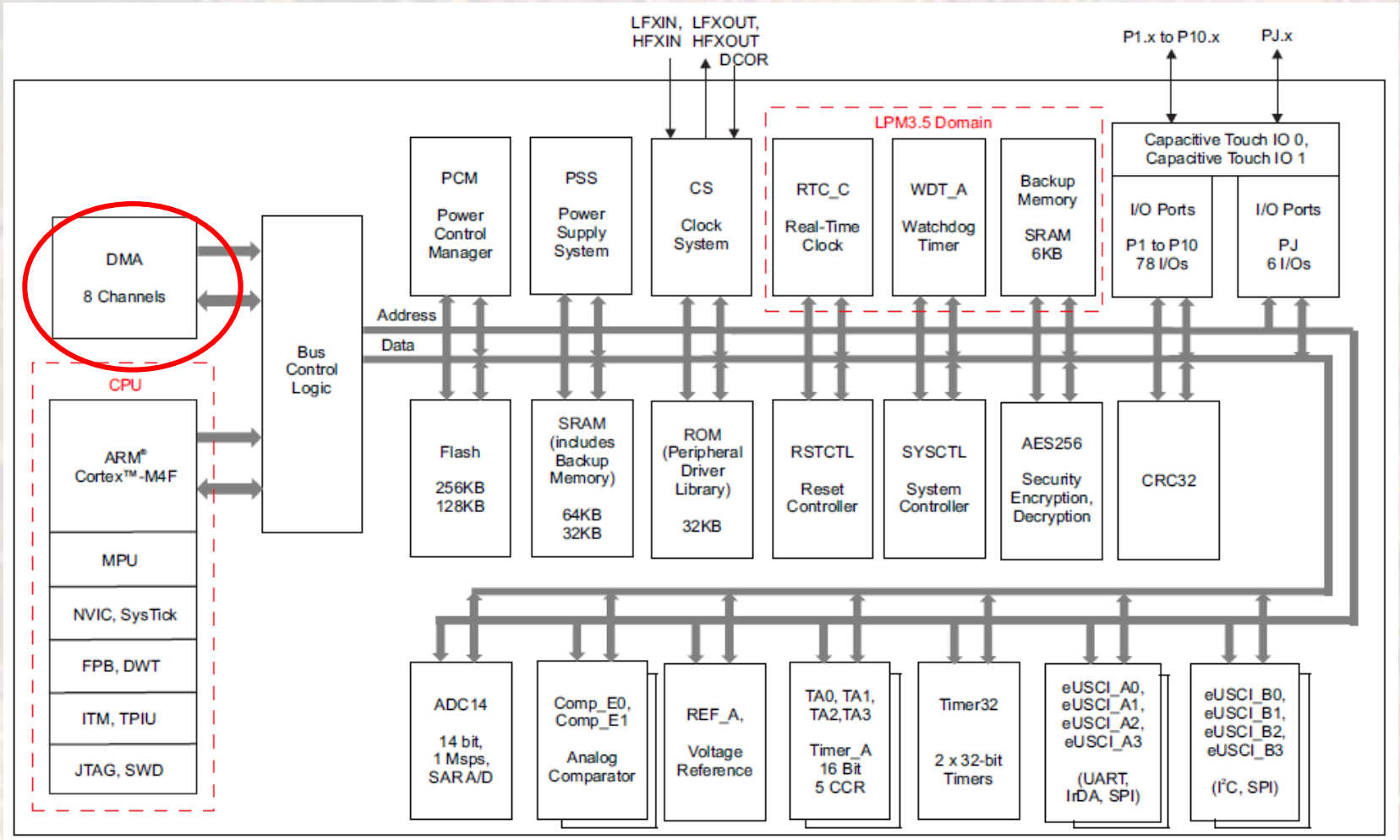
Direct Memory Access (DMA)

Last updated 6/17/19

DMA

- DMA Channels



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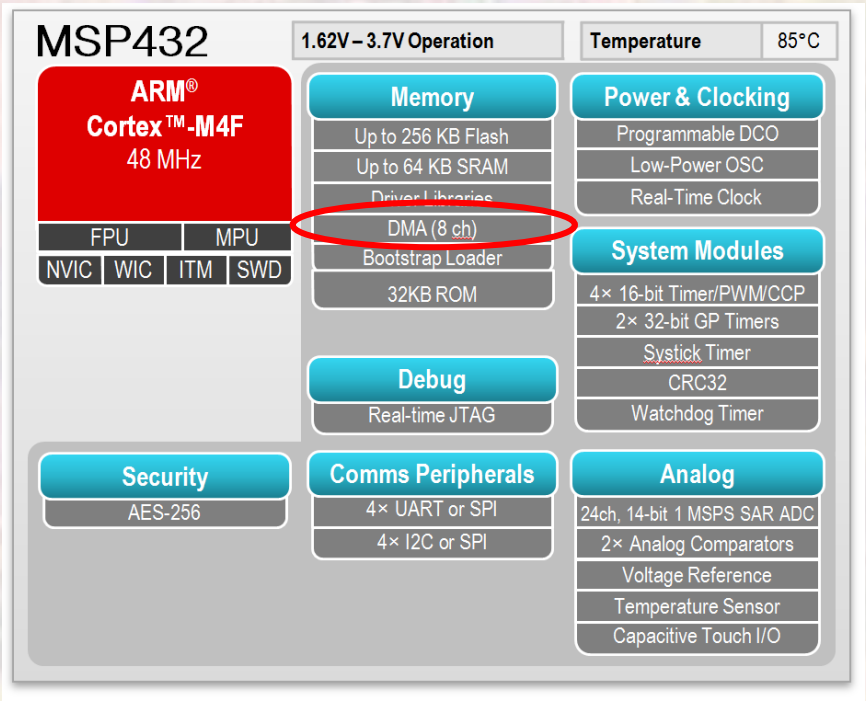
DMA

- MSP432 DMA
  - AMBA Compliant
  - 8 Channels
  - Up to 1024 transfers
  - Access to Memory and Peripherals



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DMA

- MSP432 DMA
  - Allows transfers from memory to
    - memory
    - peripherals
  - After setup, requires no CPU intervention
  - Can generate completion interrupts

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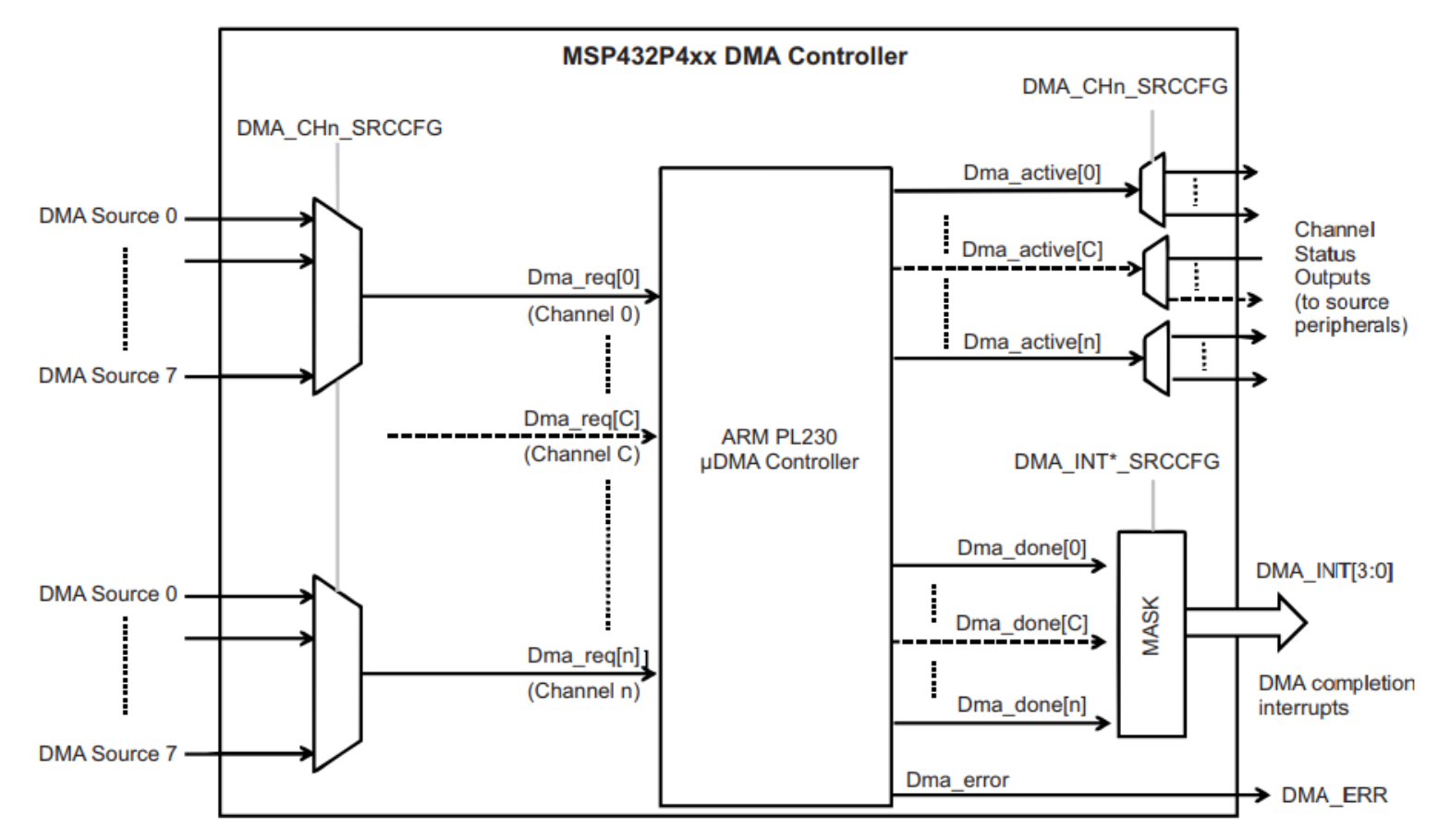
DMA

- MSP432 DMA



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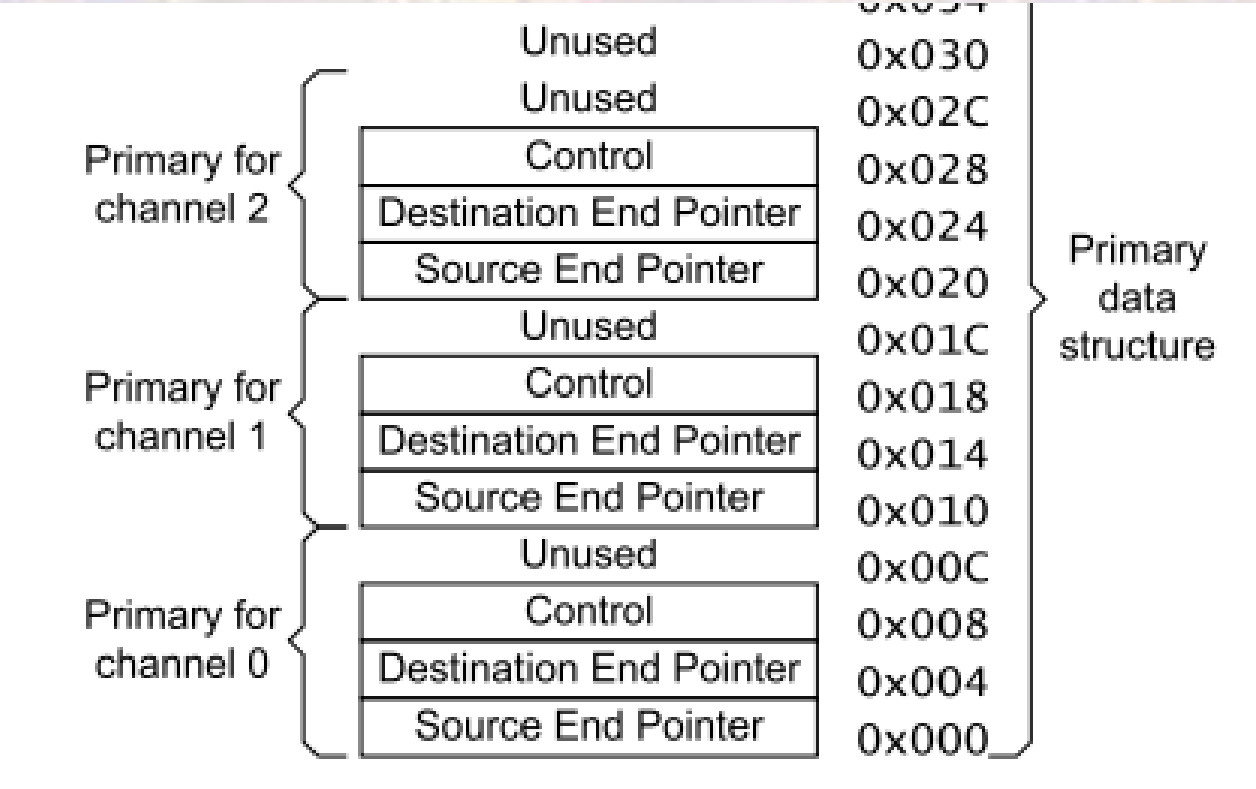
DMA

- MSP432 DMA



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DMA

- MSP432 DMA

Table 6-36. DMA Sources

	SRCCFG = 0	SRCCFG = 1	SRCCFG = 2	SRCCFG = 3	SRCCFG = 4	SRCCFG = 5	SRCCFG = 6	SRCCFG = 7
Channel 0	Reserved	eUSCI_A0 TX	eUSCI_B0 TX0	eUSCI_B3 TX1	eUSCI_B2 TX2	eUSCI_B1 TX3	TA0CCR0	AES256_Trigger0
Channel 1	Reserved	eUSCI_A0 RX	eUSCI_B0 RX0	eUSCI_B3 RX1	eUSCI_B2 RX2	eUSCI_B1 RX3	TA0CCR2	AES256_Trigger1
Channel 2	Reserved	eUSCI_A1 TX	eUSCI_B1 TX0	eUSCI_B0 TX1	eUSCI_B3 TX2	eUSCI_B2 TX3	TA1CCR0	AES256_Trigger2
Channel 3	Reserved	eUSCI_A1 RX	eUSCI_B1 RX0	eUSCI_B0 RX1	eUSCI_B3 RX2	eUSCI_B2 RX3	TA1CCR2	Reserved
Channel 4	Reserved	eUSCI_A2 TX	eUSCI_B2 TX0	eUSCI_B1 TX1	eUSCI_B0 TX2	eUSCI_B3 TX3	TA2CCR0	Reserved
Channel 5	Reserved	eUSCI_A2 RX	eUSCI_B2 RX0	eUSCI_B1 RX1	eUSCI_B0 RX2	eUSCI_B3 RX3	TA2CCR2	Reserved
Channel 6	Reserved	eUSCI_A3 TX	eUSCI_B3 TX0	eUSCI_B2 TX1	eUSCI_B1 TX2	eUSCI_B0 TX3	TA3CCR0	DMAE0 (External Pin)
Channel 7	Reserved	eUSCI_A3 RX	eUSCI_B3 RX0	eUSCI_B2 RX1	eUSCI_B1 RX2	eUSCI_B0 RX3	TA3CCR2	ADC14

22.3.16 DMA Operation

In devices with a DMA controller, the eUSCI module can trigger DMA transfers when the transmit buffer UCAxTXBUF is empty or when data was received in the UCAxRXBUF buffer. The DMA trigger signals correspond to the UCTXIFG transmit interrupt flag and the UCRXIFG receive interrupt flag, respectively. The interrupt functionality must be disabled for the selected DMA triggers with UCTXIE = 0 or UCRXIE = 0.

A DMA read access to UCAxRXBUF has the same effects as a CPU (software) read: all error flags (UCRXERR, UCFE, UCPE, UCOE, and UCBRK) are cleared after the read. Thus these errors might go unnoticed.

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DMA

- MSP43

Table 6-38. Memory Map Access Response

ADDRESS RANGE	DESCRIPTION	READ [1]	WRITE [1]	INSTRUCTION FETCH [1]
0x0000_0000–0x0003_FFFF	Flash Main Memory	OK	OK [2][3]	OK
0x0004_0000–0x001F_FFFF	Reserved	Error	Error	Error
0x0020_0000–0x0020_3FFF	Flash Information Memory	OK	OK [3]	OK
0x0020_4000–0x00FF_FFFF	Reserved	Error	Error	Error
0x0100_0000–0x0100_FFFF	SRAM	OK	OK	OK
0x0101_0000–0x01FF_FFFF	Reserved	Error	Error	Error
0x0200_0000–0x0200_03FF	ROM (Reserved)	Error	Error	Error
0x0200_0400–0x0200_7FFF	ROM	OK	Error	OK
0x0200_8000–0x1FFF_FFFF	Reserved	Error	Error	Error
0x2000_0000–0x2000_FFFF	SRAM	OK	OK	OK
0x2001_0000–0x21FF_FFFF	Reserved	Error	Error	Error
0x2200_0000–0x23FF_FFFF	SRAM bit-band alias	OK [4]	OK	Error
0x2400_0000–0x3FFF_FFFF	Reserved	Error	Error	Error
0x4000_0000–0x4001_FFFF	Peripheral	OK	OK	Error
0x4002_0000–0x41FF_FFFF	Reserved	Error	Error	Error
0x4200_0000–0x43FF_FFFF	Peripheral bit-band alias	OK [4]	OK	Error
0x4400_0000–0xDFFF_FFFF	Reserved	Error	Error	Error
0xE000_0000–0xE003_FFFF	Internal PPB [5]	OK	OK	Error
0xE004_0000–0xE004_0FFF	TPIU (External PPB)	OK	OK	Error
0xE004_1000–0xE004_1FFF	Reserved	Reserved	Reserved	Error
0xE004_2000–0xE004_23FF	Reset Controller (External PPB)	OK	OK	Error
0xE004_2400–0xE004_2FFF	Reserved	Reserved	Reserved	Error
0xE004_3000–0xE004_33FF	SYSCTL (External PPB)	OK	OK	Error
0xE004_3400–0xE004_3FFF	Reserved	Reserved	Reserved	Error
0xE004_4000–0xE004_43FF	SYSCTL (External PPB)	OK	OK	Error
0xE004_4400–0xE00F_EFFF	Reserved	Reserved	Reserved	Error
0xE00F_F000–0xE00F_FFFF	ROM Table (External PPB)	OK	OK	Error
0xE010_0000–0xFFFF_FFFF	Reserved	Error	Error	Error

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DMA

- MSP432 DMA

DMA_Control->

- ALTBASE : const volatile uint32_t
- ALTCLR : volatile uint32_t
- ALTSET : volatile uint32_t
- CFG : volatile uint32_t
- CTLBASE : volatile uint32_t
- ENACLR : volatile uint32_t
- ENASET : volatile uint32_t
- ERRCLR : volatile uint32_t
- PRIOCLR : volatile uint32_t
- PRIOSET : volatile uint32_t
- REQMASKCLR : volatile uint32_t
- REQMASKSET : volatile uint32_t
- RESERVED4 : uint32_t [3]
- STAT : const volatile uint32_t
- SWREQ : volatile uint32_t
- USEBURSTCLR : volatile uint32_t
- USEBURSTSET : volatile uint32_t
- WAITSTAT : const volatile uint32_t

DMA_Channel->

- CH_SRCCFG : volatile uint32_t [32]
- DEVICE_CFG : const volatile uint32_t
- INT0_CLRFLG : volatile uint32_t
- INT0_SRCFLG : const volatile uint32_t
- INT1_SRCCFG : volatile uint32_t
- INT2_SRCCFG : volatile uint32_t
- INT3_SRCCFG : volatile uint32_t
- RESERVED0 : uint32_t [2]
- RESERVED1 : uint32_t [28]
- RESERVED2 : uint32_t
- SW_CHTRIG : volatile uint32_t

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