EE 2920

Dr. Johnson

Final

90 min

Closed book/notes

Calculator allowed

Notes

1) SPI	10pts
2) TWI	10pts
3) UART	10pts
4) TIMER_A	15pts
5) TIMER_A	10pts
6) SPEC	15pts
7) Rectifier	15pts
8) Thermal	15pts
9) Schematics	10pts
10) ADC	15pts

Table 17-4. TAxCTL Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	RW	0h	Reserved
9-8	TASSEL	RW	0h	Timer_A clock source select 00b = TAxCLK 01b = ACLK 10b = SMCLK 11b = INCLK
7-6	ID	RW	0h	Input divider. These bits along with the TAIDEX bits select the divider for the input clock. 00b = /1 01b = /2 10b = /4 11b = /8
5-4	MC	RW	0h	Mode control. Setting MCx = 00h when Timer_A is not in use conserves power. 00b = Stop mode: Timer is halted 01b = Up mode: Timer counts up to TAxCCR0 10b = Continuous mode: Timer counts up to 0FFFFh 11b = Up/down mode: Timer counts up to TAxCCR0 then down to 0000h
3	Reserved	RW	0h	Reserved
2	TACLR	RW	0h	Timer_A clear. Setting this bit resets TAxR, the timer clock divider logic, and the count direction. The TACLR bit is automatically reset and is always read as zero.
1	TAIE	RW	0h	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
0	TAIFG	RW	0h	Timer_A interrupt flag 0b = No interrupt pending 1b = Interrupt pending

Table 17-9. TAxEX0 Register Description

Bit	Field	Type	Reset	Description
15-3	Reserved	R	0h	Reserved. Reads as 0.
2-0	TAIDEX	RW	0h	Input divider expansion. These bits along with the ID bits select the divider for the input clock. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b = Divide by 5 101b = Divide by 6 110b = Divide by 7 111b = Divide by 8

Table 17-7. TAxCCR0 to TAxCCR6 Register Description

Bit	Field	Type	Reset	Description
15-0	TAxCCR0	RW	0h	Compare mode: TAxCCRn holds the data for the comparison to the timer value in the Timer_A Register, TAxR. Capture mode: The Timer_A Register, TAxR, is copied into the TAxCCRn register when a capture is performed.

Table 17-5. TAxR Register Description

Bit	Field	Type	Reset	Description
15-0	TAxR	RW	0h	Timer_A register. The TAxR register is the count of Timer_A.

Table 17-6. TAxCCTL0 to TAxCCTL6 Register Description

Bit	Field	Type	Reset	Description
15-14	CM	RW	0h	Capture mode 00b = No capture 01b = Capture on rising edge 10b = Capture on falling edge 11b = Capture on both rising and falling edges
13-12	CCIS	RW	0h	Capture/compare input select. These bits select the TAxCCR0 input signal. See the device-specific data sheet for specific signal connections. 00b = CCIxA 01b = CCIxB 10b = GND 11b = VCC
11	SCS	RW	0h	Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock. 0b = Asynchronous capture 1b = Synchronous capture
10	SCCI	RW	0h	Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit.
9	Reserved	R	0h	Reserved. Reads as 0.
8	CAP	RW	0h	Capture mode 0b = Compare mode 1b = Capture mode
7-5	OUTMOD	RW	0h	Output mode. Modes 2, 3, 6, and 7 are not useful for TAxCCR0 because EQUx = EQU0. 000b = OUT bit value 001b = Set 010b = Toggle/reset 011b = Set/reset 100b = Toggle 101b = Reset 110b = Toggle/set 111b = Reset/set
4	CCIE	RW	0h	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0b = Interrupt disabled 1b = Interrupt enabled
3	CCI	R	0h	Capture/compare input. The selected input signal can be read by this bit.
2	OUT	RW	0h	Output. For output mode 0, this bit directly controls the state of the output. 0b = Output low 1b = Output high
1	COV	RW	0h	Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software. 0b = No capture overflow occurred 1b = Capture overflow occurred
0	CCIFG	RW	0h	Capture/compare interrupt flag 0b = No interrupt pending 1b = Interrupt pending

$$Vripple < 2 \times Vpk \times (1 - e^{-T/4\tau})$$

Table 20-4. ADC14CTL0 Register Description

Bit	Field	Type	Reset	Description
31-30	ADC14PDIV	RW	0h	ADC14 predivider. This bit predivides the selected ADC14 clock source. Can be modified only when ADC14ENC = 0. 00b = Predivide by 1 01b = Predivide by 4 10b = Predivide by 32 11b = Predivide by 64
29-27	ADC14SHSx	RW	0h	ADC14 sample-and-hold source select. Can be modified only when ADC14ENC = 0. 000b = ADC14SC bit 001b = See device-specific data sheet for source 010b = See device-specific data sheet for source 011b = See device-specific data sheet for source 100b = See device-specific data sheet for source 101b = See device-specific data sheet for source 110b = See device-specific data sheet for source 111b = See device-specific data sheet for source
26	ADC14SHP	RW	0h	ADC14 sample-and-hold pulse-mode select. This bit selects the source of the sampling signal (SAMPCON) to be either the output of the sampling timer or the sample-input signal directly. Can be modified only when ADC14ENC = 0. 0b = SAMPCON signal is sourced from the sample-input signal. 1b = SAMPCON signal is sourced from the sampling timer.
25	ADC14ISSH	RW	0h	ADC14 invert signal sample-and-hold. Can be modified only when ADC14ENC = 0. 0b = The sample-input signal is not inverted. 1b = The sample-input signal is inverted. Setting ADC14ISSH = 1 and triggering a conversion using ADC14SC is not recommended. ADC14SC bit gets reset to 0 automatically at the end of conversion and if ADC14ISSH = 1, the 1->0 transition on ADC14SC triggers another conversion.
24-22	ADC14DIVx	RW	0h	ADC14 clock divider. Can be modified only when ADC14ENC = 0. 000b = /1 001b = /2 010b = /3 011b = /4 100b = /5 101b = /6 110b = /7 111b = /8
21-19	ADC14SSELx	RW	0h	ADC14 clock source select. Can be modified only when ADC14ENC = 0. 000b = MODCLK 001b = SYSCLK 010b = ACLK 011b = MCLK 100b = SMCLK 101b = HSMCLK 110b = Reserved 111b = Reserved
18-17	ADC14CONSEQx	RW	0h	ADC14 conversion sequence mode select Can be modified only when ADC14ENC = 0. 00b = Single-channel, single-conversion 01b = Sequence-of-channels 10b = Repeat-single-channel 11b = Repeat-sequence-of-channels
16	ADC14BUSY	R	0h	ADC14 busy. This bit indicates an active sample or conversion operation. 0b = No operation is active. 1b = A sequence, sample, or conversion is active.
15-12	ADC14SHT1x	RW	0h	ADC14 sample-and-hold time. These bits define the number of ADC14CLK cycles in the sampling period for registers ADC14MEM8 to ADC14MEM23. Can be modified only when ADC14ENC = 0. 0000b = 4 0001b = 8 0010b = 16 0011b = 32 0100b = 64 0101b = 96 0110b = 128 0111b = 192 1000b to 1111b = Reserved
11-8	ADC14SHT0x	RW	0h	ADC14 sample-and-hold time. These bits define the number of ADC14CLK cycles in the sampling period for registers ADC14MEM0 to ADC14MEM7 and ADC14MEM24 to ADC14MEM31. Can be modified only when ADC14ENC = 0. 0000b = 4 0001b = 8 0010b = 16 0011b = 32 0100b = 64 0101b = 96 0110b = 128 0111b = 192 1000b to 1111b = Reserved
7	ADC14MSC	RW	0h	ADC14 multiple sample and conversion. Valid only for sequence or repeated modes. 0b = The sampling timer requires a rising edge of the SHI signal to trigger each sample-and-convert. 1b = The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed.
6-5	Reserved	R	0h	Reserved. Always reads as 0.
4	ADC14ON	RW	0h	ADC14 on 0b = ADC14 off 1b = ADC14 on. ADC core is ready to power up when a valid conversion is triggered.
3-2	Reserved	R	0h	Reserved. Always reads as 0.
1	ADC14ENC	RW	0h	ADC14 enable conversion 0b = ADC14 disabled 1b = ADC14 enabled ADC14ENC low pulse width must be at-least 3 ADC14CLK cycles.
0	ADC14SC	RW	0h	ADC14 start conversion. Software-controlled sample-and-conversion start. ADC14SC and ADC14ENC may be set together with one instruction. ADC14SC is reset automatically. 0b = No sample-and-conversion-start 1b = Start sample-and-conversion

ADC→CTL1

23	ADC14TCMAP	RW	0h	Controls temperature sensor ADC input channel selection 0b = ADC internal temperature sensor channel is not selected for ADC 1b = ADC internal temperature sensor channel is selected for ADC input channel MAX – 1
22	ADC14BATMAP	RW	0h	Controls 1/2 AVCC ADC input channel selection 0b = ADC internal 1/2 x AVCC channel is not selected for ADC 1b = ADC internal 1/2 x AVCC channel is selected for ADC input channel MAX
21	Reserved	R	0h	Reserved. Always reads as 0.
20-16	ADC14CSTARTADDx	RW	0h	ADC14 conversion start address. These bits select which ADC14 conversion memory register is used for a single conversion or for the first conversion in a sequence. The value of CSTARTADDx is 0h to 1Fh, corresponding to ADC14MEM0 to ADC14MEM31
15-6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	ADC14RES	RW	3h	ADC14 resolution. This bit defines the conversion result resolution. Can be modified only when ADC14ENC = 0. 00b = 8 bit (9 clock cycle conversion time) 01b = 10 bit (11 clock cycle conversion time) 10b = 12 bit (14 clock cycle conversion time) 11b = 14 bit (16 clock cycle conversion time)
3	ADC14DF	RW	0h	ADC14 data read-back format. Data is always stored in the binary unsigned format. 0b = Binary unsigned. Theoretically, for ADC14DIF = 0 and 14-bit mode, the analog input voltage - V(REF) results in 0000h, and the analog input voltage + V(REF) results in 3FFFh. 1b = Signed binary (2s complement), left aligned. Theoretically, for ADC14DIF = 0 and 14-bit mode, the analog input voltage - V(REF) results in 8000h, and the analog input voltage + V(REF) results in 7FFCh.
2	ADC14REFBURST	RW	0h	ADC reference buffer burst. Can be modified only when ADC14ENC = 0. 0b = ADC reference buffer on continuously 1b = ADC reference buffer on only during sample-and-conversion
1-0	ADC14PWRMD	RW	0h	ADC power modes. Can be modified only when ADC14ENC = 0. 00b = Regular-power mode for use with any resolution setting. Sample rate can be up to 1 Msps. 01b = Reserved 10b = Low-power mode for 12-bit, 10-bit, and 8-bit resolution settings. Sample rate must not exceed 200 ksps. 11b = Reserved

Table 20-10. ADC14MCTL0 to ADC14MCTL31 Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always reads as 0.
15	ADC14WINCTH	RW	0h	Window comparator threshold register selection Can be modified only when ADC14ENC = 0. 0b = Use window comparator thresholds 0, ADC14LO0 and ADC14HI0 1b = Use window comparator thresholds 1, ADC14LO1 and ADC14HI1
14	ADC14WINC	RW	0h	Comparator window enable Can be modified only when ADC14ENC = 0. 0b = Comparator window disabled 1b = Comparator window enabled
13	ADC14DIF	RW	0h	Differential mode. Can be modified only when ADC14ENC = 0. 0b = Single-ended mode enabled 1b = Differential mode enabled
12	Reserved	R	0h	Reserved. Always reads as 0.
11-8	ADC14VRSEL	RW	0h	Selects combinations of V(R+) and V(R-) sources as well as the buffer selection and buffer on or off. When REFOUT = 1, VeREF+ buffered configuration is not available. Can be modified only when ADC14ENC = 0. 0000b = V(R+) = AVCC, V(R-) = AVSS 0001b = V(R+) = VREF buffered, V(R-) = AVSS 0010b to 1101b = Reserved 1110b = V(R+) = VeREF+, V(R-) = VeREF- 1111b = V(R+) = VeREF+ buffered, V(R-) = VeREF- It is recommended to connect VeREF- to on-board ground when VeREF- is selected for V(R-).
7	ADC14EOS	RW	0h	End of sequence. Indicates the last conversion in a sequence. Can be modified only when ADC14ENC = 0. 0b = Not end of sequence 1b = End of sequence
6-5	Reserved	R	0h	Reserved. Always reads as 0.
4-0	ADC14INCHx	RW	0h	Input channel select. If even channels are set as differential then odd channel configuration is ignored. Can be modified only when ADC14ENC = 0. 00000b = If ADC14DIF = 0: A0; If ADC14DIF = 1: Ain+ = A0, Ain- = A1 00001b = If ADC14DIF = 0: A1; If ADC14DIF = 1: Ain+ = A0, Ain- = A1 00010b = If ADC14DIF = 0: A2; If ADC14DIF = 1: Ain+ = A2, Ain- = A3 00011b = If ADC14DIF = 0: A3; If ADC14DIF = 1: Ain+ = A2, Ain- = A3 ■ ■ ■ 10100b = If ADC14DIF = 0: A20; If ADC14DIF = 1: Ain+ = A20, Ain- = A21 10101b = If ADC14DIF = 0: A21; If ADC14DIF = 1: Ain+ = A20, Ain- = A21 10110b = If ADC14DIF = 0: A22; If ADC14DIF = 1: Ain+ = A22, Ain- = A23 10111b = If ADC14DIF = 0: A23; If ADC14DIF = 1: Ain+ = A22, Ain- = A23