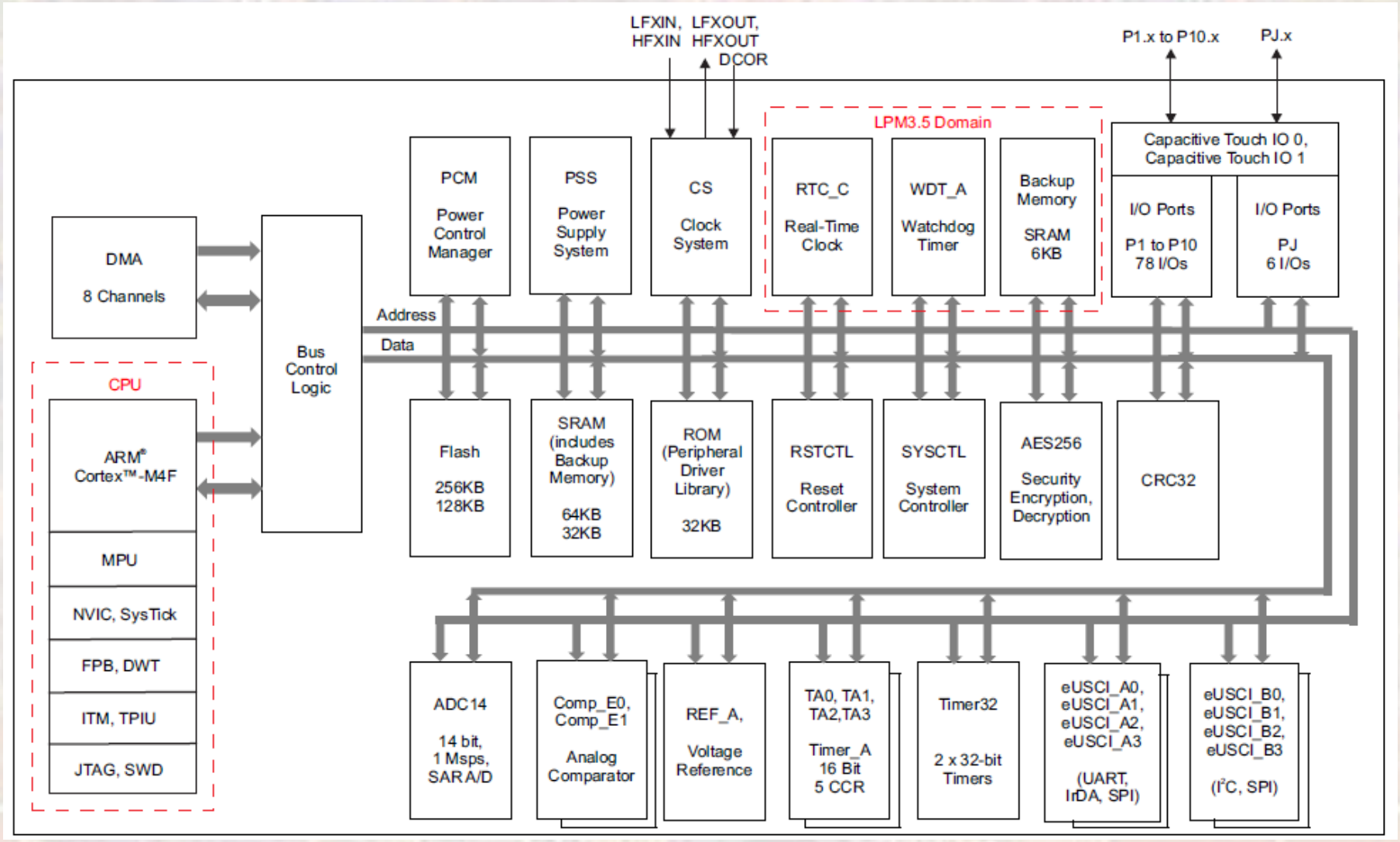
MSP432

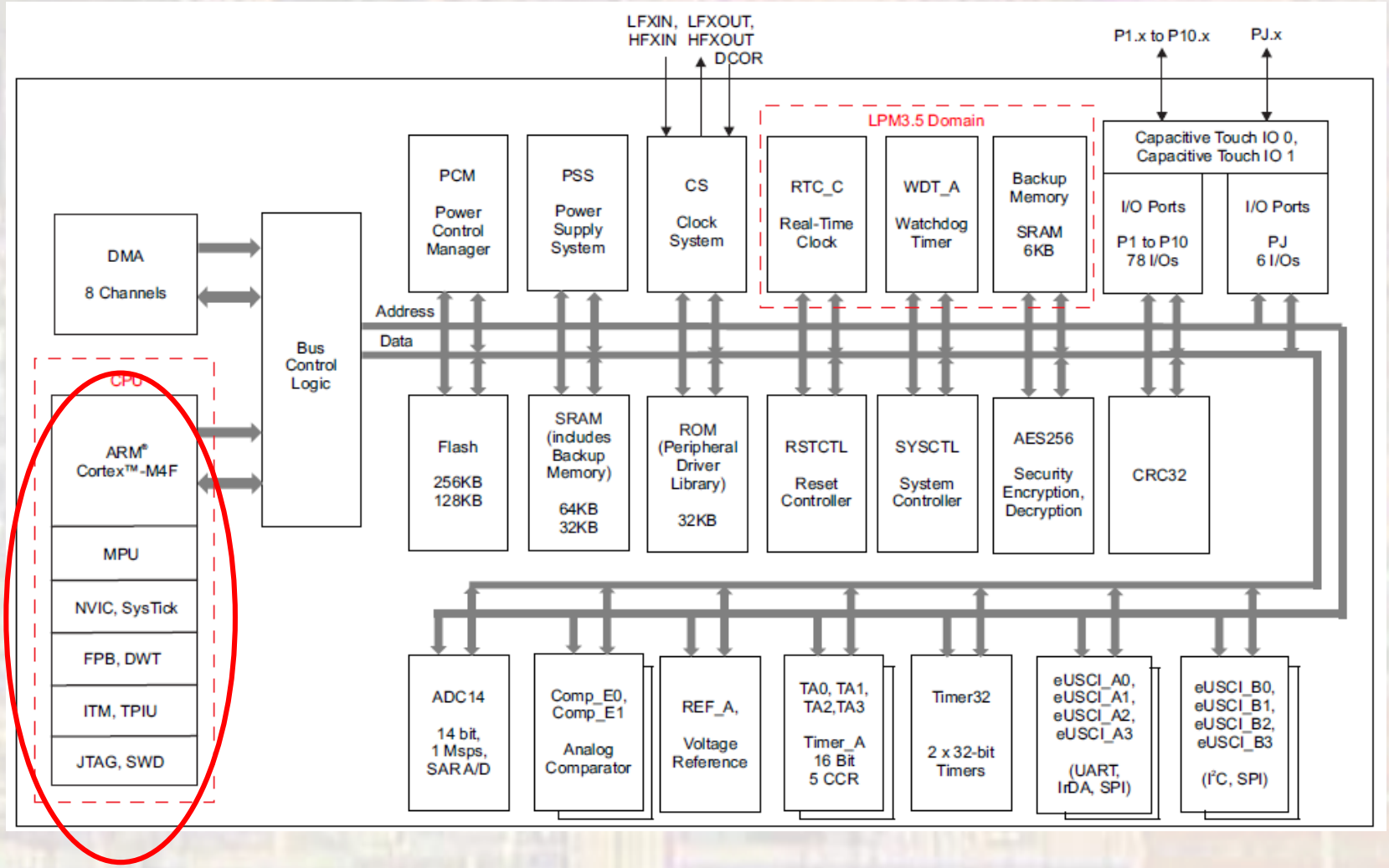
Last updated 5/21/19

MSP432P401R



MSP432P401R

- ARM M4 Core



ARM M4

- Functional Description
  - ARMv7-M 32 Bit Harvard Architecture Processor
  - Support for Thumb instructions
  - Multiple high-performance busses
  - Memory Protection Unit (MPU)
  - Atomic bit manipulation (bit-banding)
  - IEEE 754 Floating Point Unit (FPU)
  - 16 bit SIMD vector processing unit
  - Advanced debug support

ARM M4

- CPU Block Diagram

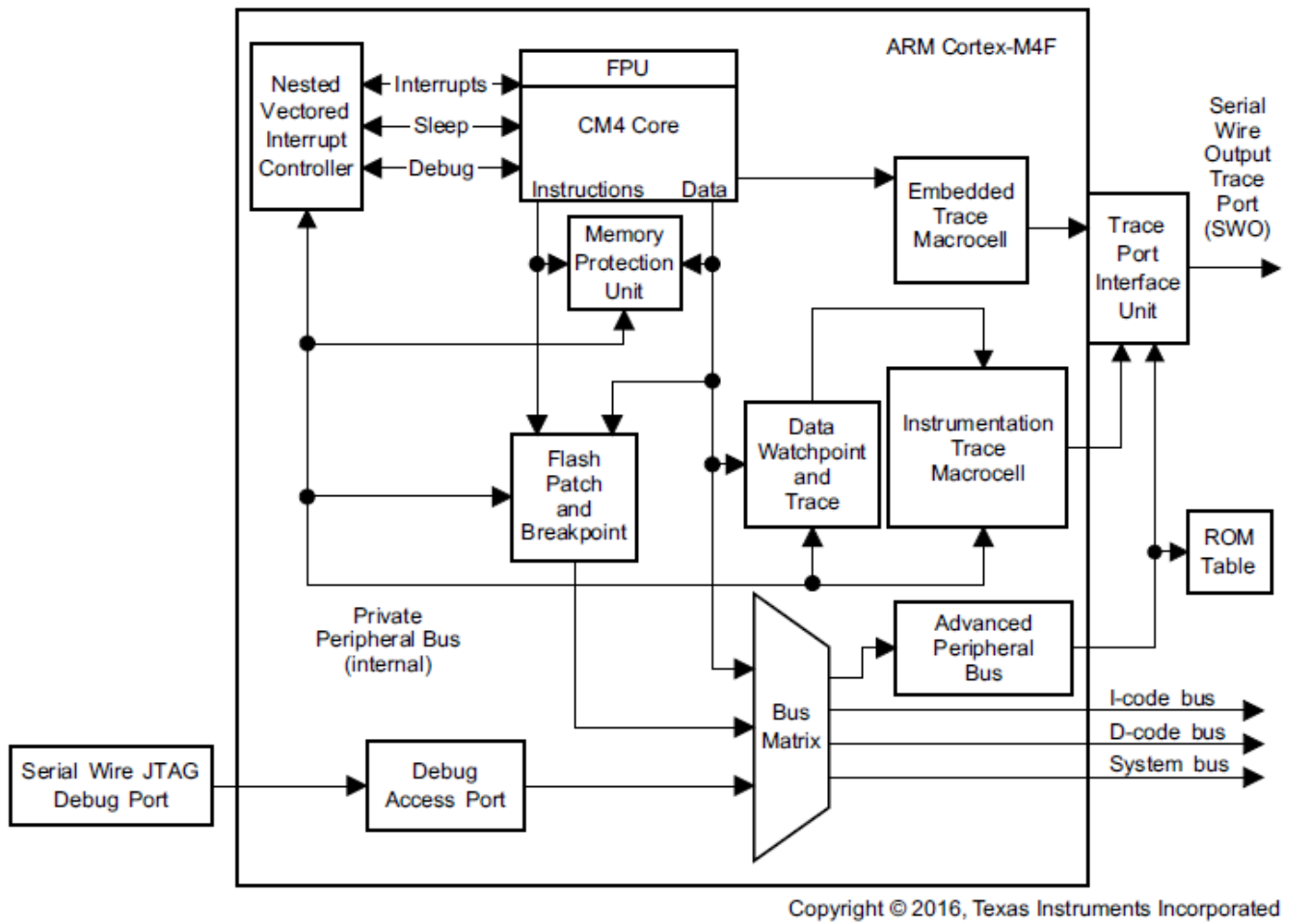
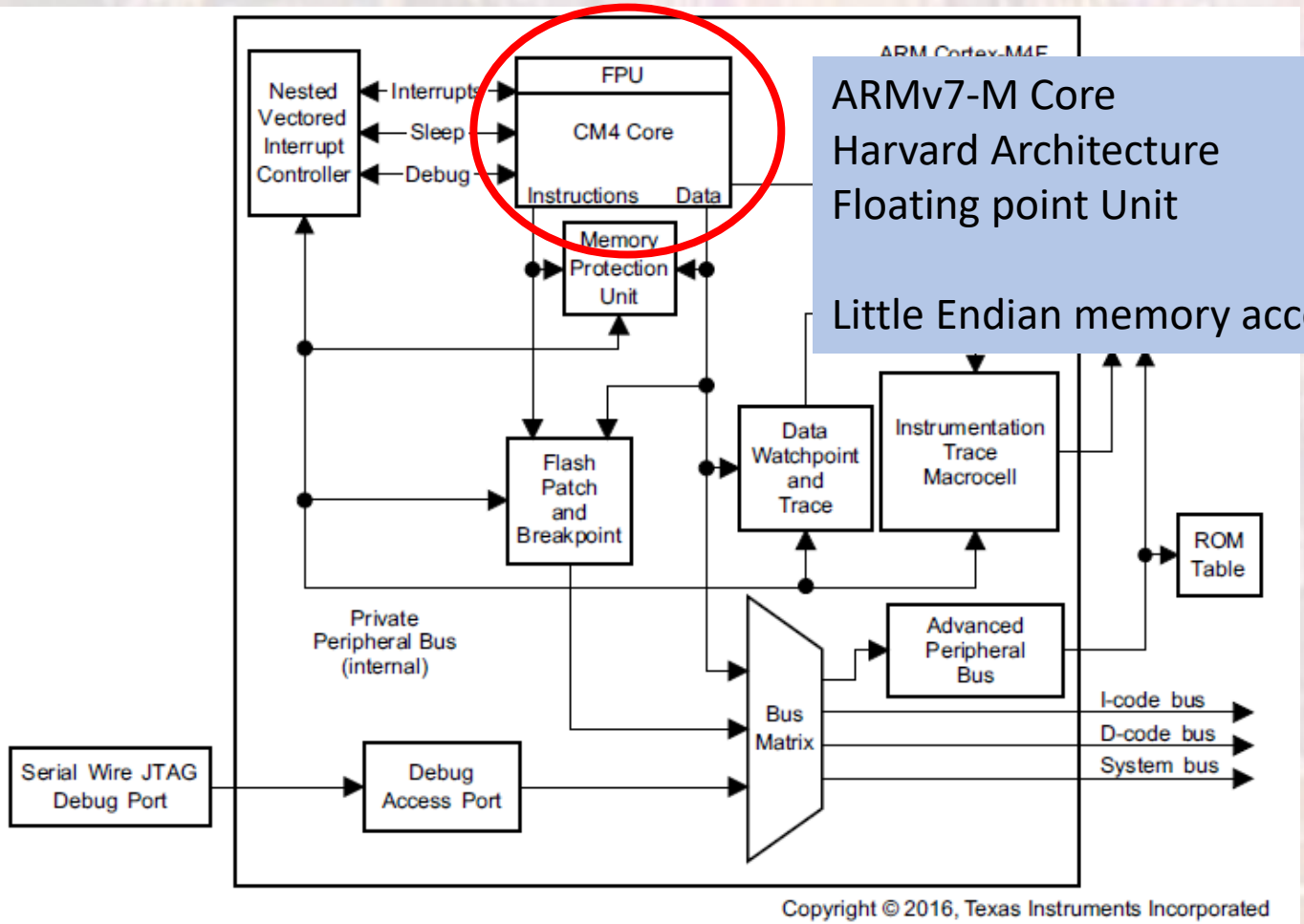


Figure 1-1. CPU Block Diagram

ARM M4

- CPU Block Diagram



ARMv7-M Core
Harvard Architecture
Floating point Unit

Little Endian memory access

Figure 1-1. CPU Block Diagram

ARM M4

- CPU Block Diagram

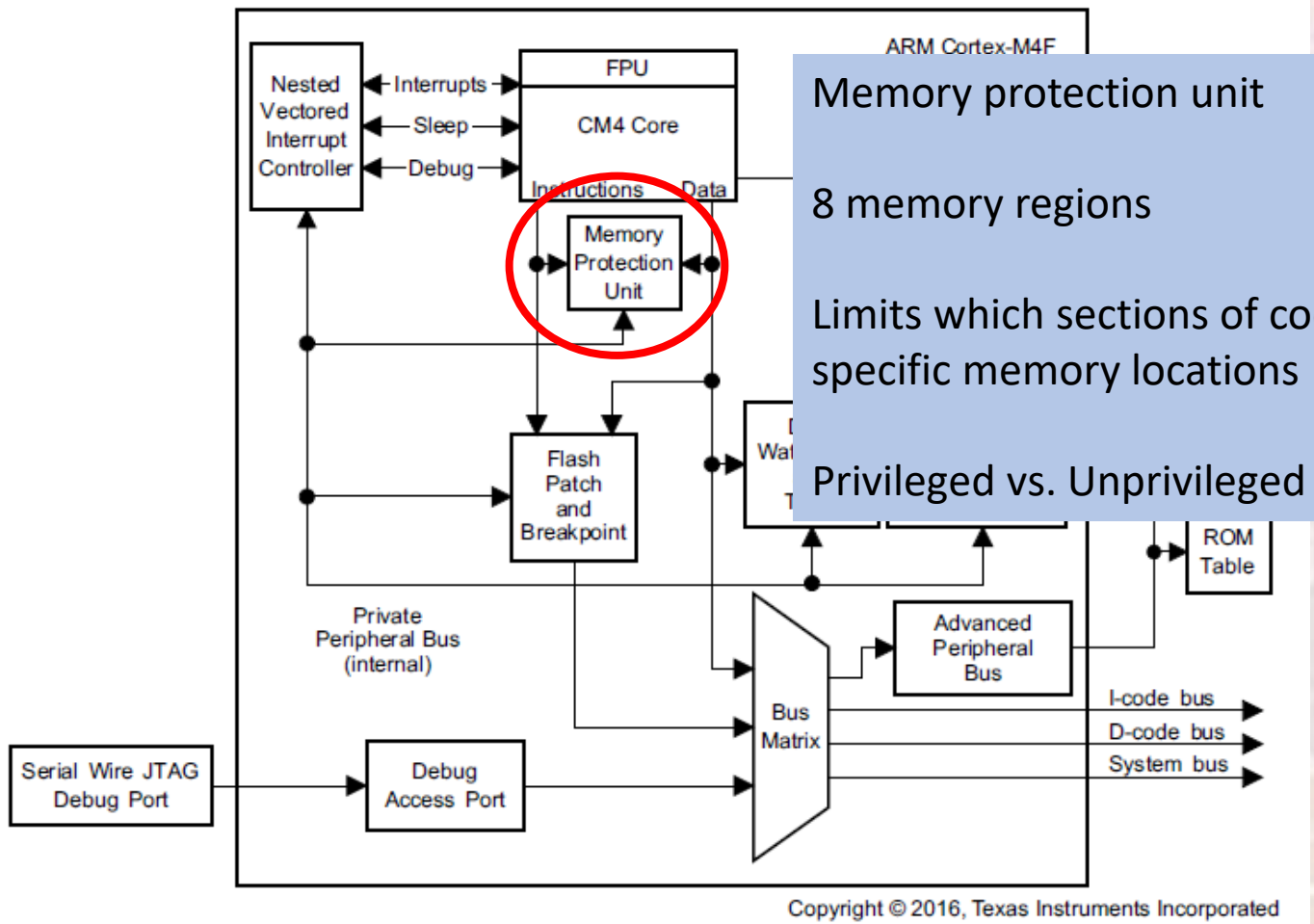


Figure 1-1. CPU Block Diagram

Memory protection unit

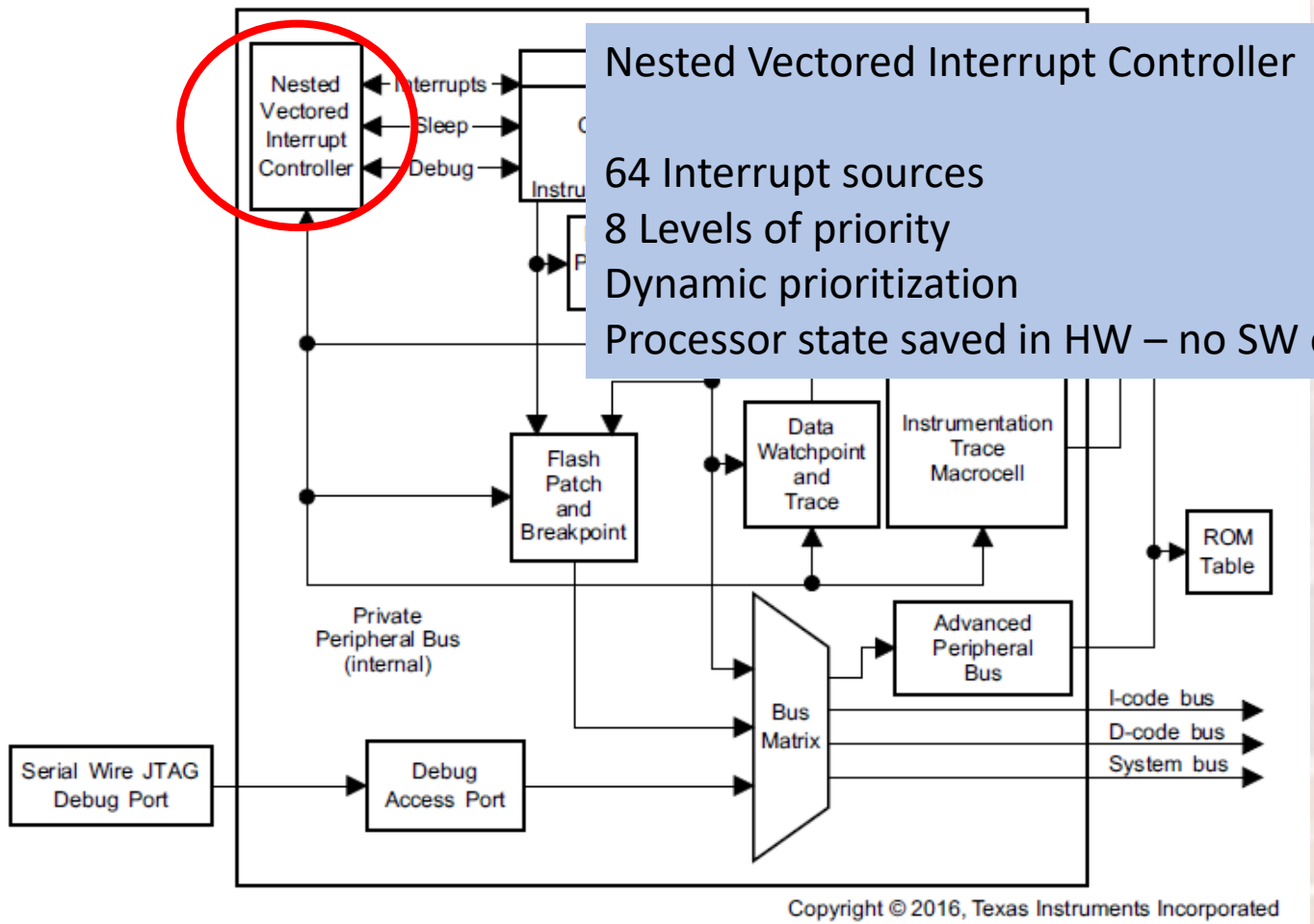
8 memory regions

Limits which sections of code can access specific memory locations

Privileged vs. Unprivileged (User) mode

ARM M4

- CPU Block Diagram



Nested Vectored Interrupt Controller

64 Interrupt sources
8 Levels of priority
Dynamic prioritization
Processor state saved in HW – no SW overhead

Figure 1-1. CPU Block Diagram

ARM M4

- CPU Block Diagram

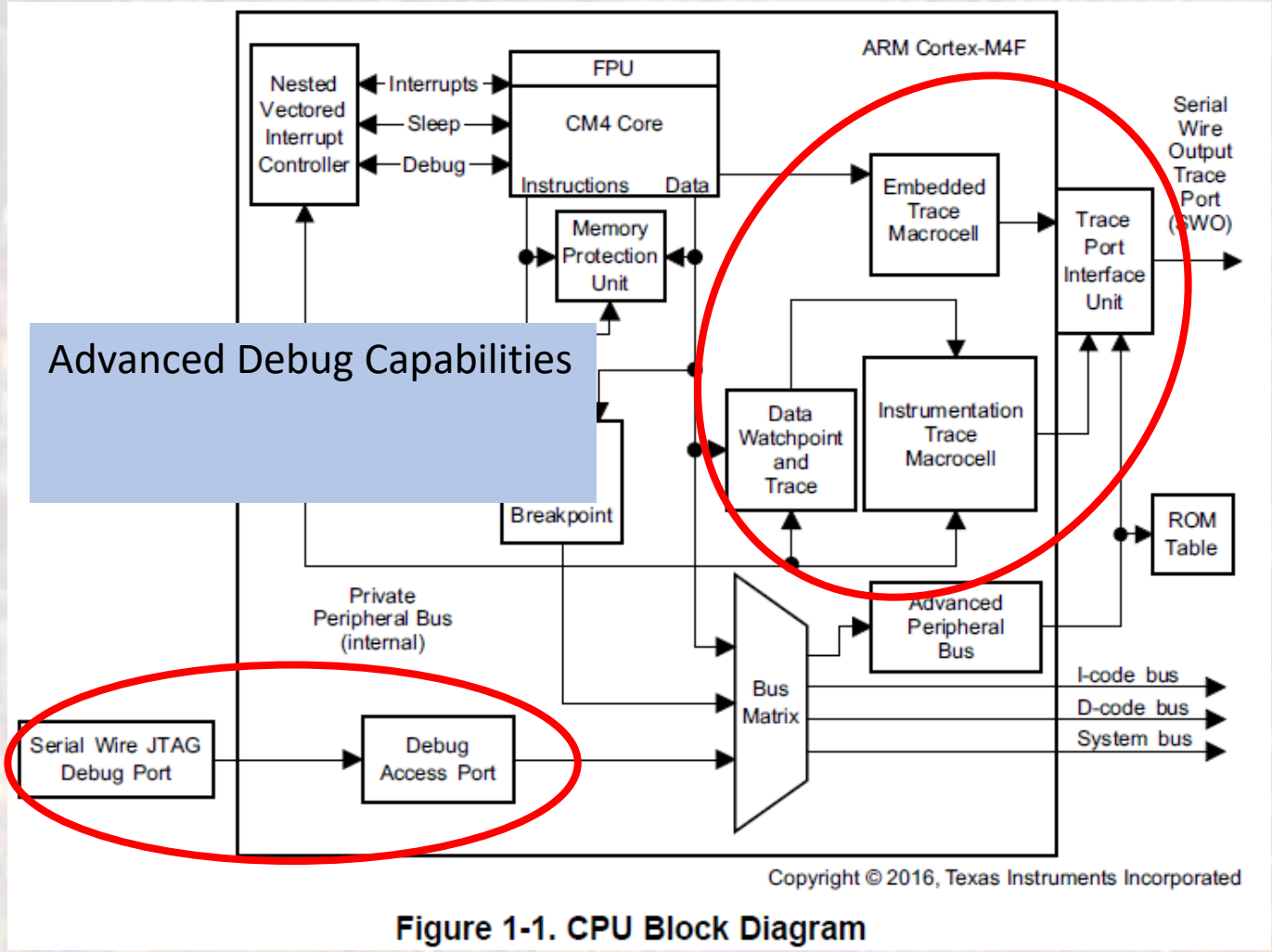
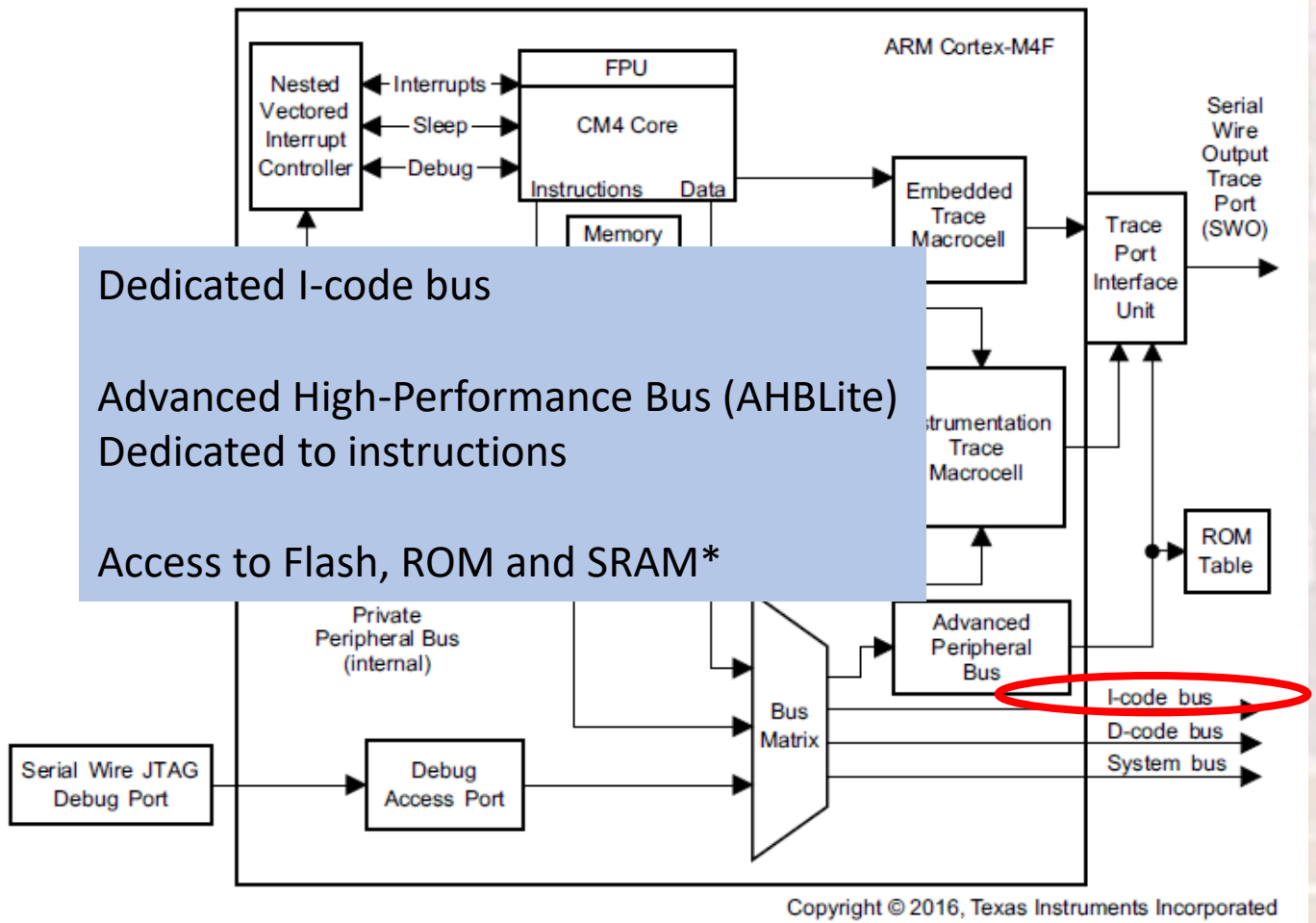


Figure 1-1. CPU Block Diagram

ARM M4

- CPU Block Diagram



Dedicated I-code bus

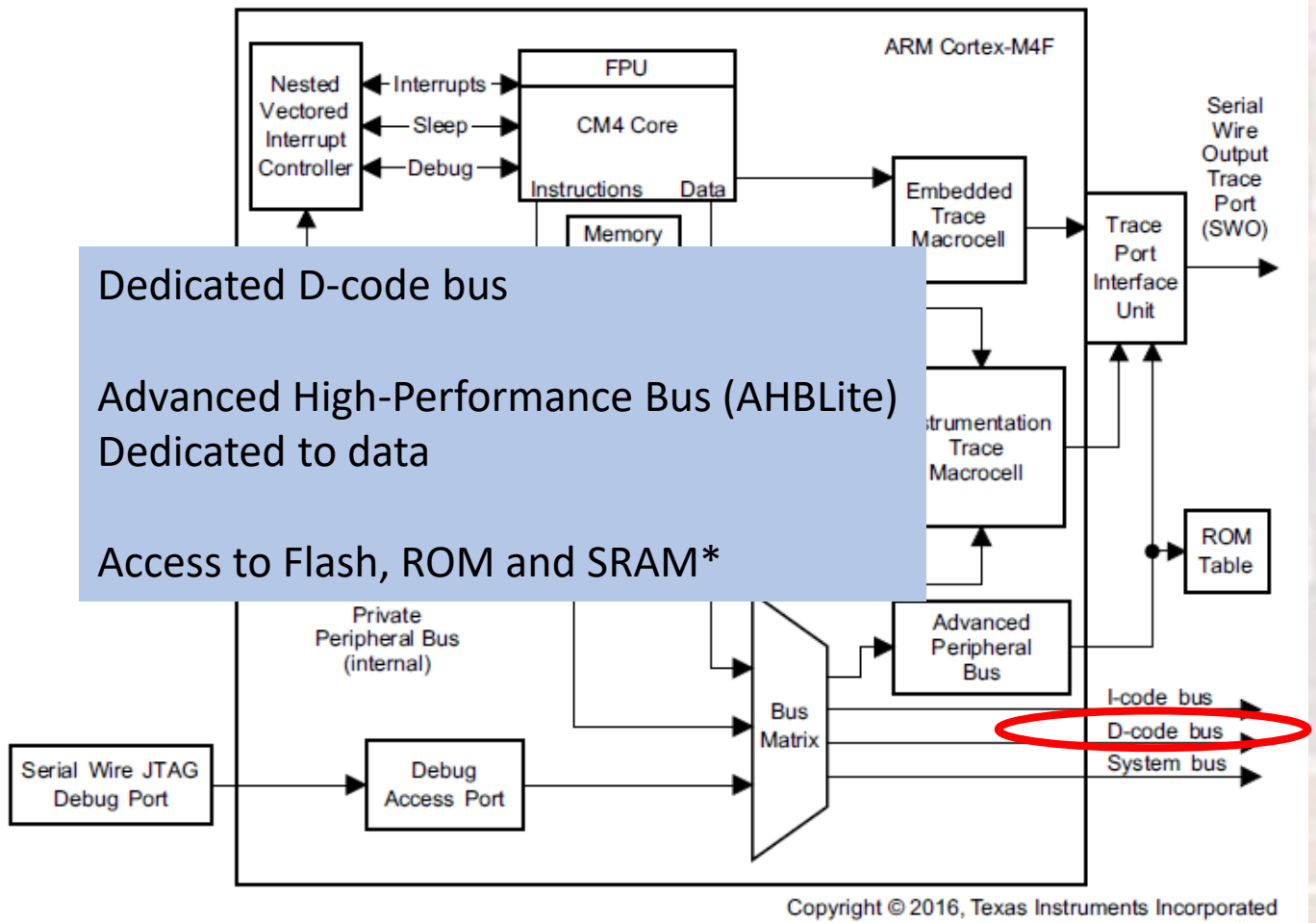
Advanced High-Performance Bus (AHBLite)
Dedicated to instructions

Access to Flash, ROM and SRAM*

Figure 1-1. CPU Block Diagram

ARM M4

- CPU Block Diagram



Dedicated D-code bus

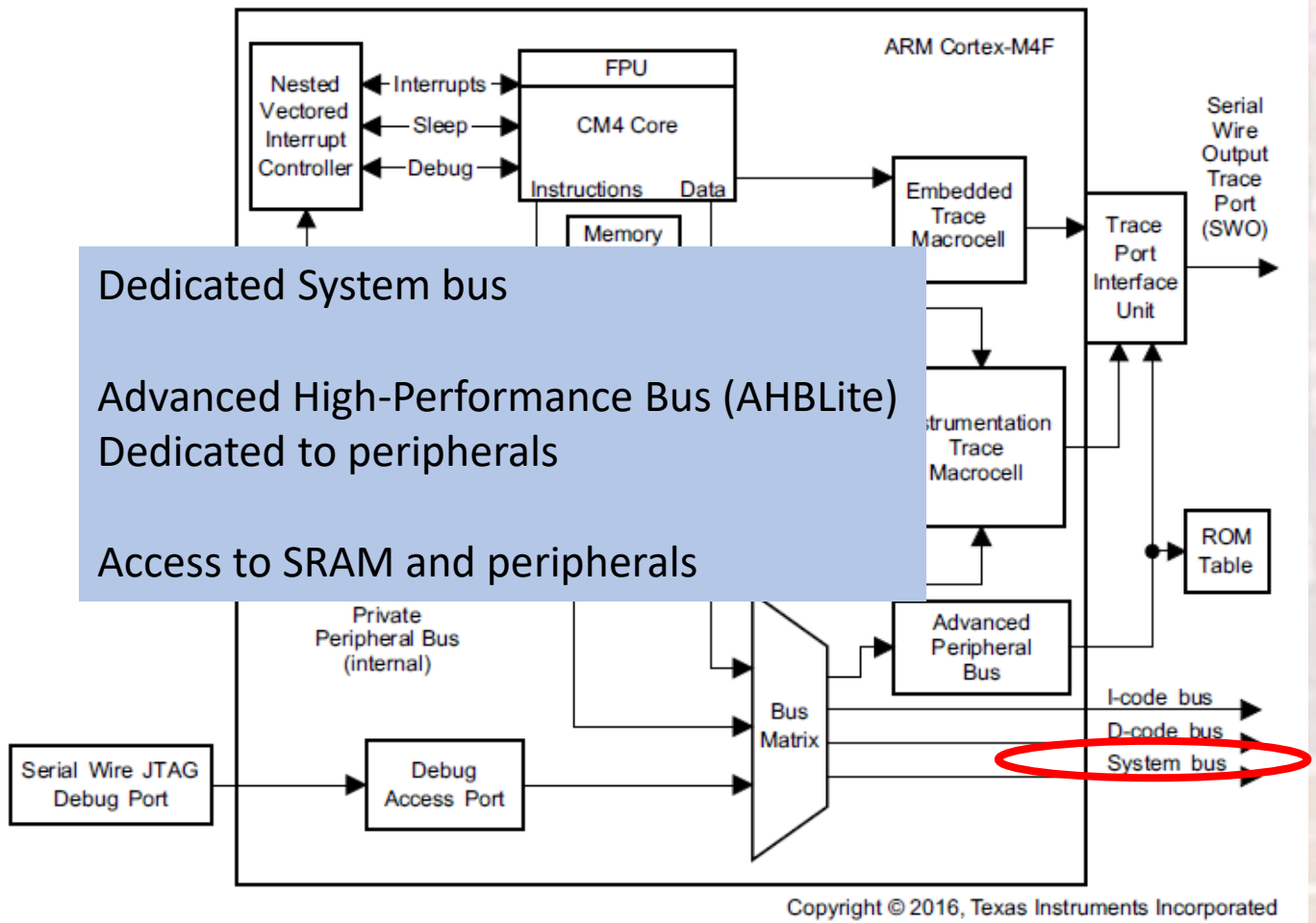
Advanced High-Performance Bus (AHBLite)
Dedicated to data

Access to Flash, ROM and SRAM*

Figure 1-1. CPU Block Diagram

ARM M4

- CPU Block Diagram



Dedicated System bus

Advanced High-Performance Bus (AHBLite)
Dedicated to peripherals

Access to SRAM and peripherals

Figure 1-1. CPU Block Diagram

ARM M4

- CPU Block Diagram

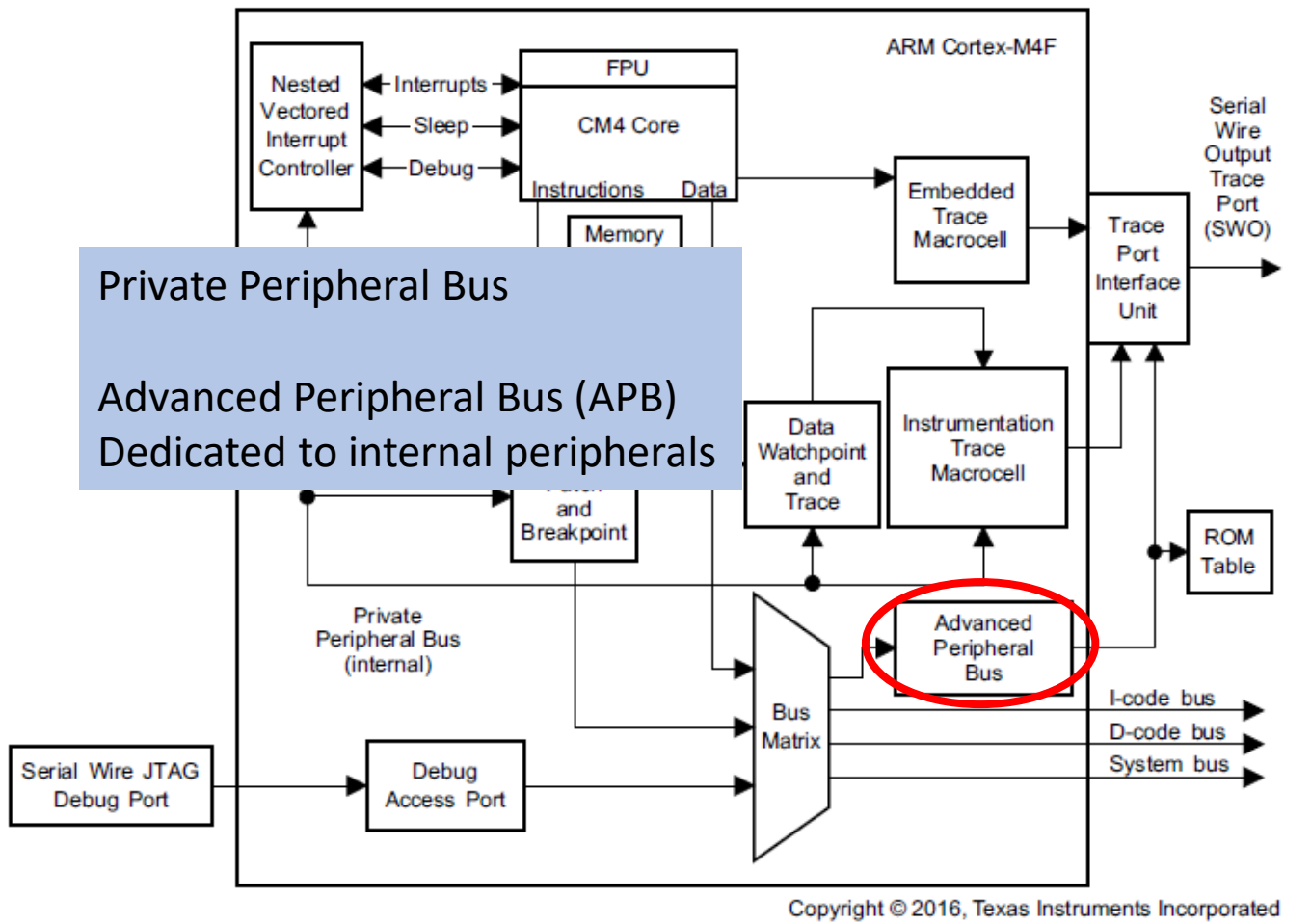


Figure 1-1. CPU Block Diagram

ARM M4

- CPU Register Set
  - 32 Bit registers
  - Not memory mapped
  - Program counter
  - Banked stack pointers(2)
  - Link register
  - Program Status register
  - Exception mask registers
  - Floating Point control
    - not shown – R21

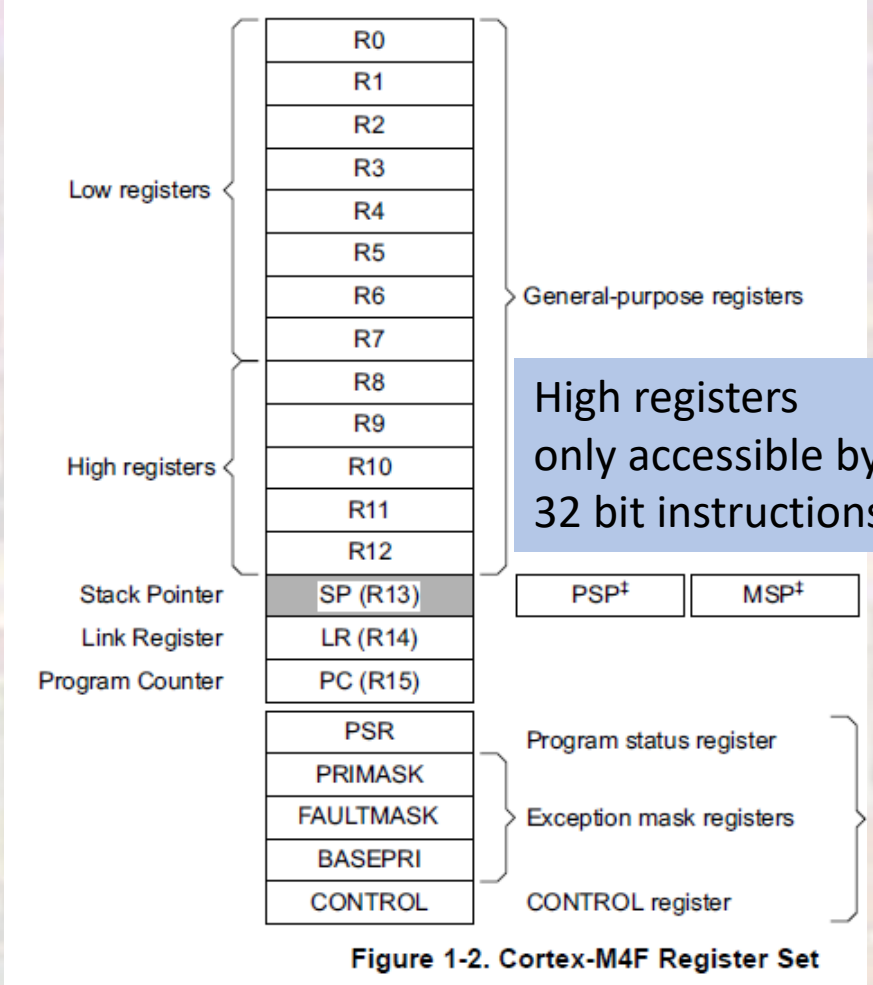
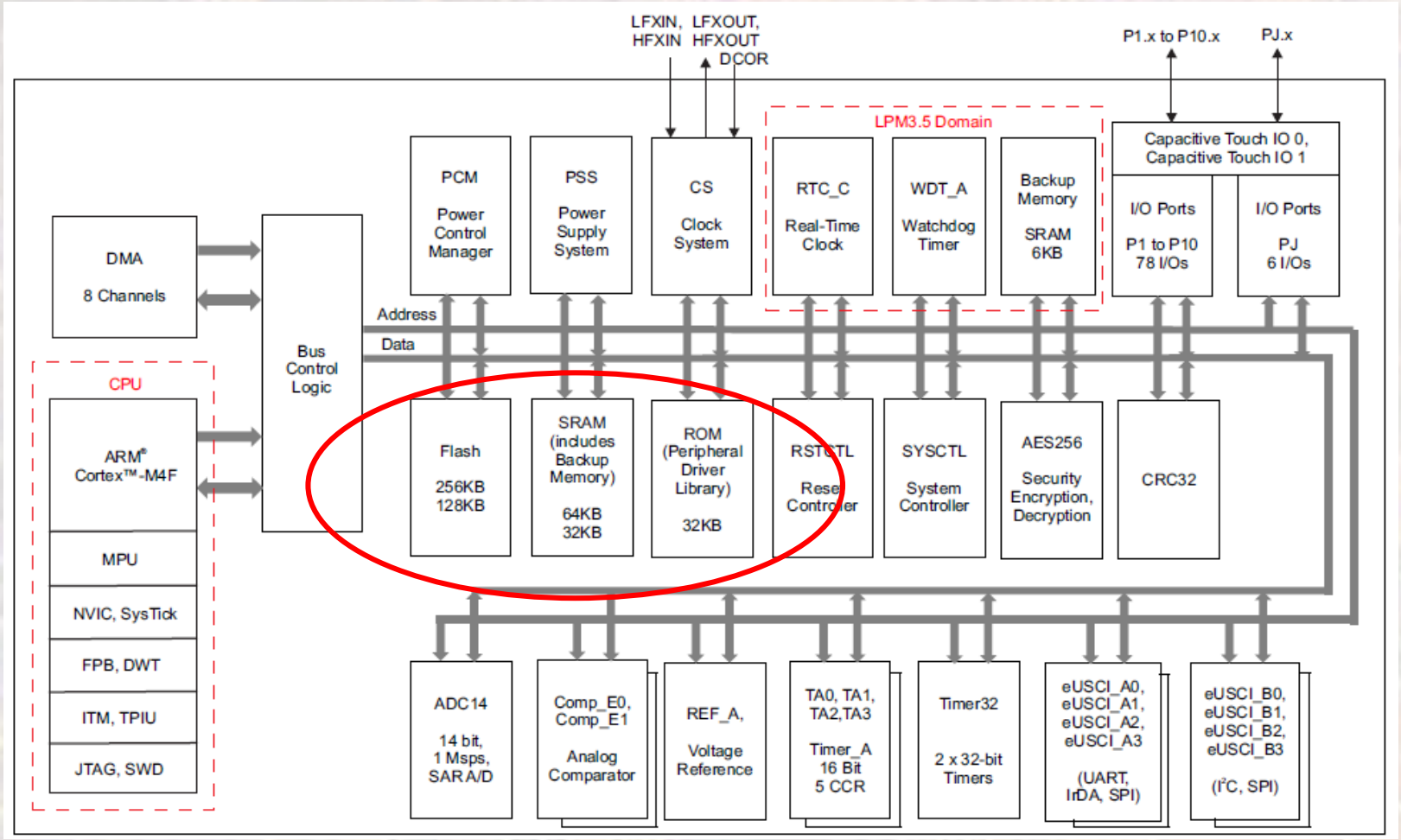


Figure 1-2. Cortex-M4F Register Set

MSP432P401R

- Memory Map



MSP432P401R

- Memory Map

  MSP432P401R

  - 256KB Flash
    - Code
  - 32KB ROM
    - Code
  - 64KB SRAM
    - Mapped to both code and data space
  - Peripheral Registers

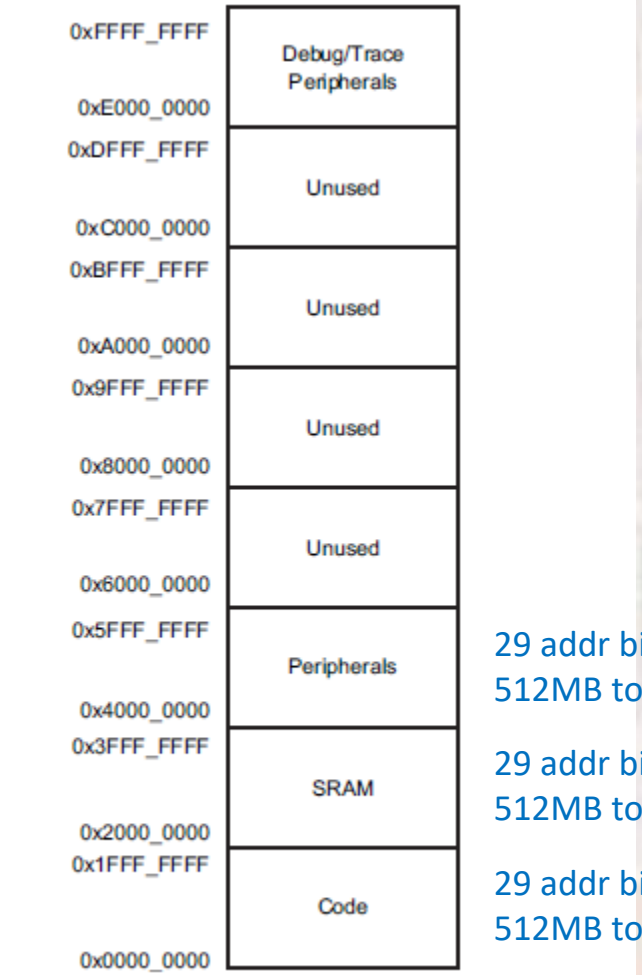


Figure 6-1. Device Memory Zones

MSP432P401R

- Memory Map
  - Code Zone
  - 256KB Flash used
  - 32KB ROM used
  - SRAM is mapped onto the code zone memory map

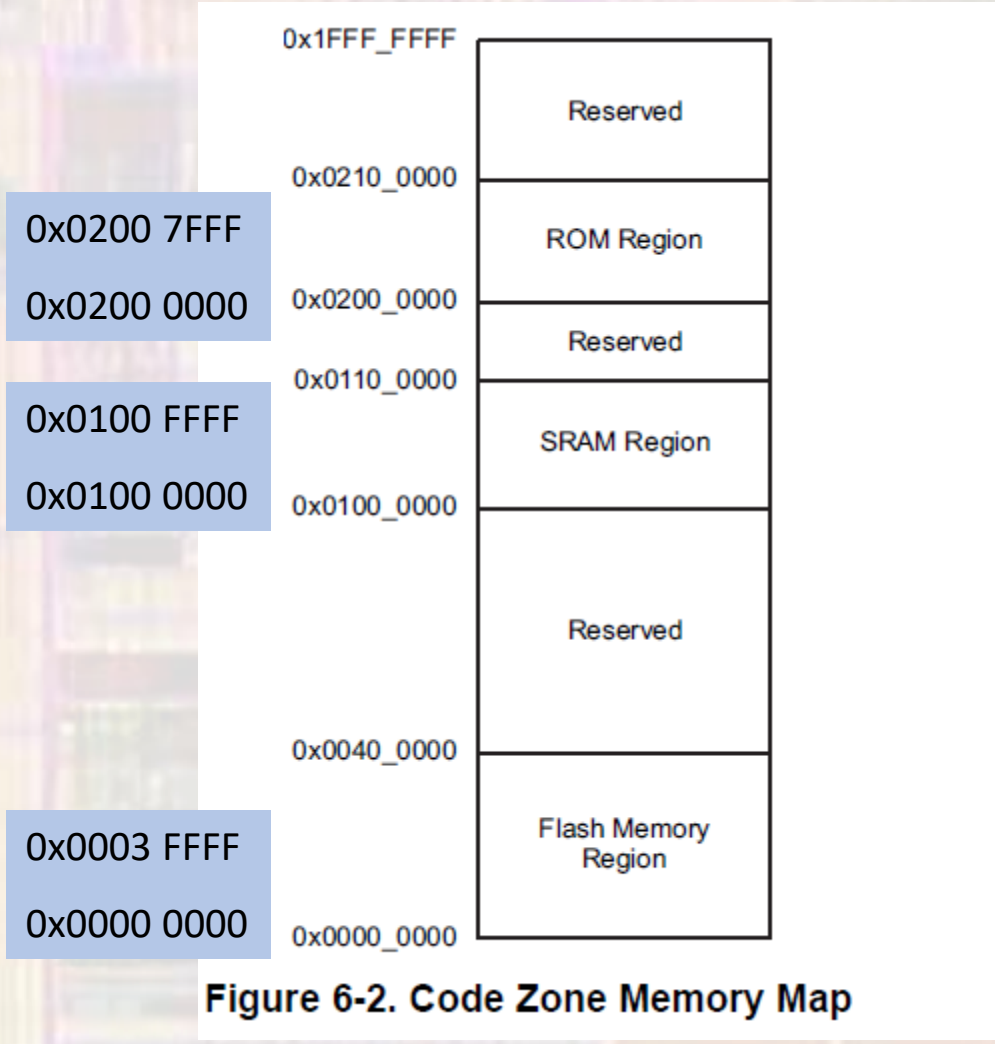


Figure 6-2. Code Zone Memory Map

MSP432P401R

- Memory Map
  - SRAM Zone
  - 64KB used
  - SRAM supports bit-banding
  - SRAM is mapped onto the code zone memory map

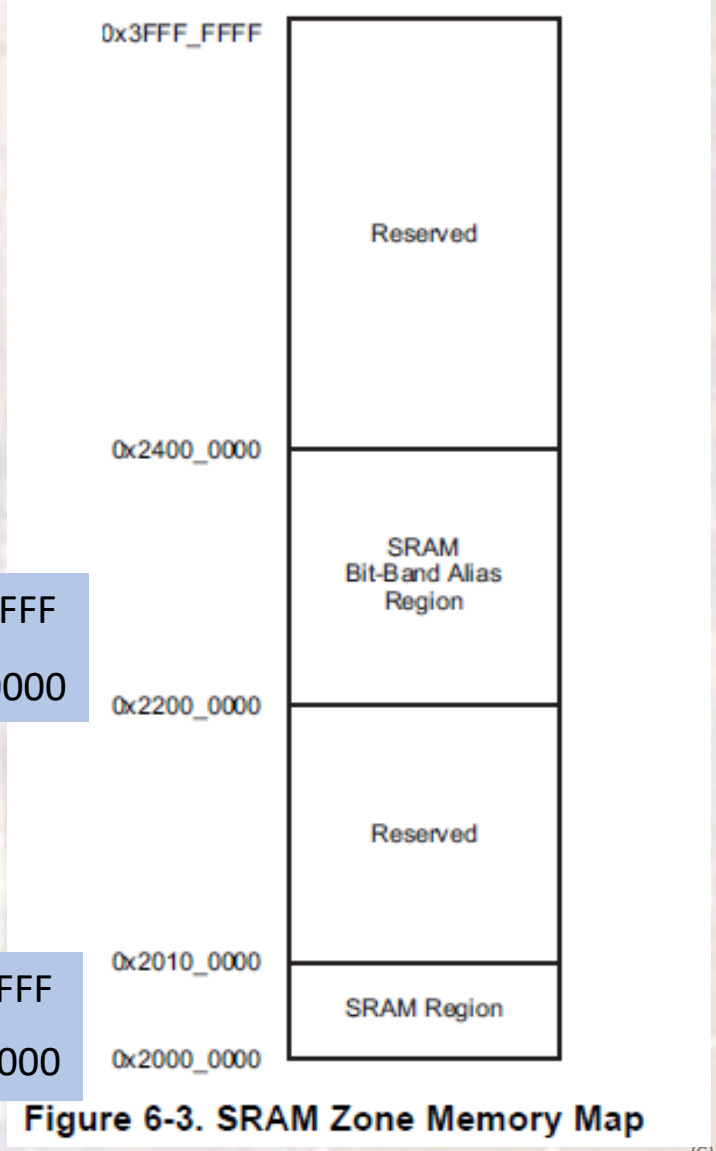
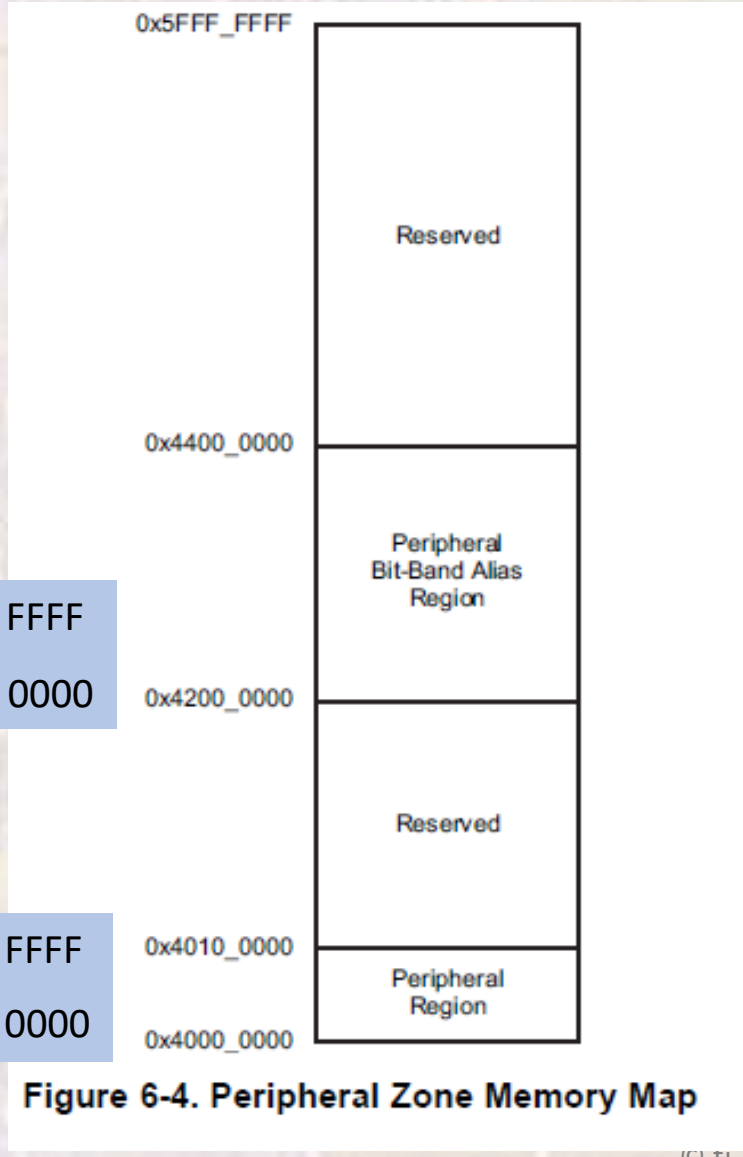


Figure 6-3. SRAM Zone Memory Map

MSP432P401R

- Memory Map
  - Peripheral Zone
  - 128KB used
  - Peripherals support bit-banding



0x423F FFFF

0x4200 0000

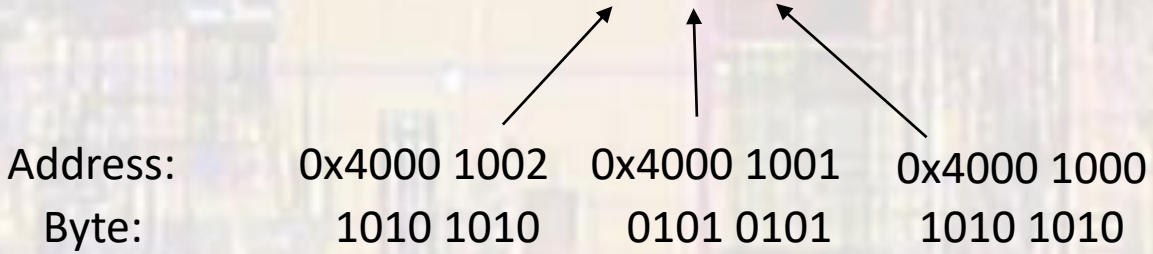
0x4001 FFFF

0x4000 0000

Figure 6-4. Peripheral Zone Memory Map

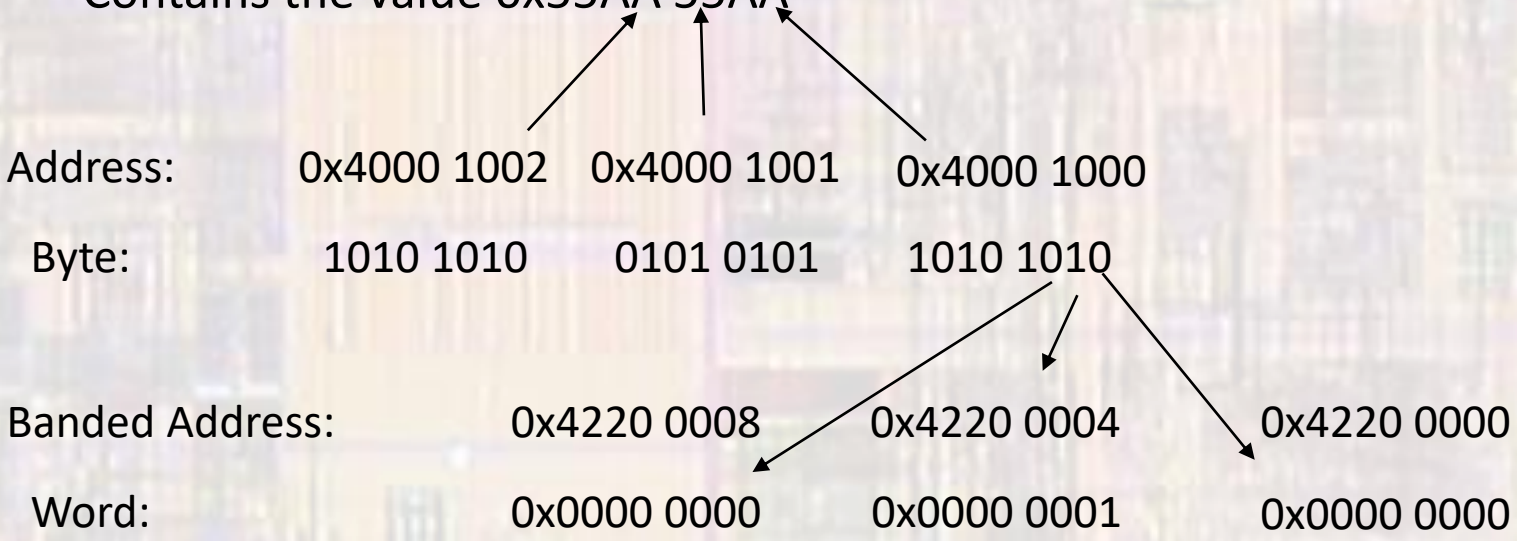
MSP432P401R

- Memory Map
  - Bit Banding
    - Allows access to individual bits
    - Simplifies bit-level manipulations
    - Provide atomic Read-Modify-Write
  - Uses a 32 bit word to access each bit in the original word
    - Original word located at 0x4000 1000
    - Contains the value 0x55AA 55AA



MSP432P401R

- Memory Map – Bit Banding
  - Uses a 32 bit word to access each bit in the original word
    - Original word located at 0x4000 1000
    - Contains the value 0x55AA 55AA



MSP432P401R

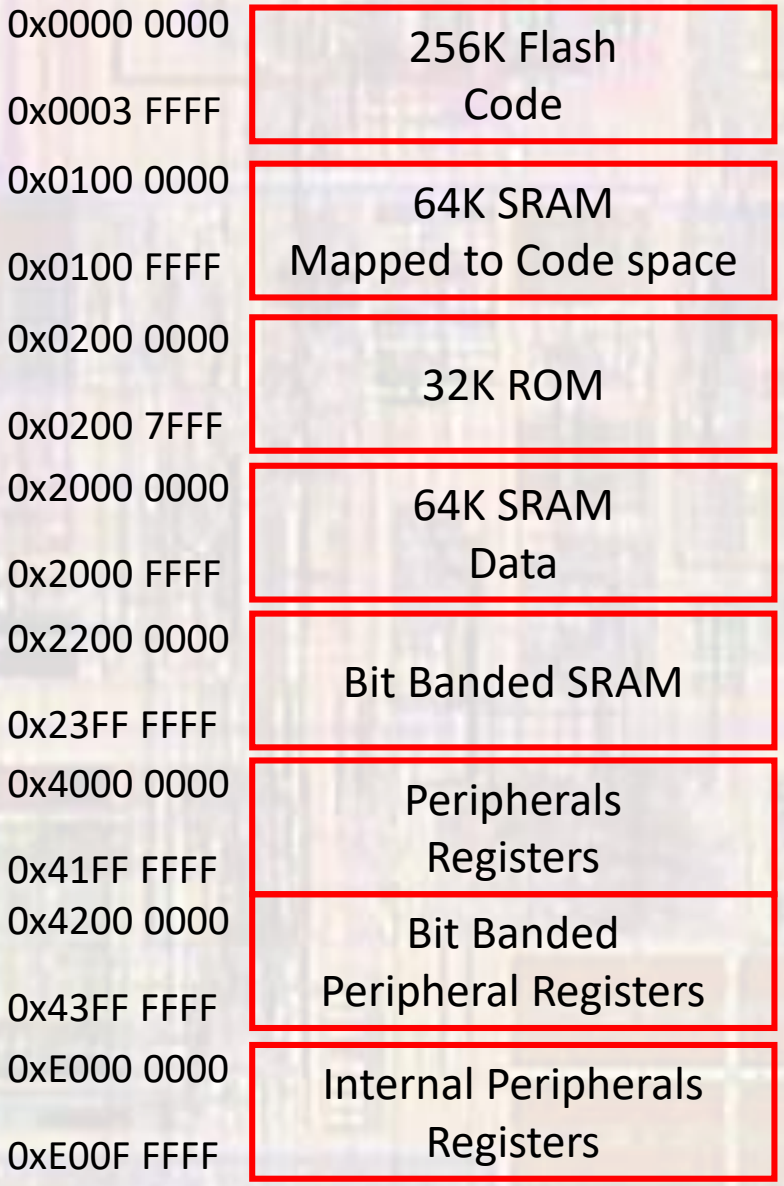
- Memory Map
  - Peripherals

Table 6-1. Peripheral Address Offsets

ADDRESS RANGE	PERIPHERAL	TABLE	REMARKS
0x4000_0000–0x4000_03FF	Timer_A0	Table 6-2	16-bit peripheral
0x4000_0400–0x4000_07FF	Timer_A1	Table 6-3	16-bit peripheral
0x4000_0800–0x4000_0BFF	Timer_A2	Table 6-4	16-bit peripheral
0x4000_0C00–0x4000_0FFF	Timer_A3	Table 6-5	16-bit peripheral
0x4000_1000–0x4000_13FF	eUSCI_A0	Table 6-6	16-bit peripheral
0x4000_1400–0x4000_17FF	eUSCI_A1	Table 6-7	16-bit peripheral
0x4000_1800–0x4000_1BFF	eUSCI_A2	Table 6-8	16-bit peripheral
0x4000_1C00–0x4000_1FFF	eUSCI_A3	Table 6-9	16-bit peripheral
0x4000_2000–0x4000_23FF	eUSCI_B0	Table 6-10	16-bit peripheral
0x4000_2400–0x4000_27FF	eUSCI_B1	Table 6-11	16-bit peripheral
0x4000_2800–0x4000_2BFF	eUSCI_B2	Table 6-12	16-bit peripheral
0x4000_2C00–0x4000_2FFF	eUSCI_B3	Table 6-13	16-bit peripheral
0x4000_3000–0x4000_33FF	REF_A	Table 6-14	16-bit peripheral
0x4000_3400–0x4000_37FF	COMP_E0	Table 6-15	16-bit peripheral
0x4000_3800–0x4000_3BFF	COMP_E1	Table 6-16	16-bit peripheral
0x4000_3C00–0x4000_3FFF	AES256	Table 6-17	16-bit peripheral
0x4000_4000–0x4000_43FF	CRC32	Table 6-18	16-bit peripheral
0x4000_4400–0x4000_47FF	RTC_C	Table 6-19	16-bit peripheral
0x4000_4800–0x4000_4BFF	WDT_A	Table 6-20	16-bit peripheral
0x4000_4C00–0x4000_4FFF	Port Module	Table 6-21	16-bit peripheral
0x4000_5000–0x4000_53FF	Port Mapping Controller	Table 6-22	16-bit peripheral
0x4000_5400–0x4000_57FF	Capacitive Touch I/O 0	Table 6-23	16-bit peripheral
0x4000_5800–0x4000_5BFF	Capacitive Touch I/O 1	Table 6-24	16-bit peripheral
0x4000_5C00–0x4000_8FFF	Reserved		Read only, always reads 0h
0x4000_9000–0x4000_BFFF	Reserved		Read only, always reads 0h
0x4000_C000–0x4000_CFFF	Timer32	Table 6-25	
0x4000_D000–0x4000_DFFF	Reserved		Read only, always reads 0h
0x4000_E000–0x4000_FFFF	DMA	Table 6-26	
0x4001_0000–0x4001_03FF	PCM	Table 6-27	
0x4001_0400–0x4001_07FF	CS	Table 6-28	
0x4001_0800–0x4001_0FFF	PSS	Table 6-29	
0x4001_1000–0x4001_17FF	FLCTL	Table 6-30	
0x4001_1800–0x4001_1BFF	Reserved		Read only, always reads 0h
0x4001_1C00–0x4001_1FFF	Reserved		Read only, always reads 0h
0x4001_2000–0x4001_23FF	ADC14	Table 6-31	
0x4001_2400–0x4001_FFFF	Reserved		Read only, always reads 0h

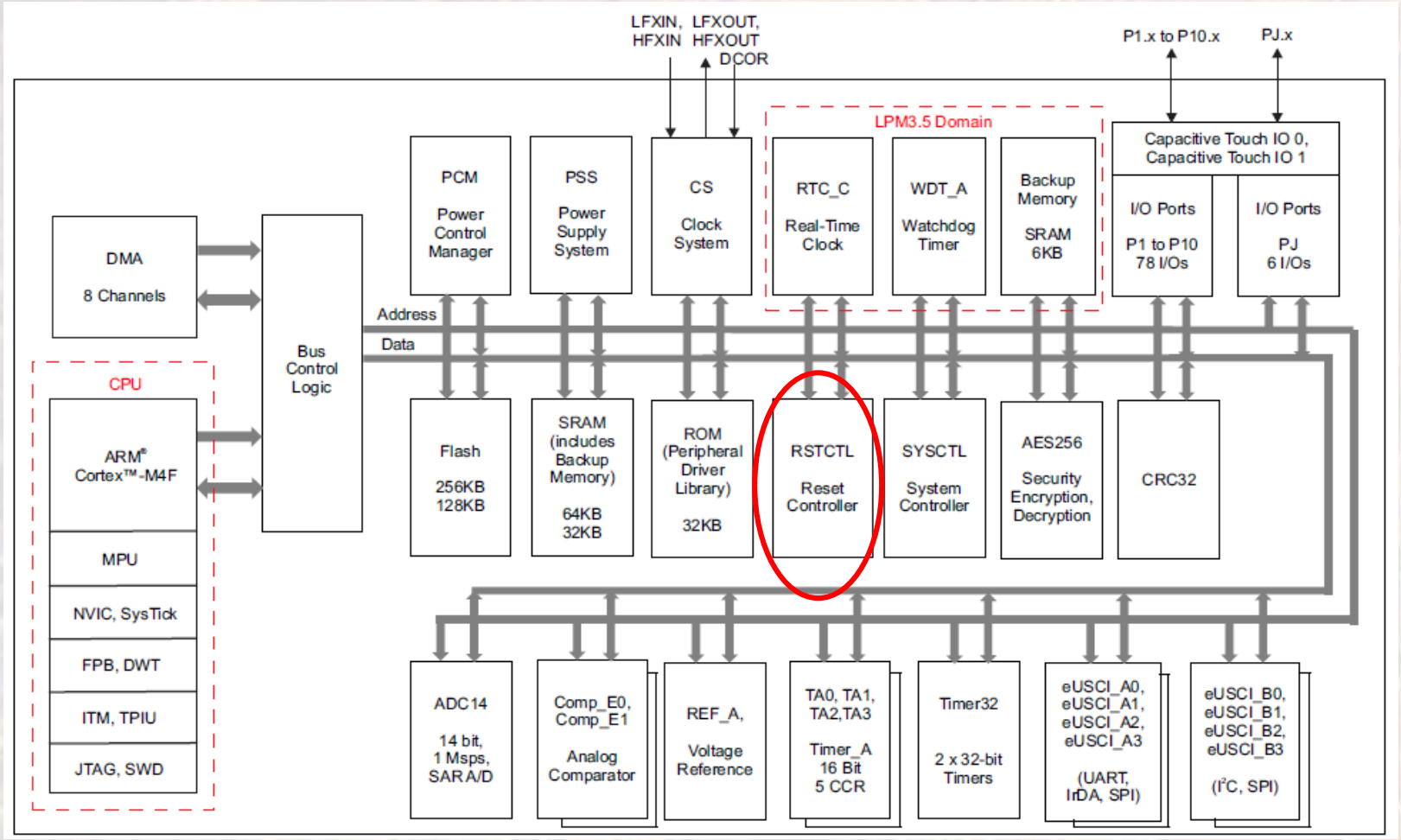
MSP432P401R

- Memory Map
  MSP432P401R
  - 256KB Flash
    - Code
  - 32KB ROM
    - Code
  - 64KB SRAM
    - Mapped to both code and data space
  - Peripheral Registers



MSP432P401R

- Reset Controller



MSP432P401R

- Reset Controller
  - 4 classes of Reset
  - Power Off/On Reset (POR)
  - Reboot Reset
  - Hard Reset
  - Soft Reset

MSP432P401R

- Reset Controller
  - Power Off/On Reset (POR)
    - Highest priority
    - Power off/on
    - User initiated reset
    - All components reset
    - SRAM not maintained
    - Debugger resets

MSP432P401R

- Reset Controller
  - Reboot Reset
    - 2nd highest priority
    - Same as POR except debugger is maintained
    - Allows for boot to be debugged
  - Hard Reset
    - User initiated reset
    - Processor is NOT rebooted
    - Control is returned to user code
    - All components reset
    - SRAM is maintained
    - Debugger is maintained

MSP432P401R

- Reset Controller
  - Soft Reset
    - User initiated reset
    - Processor is NOT rebooted
    - Control is returned to user code
    - All components maintained
    - SRAM is maintained
    - Debugger is maintained

MSP432P401R

- Reset Controller - Registers

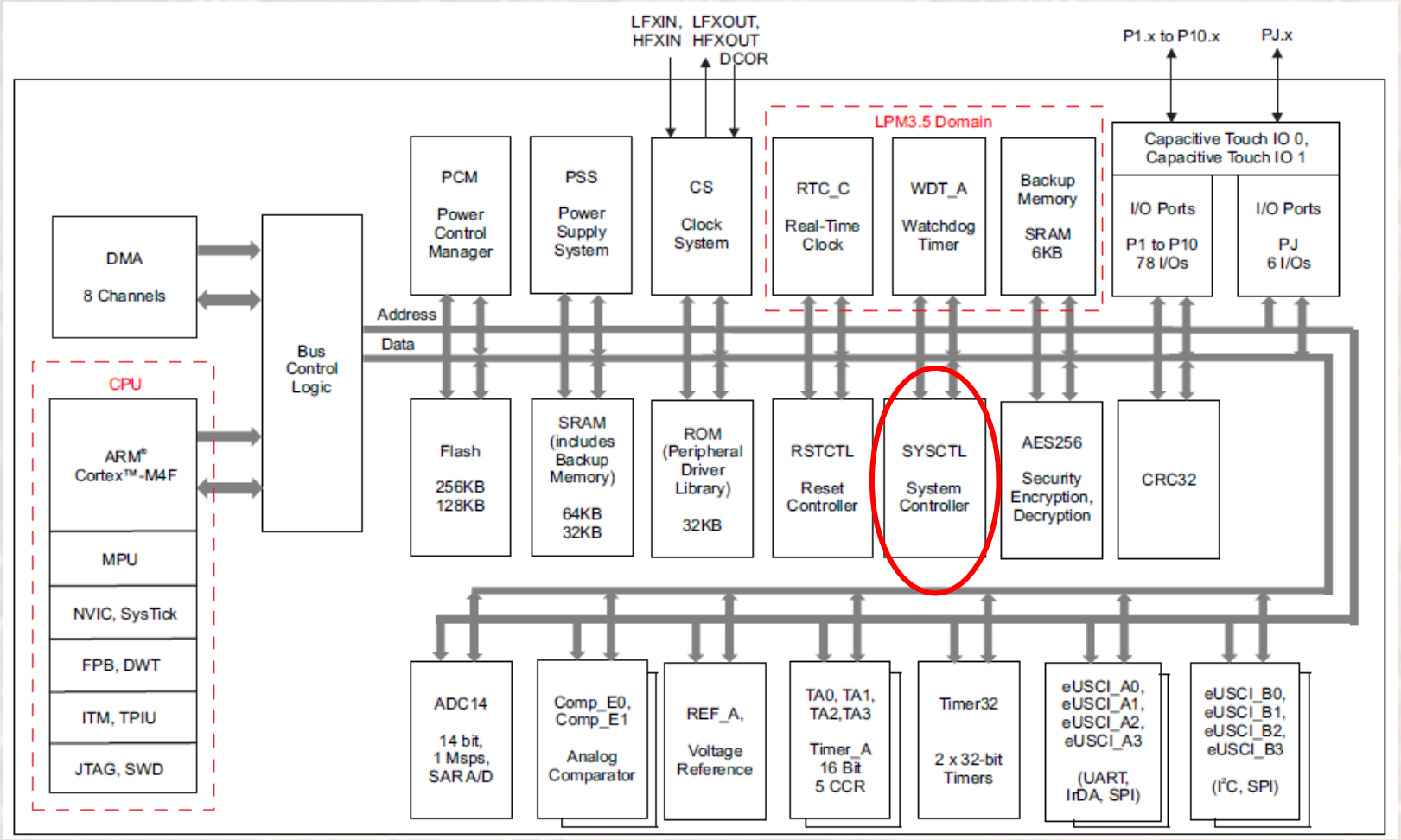
RSTCTL->RESET_REQ, …

Table 3-1. RSTCTL Registers

Offset	Acronym	Register Name	Section
000h	RSTCTL_RESET_REQ	Reset Request Register	Section 3.3.1
004h	RSTCTL_HARDRESET_STAT	Hard Reset Status Register	Section 3.3.2
008h	RSTCTL_HARDRESET_CLR	Hard Reset Status Clear Register	Section 3.3.3
00Ch	RSTCTL_HARDRESET_SET	Hard Reset Status Set Register	Section 3.3.4
010h	RSTCTL_SOFTRESET_STAT	Soft Reset Status Register	Section 3.3.5
014h	RSTCTL_SOFTRESET_CLR	Soft Reset Status Clear Register	Section 3.3.6
018h	RSTCTL_SOFTRESET_SET	Soft Reset Status Set Register	Section 3.3.7
100h	RSTCTL_PSSRESET_STAT	PSS Reset Status Register	Section 3.3.8
104h	RSTCTL_PSSRESET_CLR	PSS Reset Status Clear Register	Section 3.3.9
108h	RSTCTL_PCMRESET_STAT	PCM Reset Status Register	Section 3.3.10
10Ch	RSTCTL_PCMRESET_CLR	PCM Reset Status Clear Register	Section 3.3.11
110h	RSTCTL_PINRESET_STAT	Pin Reset Status Register	Section 3.3.12
114h	RSTCTL_PINRESET_CLR	Pin Reset Status Clear Register	Section 3.3.13
118h	RSTCTL_REBOOTRESET_STAT	Reboot Reset Status Register	Section 3.3.14
11Ch	RSTCTL_REBOOTRESET_CLR	Reboot Reset Status Clear Register	Section 3.3.15
120h	RSTCTL_CSRESET_STAT	CS Reset Status Register	Section 3.3.16
124h	RSTCTL_CSRESET_CLR	CS Reset Status Clear Register	Section 3.3.17

MSP432P401R

- System Controller



MSP432P401R

- System Controller
  - Device memory configuration and status
    - Flash configuration
    - SRAM configuration
    - SRAM retention in low power modes
  - Non-Maskable Interrupt sources configuration and status
    - RSTn/NMI device pin in NMI configuration
    - Clock System (CS) sources
    - Power Supply System (PSS) sources
    - Power Control Manager (PCM) sources

MSP432P401R

- System Controller
  - Watchdog configuration to generate hard reset or soft reset
  - Clock run or stop configuration to various modules in debug mode
  - Override controls for resets for device debug

MSP432P401R

- System Controller
  - Device security configuration
    - Secures Boot code
    - Blocks debugger access
    - Intellectual Property (IP) protection in Flash
  - Boot override code
  - Device configuration and peripherals calibration information through Device Descriptors
    - Clock calibration
    - Temperature sensor
    - Random number seed
    - Device part number

MSP432P401R

- System Controller

Table 2-58. SCB Registers

Offset	Acronym	Register Name	Type	Reset
D00h	CPUID	CPUID Base Register	read-only	410FC241h
D04h	ICSR	Interrupt Control State Register	read-write	00000000h
D08h	VTOR	Vector Table Offset Register	read-write	00000000h
D0Ch	AIRCR	Application Interrupt/Reset Control Register	read-write	FA050000h
D10h	SCR	System Control Register	read-write	00000000h
D14h	CCR	Configuration Control Register	read-write	00000200h
D18h	SHPR1	System Handlers 4-7 Priority Register	read-write	00000000h
D1Ch	SHPR2	System Handlers 8-11 Priority Register	read-write	00000000h
D20h	SHPR3	System Handlers 12-15 Priority Register	read-write	00000000h
D24h	SHCSR	System Handler Control and State Register	read-write	00000000h
D28h	CFSR	Configurable Fault Status Registers	read-write	00000000h
D2Ch	HFSR	Hard Fault Status Register	read-write	00000000h
D30h	DFSR	Debug Fault Status Register	read-write	00000000h
D34h	MMFAR	Mem Manage Fault Address Register	read-write	Undefined
D38h	BFAR	Bus Fault Address Register	read-write	Undefined
D3Ch	AFSR	Auxiliary Fault Status Register	read-write	00000000h
D40h	PFR0	Processor Feature register0	read-only	00000030h
D44h	PFR1	Processor Feature register1	read-only	00000200h
D48h	DFR0	Debug Feature register0	read-only	00100000h
D4Ch	AFR0	Auxiliary Feature register0	read-only	00000000h
D50h	MMFR0	Memory Model Feature register0	read-only	00100030h
D54h	MMFR1	Memory Model Feature register1	read-only	00000000h
D58h	MMFR2	Memory Model Feature register2	read-only	01000000h
D5Ch	MMFR3	Memory Model Feature register3	read-only	00000000h
D60h	ISAR0	ISA Feature register0	read-only	01101110h
D64h	ISAR1	ISA Feature register1	read-only	02112000h
D68h	ISAR2	ISA Feature register2	read-only	21232231h
D6Ch	ISAR3	ISA Feature register3	read-only	01111131h
D70h	ISAR4	ISA Feature register4	read-only	01310132h
D88h	CPACR	Coprocessor Access Control Register	read-write	00F00000h