MSP432 Spec

Last updated 6/17/19

MSP 432 Spec

- IC Specifications
  - Integrated circuit performance varies:
    - Part to part
      - Die to die
      - Wafer to wafer
      - Lot to lot
        - machine to machine
    - Over temperature
    - Over voltage
    - With load
    - Over time

MSP 432 Spec

- IC Specifications
  - Performance is guaranteed:
    - By design
    - By test
      - Wafer level
      - Part level
      - Accelerated life
    - Statistically
    - Use guard banding
      - Must be careful not to multiply effects

MSP 432 Spec

- Absolute Maximum Ratings

5.1 Absolute Maximum Ratings[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3	4.17	V
Voltage difference between DVCC and AVCC pins[2]		±0.3	V
Voltage applied to any pin[3]	–0.3	V_{CC} + 0.3 V (4.17 V MAX)	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} [4]	–40	125	°C
Maximum junction temperature, T_J		95	°C

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

MSP 432 Spec

° C	°F
150	302
125	257
100	212
85	185
25	77
0	32
-40	-40
-55	-67
-65	-85

- Absolute Maximum Ratings
  - Temperature Ranges
  - Commercial 0°C to 85°C 32°F to 185°F
  - Industrial -40°C to 100°C -40°F to 212°F
  - Automotive -40°C to 125°C -40°F to 257°F
  - Military -55°C to 125°C -67°F to 257°F

** These are not necessarily ambient temperature

MSP 432 Spec

- Absolute Maximum Ratings

  - Electro-Static Discharge

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] [2]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [3]	±250	

MSP 432 Spec

- Nominal Operating Conditions

5.3 Recommended Operating Conditions

Typical data are based on V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range at all DVCC and AVCC pins [1] [2] [3]	At power-up (with internal V_{CC} supervision)	1.71		3.7	V
		Normal operation with internal V_{CC} supervision	1.71		3.7	
		Normal operation without internal V_{CC} supervision	1.62		3.7	
V_{SS}	Supply voltage on all DVSS and AVSS pins			0		V
I_{INRUSH}	Inrush current into the V_{CC} pins [4]				100	mA
f_{MCLK}	Frequency of the CPU and AHB clock in the system [5]		0		48	MHz
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C

MSP 432 Spec

- Current Consumption

5.10 Current Consumption in LDO-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted)[1] [2] [3] [4] [5]

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM\_LDO\_VCORE0,Flash}$ [6] [7] [8]	Flash	3.0 V	490	625	1500	1700	2650	2950	3580	3900							µA
$I_{AM\_LDO\_VCORE1,Flash}$ [6] [7] [8]	Flash	3.0 V	510	685	1650	1900	2970	3300	4260	4700	5300	5800	6500	7100	7700	8400	µA
$I_{AM\_LDO\_VCORE0,SRAM}$ [9]	SRAM	3.0 V	435	565	1070	1240	1800	2010	2530	2800							µA
$I_{AM\_LDO\_VCORE1,SRAM}$ [9]	SRAM	3.0 V	450	620	1160	1370	1980	2250	2800	3120	3650	4020	4470	4900	5280	5760	µA

5.11 Current Consumption in DC-DC-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted)[1] [2] [3] [4] [5]

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM\_DCDC\_VCORE0,Flash}$ [6] [7] [8]	Flash	3.0 V	400	475	925	1050	1530	1720	2060	2300							µA
$I_{AM\_DCDC\_VCORE1,Flash}$ [6] [7] [8]	Flash	3.0 V	430	550	1100	1280	1880	2140	2650	3000	3290	3700	4020	4500	4720	5300	µA
$I_{AM\_DCDC\_VCORE0,SRAM}$ [9]	SRAM	3.0 V	370	450	680	780	1040	1180	1410	1600							µA
$I_{AM\_DCDC\_VCORE1,SRAM}$ [9]	SRAM	3.0 V	390	510	790	940	1250	1440	1720	1960	2200	2480	2670	3000	3050	3420	µA

MSP 432 Spec

- Current Consumption

5.12 Current Consumption in Low-Frequency Active Modes – Dhrystone 2.1 Program

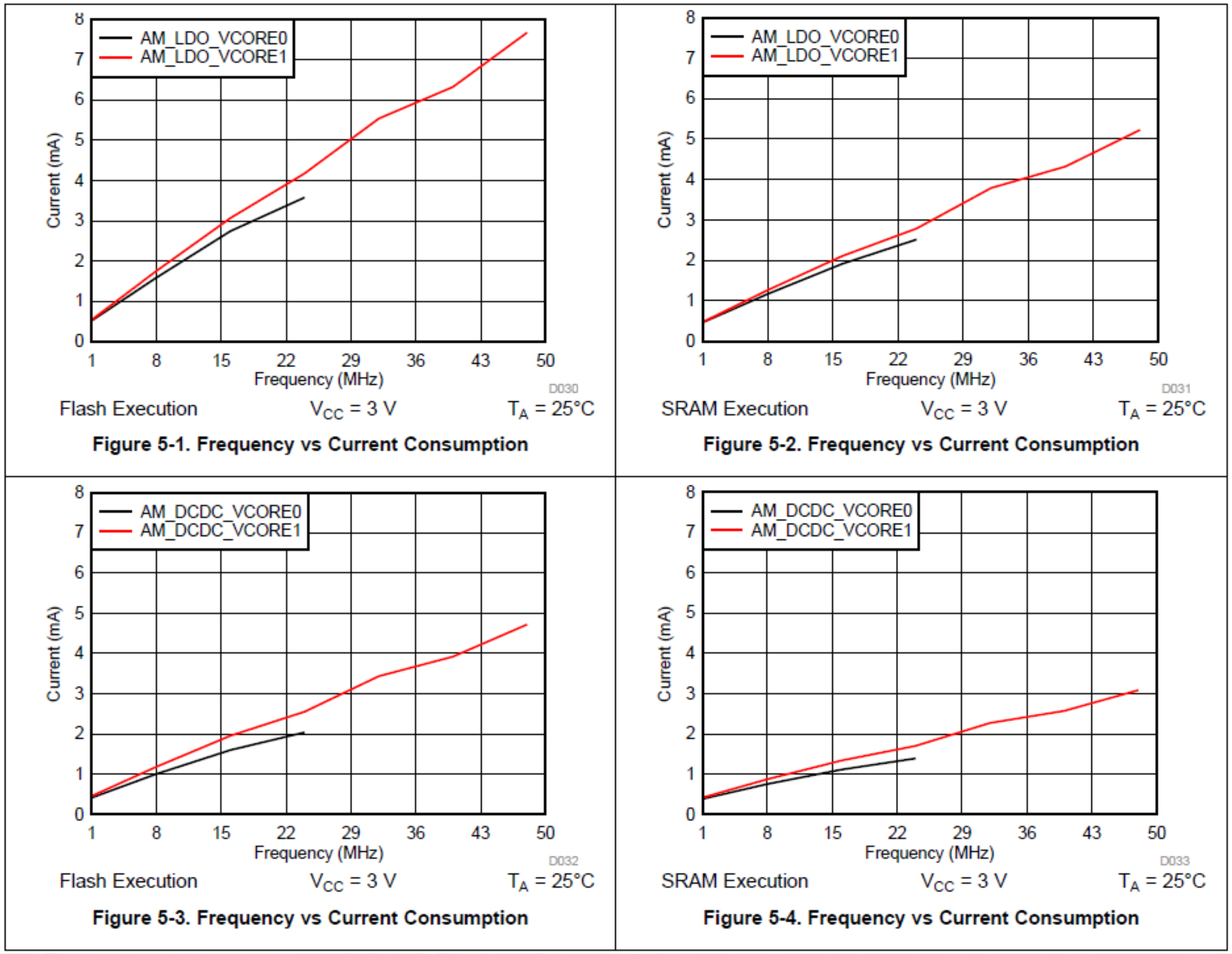
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] [2] [3] [4] [5]

PARAMETER	EXECUTION MEMORY	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM\_LF\_VCORE0, Flash}$ [6] [7] [8]	Flash	2.2 V	75		80		95		115		µA
		3.0 V	78		83	100	98		118	200	
$I_{AM\_LF\_VCORE1, Flash}$ [6] [7] [8]	Flash	2.2 V	78		85		105		125		µA
		3.0 V	81		88	110	108		128	245	
$I_{AM\_LF\_VCORE0, SRAM}$ [9]	SRAM	2.2 V	68		73		90		105		µA
		3.0 V	71		76	92	93		108	190	
$I_{AM\_LF\_VCORE1, SRAM}$ [9]	SRAM	2.2 V	70		77		98		117		µA
		3.0 V	73		90	102	101		120	235	

MSP 432 Spec

- Current Consumption

5.13 Typical Characteristics of Active Mode Currents for CoreMark Program



MSP 432 Spec

- Current Consumption

5.23 Current Consumption of Digital Peripherals

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
I_{TIMER_A}	Timer_A configured as PWM timer with 50% duty cycle	5		µA/MHz
$I_{TIMER32}$	Timer32 enabled	3.5		µA/MHz
I_{UART}	eUSCI_A configured in UART mode	6.5		µA/MHz
I_{SPI}	eUSCI_A configured in SPI master mode	5		µA/MHz
I_{I2C}	eUSCI_B configured in I^2C master mode	5		µA/MHz
I_{WDT_A}	WDT_A configured in interval timer mode	6		µA/MHz
I_{RTC_C}	RTC_C enabled and sourced from 32-kHz LFXT	100		nA
I_{AES256}	AES256 active	19		µA/MHz
I_{CRC32}	CRC32 active	2		µA/MHz

(1) Measured with VCORE = 1.2 V

MSP 432 Spec

- DC Characteristics
  - Inputs

Table 5-22. Digital Inputs (Applies to Both Normal and High-Drive I/Os)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2.2 V	0.99		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.21	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2.2 V	0.32		0.84	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	30	40	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins shared with analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg,ndio}$	Normal I/O high-impedance input leakage current	See [1][2]	2.2 V, 3 V			±20	nA
$I_{lkg,hdio}$	High-drive I/O high-impedance input leakage current	See [1][2]	2.2 V, 3 V			±20	nA

MSP 432 Spec

- DC Characteristics
  - Outputs

Table 5-23. Digital Outputs, Normal I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)} = -1$ mA[1]	2.2 V	$V_{CC} - 0.25$	V_{CC}	V
		$I_{(OHmax)} = -3$ mA[2]		$V_{CC} - 0.60$	V_{CC}	
		$I_{(OHmax)} = -2$ mA[1]	3.0 V	$V_{CC} - 0.25$	V_{CC}	
		$I_{(OHmax)} = -6$ mA[2]		$V_{CC} - 0.60$	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)} = 1$ mA[1]	2.2 V	V_{SS}	$V_{SS} + 0.25$	V
		$I_{(OLmax)} = 3$ mA[2]		V_{SS}	$V_{SS} + 0.60$	
		$I_{(OLmax)} = 2$ mA[1]	3.0 V	V_{SS}	$V_{SS} + 0.25$	
		$I_{(OLmax)} = 6$ mA[2]		V_{SS}	$V_{SS} + 0.60$	

MSP 432 Spec

- DC Characteristics
  - Outputs

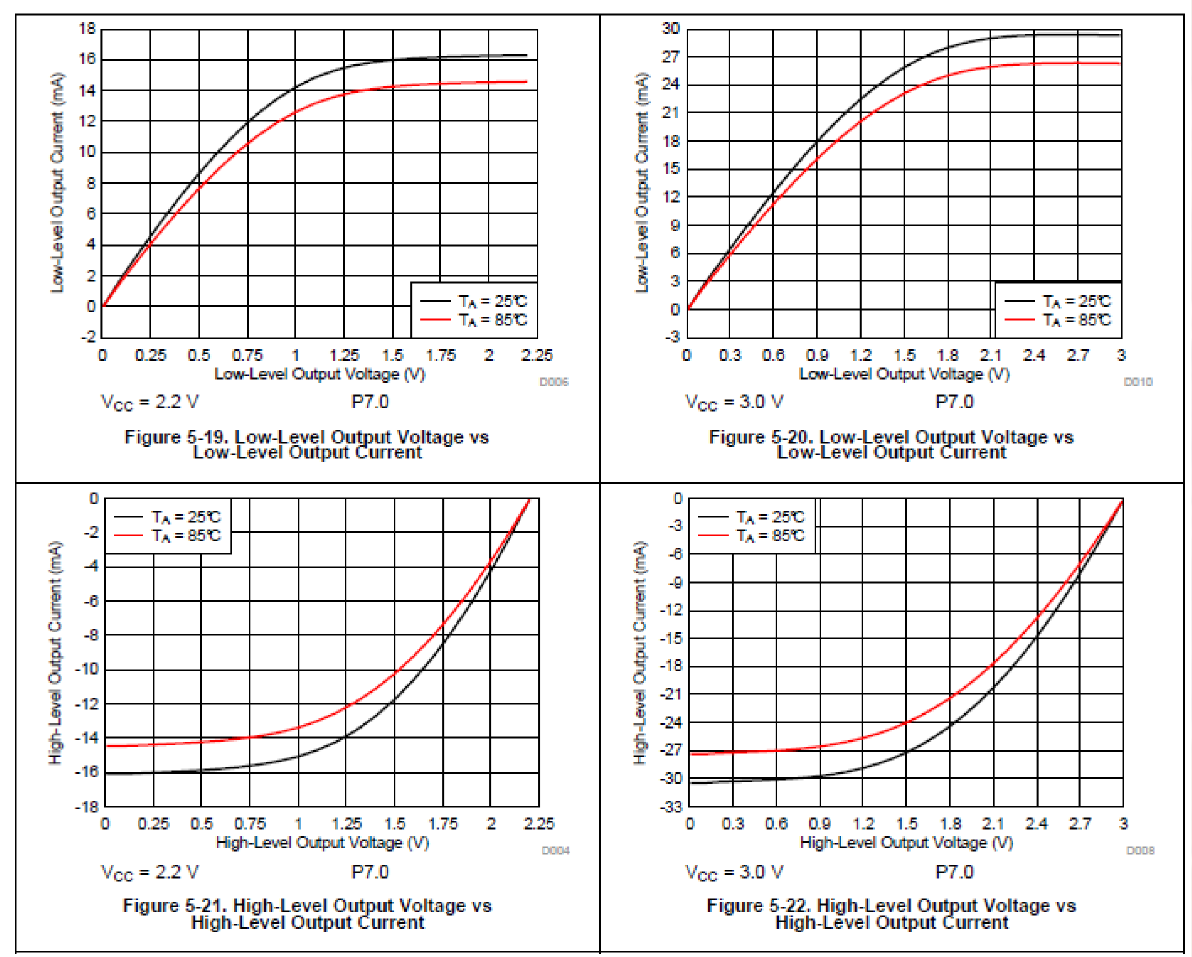


Figure 5-19. Low-Level Output Voltage vs Low-Level Output Current

Figure 5-20. Low-Level Output Voltage vs Low-Level Output Current

Figure 5-21. High-Level Output Voltage vs High-Level Output Current

Figure 5-22. High-Level Output Voltage vs High-Level Output Current

MSP 432 Spec

- DC Characteristics
  - VRef

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {0} for 1.2 V, REFON = 1	1.62 V		1.2	±1%	V
		REFVSEL = {1} for 1.45 V, REFON = 1	1.75 V		1.45	±1%	
		REFVSEL = {3} for 2.5 V, REFON = 1	2.8 V		2.5	±1%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.62			V
		REFVSEL = {1} for 1.45 V		1.75			
		REFVSEL = {3} for 2.5 V		2.8			
I_{REF+}	Operating supply current into AVCC terminal[(1)]	REFON = 1	3 V		15	20	µA

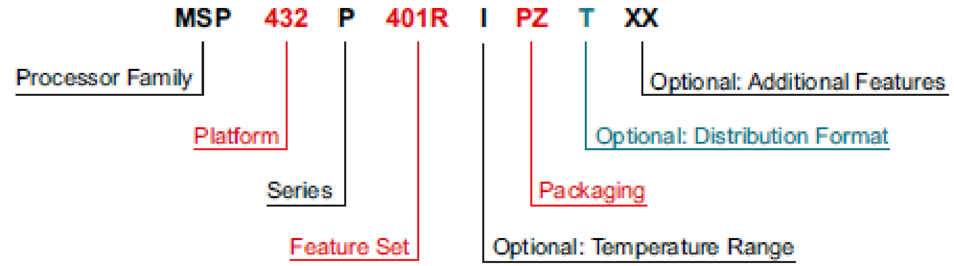
MSP 432 Spec

- AC Characteristics
  - Outputs

$f_{Px.y}$	Port output frequency (with RC load)[3]	VCORE = 1.4 V, C_L = 20 pF, R_L [4] [5]	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
$d_{Px.y}$	Port output duty cycle (with RC Load)	VCORE = 1.4 V, C_L = 20 pF, R_L [4] [5]	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
f_{Port_CLK}	Clock output frequency[3]	VCORE = 1.4 V, C_L = 20 pF[5]	1.62 V	24		MHz
			2.2 V	24		
			3.0 V	24		
d_{Port_CLK}	Clock output duty cycle	VCORE = 1.4 V, C_L = 20 pF[5]	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF [6]	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF [7]	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{rise,ana}$	Port output rise time, port pins with shared analog functions	C_L = 20 pF [6]	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,ana}$	Port output fall time, port pins with shared analog functions	C_L = 20 pF [7]	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	

MSP 432 Spec

- Packaging



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon
Platform	432 = TI's 32-Bit Low-Power Microcontroller Platform
Series	P = Performance and Low-Power Series
Feature Set	**First Digit** 4 = Flash-based devices up to 48 MHz **Second Digit** 0 = General purpose **Third Digit** 1 = ADC14 **Fourth Digit** R = 256KB of flash 64KB of SRAM M = 128KB of flash 32KB of SRAM
Optional: Temperature Range	S = 0°C to 50°C I = –40°C to 85°C T = –40°C to 105°C
Packaging	http://www.ti.com/packaging
Optional: Distribution Format	T = Small reel R = Large reel No markings = Tube or tray
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified

MSP 432 Spec

- Example
  - Estimate the power used by the processor running out of Flash in active mode (vcore 0) and operating at 3V, 24MHz, 25°C
  - What is the penalty for operating in Vcore 1 mode at this frequency

From the graph:
Icc(24MHz, 3v) = 3.5mA

P = 3v x 3.5mA = 10.5mW

From the graph:
Icc(24MHz, 3v) = 4.2mA

P = 3v x 4.2mA = 12.6mW
20% penalty

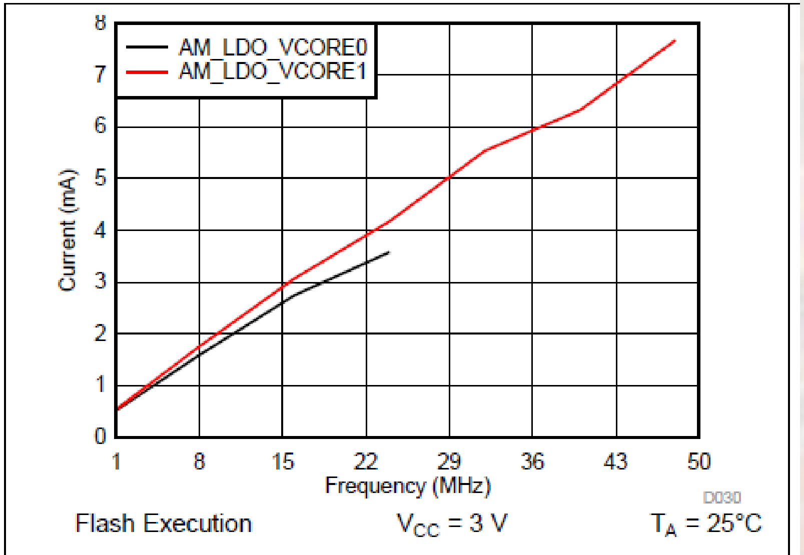


Figure 5-1. Frequency vs Current Consumption

MSP 432 Spec

- Example
  - Estimate the power used by the processor running out of Flash in active mode (vcore 0) and operating at 3V, 24MHz, 25°C with 2 Timer32s, a SPI, and the WDT running

From the graph:
Icc(24MHz, 3v) = 3.5mA

I timers = 2 * 3.5uA/MHz * 24MHz
= 168uA
I spi = 5uA/MHz * 24MHz
= 120uA
I wdt = 6uA/MHz * 24MHz
= 144uA

5.23 Current Consumption of Digital Peripherals

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
I_{TIMER_A}	Timer_A configured as PWM timer with 50% duty cycle	5		μA/MHz
$I_{TIMER32}$	Timer32 enabled	3.5		μA/MHz
I_{UART}	eUSCI_A configured in UART mode	6.5		μA/MHz
I_{SPI}	eUSCI_A configured in SPI master mode	5		μA/MHz
I_{I2C}	eUSCI_B configured in I^2C master mode	5		μA/MHz
I_{WDT_A}	WDT_A configured in interval timer mode	6		μA/MHz
I_{RTC_C}	RTC_C enabled and sourced from 32-kHz LFXT	100		nA
I_{AES256}	AES256 active	19		μA/MHz
I_{CRC32}	CRC32 active	2		μA/MHz

(1) Measured with VCORE = 1.2 V

I total = 3.932mA → Ptotal = 11.8mW

MSP 432 Spec

- Example
  - What output value would a typical output pin pull a 500Ω resister tied to Vcc down to? Assume Vcc=3.0v, T=25°C

Approximate the current
3V/500Ω = < 6mA

From the graph: near 6ma
Slope = (6mA – 0mA) / (.3V – 0V)
= 20mA/V
Intercept = 6mA – 20mA/V * 0.3V = 0

$V_{OL} = 3 - I_{OL} * R$
$I_{OL} = 20mA/V * V_{OL} + 0$

$I_{OL} = 20mA/V * (3 – I_{OL} * R)$
$I_{OL} = 5.45mA$

$V_{OL} = 3 – 2.73 = 0.27V$

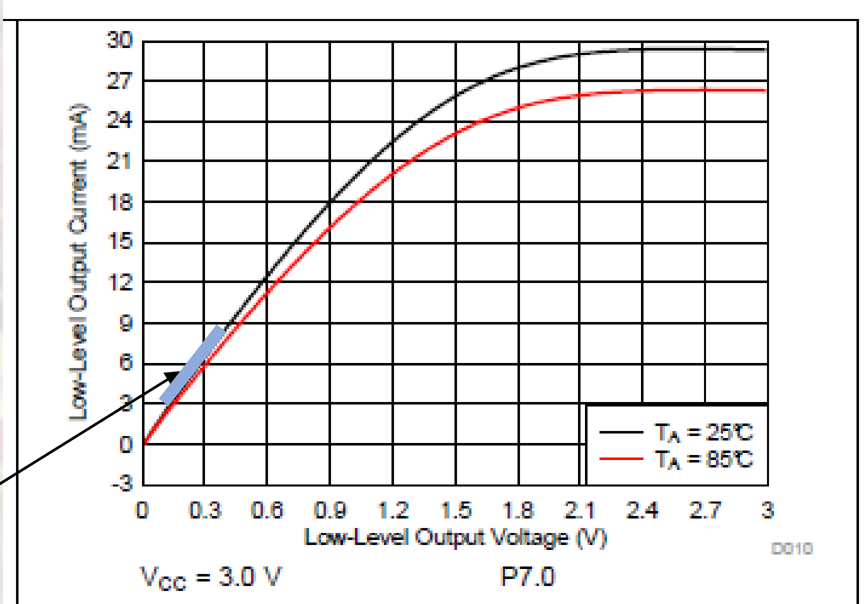


Figure 5-20. Low-Level Output Voltage vs Low-Level Output Current