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Chip Resistor





ANATOMY OF A HIGH RELIABILITY THICK FILM CHIP RESISTOR

Chip Capacitor



System Design

Chip Inductor



Structure and manufacturing process of multilayer chip inductor Manufacturing process Ferrite (dielectric Source material ceramics for RF preparation, blending, applications) sheet forming Terminal electrode Via hole processing contact area Internal electrode printing Internal electrode (forms part of the Layering printed coil pattern) Cutting Via (for inter-layer

connection)

Terminal electrode application Electroplating Measurement, packing Terminal electrode

Sintering

Spiral-shaped layered internal electrode

• Die Bond Pad Lead Frame







• Die Bond Pad







• Die Bond Pad

video



• TO – Transistor Outline





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• PDIP – Plastic Dual Inline Package



SOT – Standard Outline Transistor





SSOP – Shrink Small Outline







• TSOP – Thin Small Outline





• TQFP – Thin Quad Flat





PLCC – Plastic Leaded Chip Carrier



• Ball Grid Array (BGA)

Mold Die Die Attach Au Wire Solder Mask Eutectic Solder Ball Via Rigid Laminate

PBGA Cross Section

• Ball Grid Array (BGA)

PBGA Standard Package Offering:



PBGA (Qualified L2AA/260°C) 2 / 4 / 6 Layer 4-Layer with 1oz (35µm) Internal Cu Planes Single or Multi-Die





• Flip Chip BGA/CSP (Chip Scale Package)



Stacked CSP

Stacked CSP Cross Section 2 Die on 2-Layer Laminate Structure





Stacked CSP Cross Section 2+1 Die on 4-Layer Laminate Structure



Flip Chip Stacked



Package on Package (PoP)





Top package typically integrates high capacity and or combination memory devices through die stacking.



Bottom package typically integrates high density digital logic devices.



Wafer level CSP



CSPnI – Bump on Redistribution



CSPnI – Bump on Repassivation

Stacked Package





• SiP – System in Package





SiP – System in Package



Silicon Through Vias



Micro-Electro-Mechanical Device





• SMT Carriers







- Power Dissipation
 - Power dissipated in a part that is not provided to some load is converted into heat
 - Electrical Analogy
 - Temp (ΔT) <-> Voltage
 - Heat Flow (Q) <-> Current
 - Thermal Resistance (θ) <-> Electrical Resistance
 - Where Q corresponds to power dissipated



Power Dissipation



A regulator has a $\theta = 50^{\circ}$ C/W

If it dissipates 1W in an area where the ambient temperature is 27°C

Its temperature will be: $T_{part} = (Pd \times \theta) + T_A = (1W \times 50^{\circ}C/W) + 27^{\circ}C = 77^{\circ}C$

- Power Dissipation
 - Semiconductor devices are typically characterized by two thermal resistances
 - θ_{JC} thermal resistance from the junction to the case
 - θ_{CA} thermal resistance from the case to the ambient
 - Since most users do not care about the intermediate temperature
 - Often combined to be θ_{JA}

PD

• e.g. $\theta_{JC} = 60^{\circ}C/W$, $\theta_{CA} = 180^{\circ}C/W \rightarrow \theta_{JA} 240^{\circ}C/W$

T_J – Junction Temperature

T_A – Ambient Temperature

 θ_{JA}

Power Dissipation

A regulator has a $\theta_{JA} = 240^{\circ}$ C/W and a $T_{JMax} = 150^{\circ}$ C

If it dissipates 1W in an area where the ambient temperature is 27°C

Its junction temperature will be: $T_J = (P_D \times \theta_{JA}) + T_A = (1W \times 240^{\circ}C/W) + 27^{\circ}C = 267^{\circ}C$

- Power Dissipation
 - We can't impact the θ_{JC} but we can impact θ_{CA}
 - Attach a heat sink
 - Heat Sink
 - By increasing the air-heat interface area heat sinks allow more heat to be dissipated faster
 - Reduce the effective thermal resistance





 $\theta_{CA} = 15 \text{ °C/W}$

Power Dissipation



A regulator has: $\theta_{JC} = 60^{\circ}$ C/W, $\theta_{CA} = 180^{\circ}$ C/W and $T_{JMax} = 150^{\circ}$ C A heat sink is attached with $\theta_{CA} = 15^{\circ}$ C/W

If it dissipates 1W in an area where the ambient temperature is 27°C

Its junction temperature will be: $T_J = (P_D \times (\theta_{JC} + \theta_{CA})) + T_A = (1W \times (60^{\circ}C/W) + 15^{\circ}C/W) + 27^{\circ}C = 102^{\circ}C$