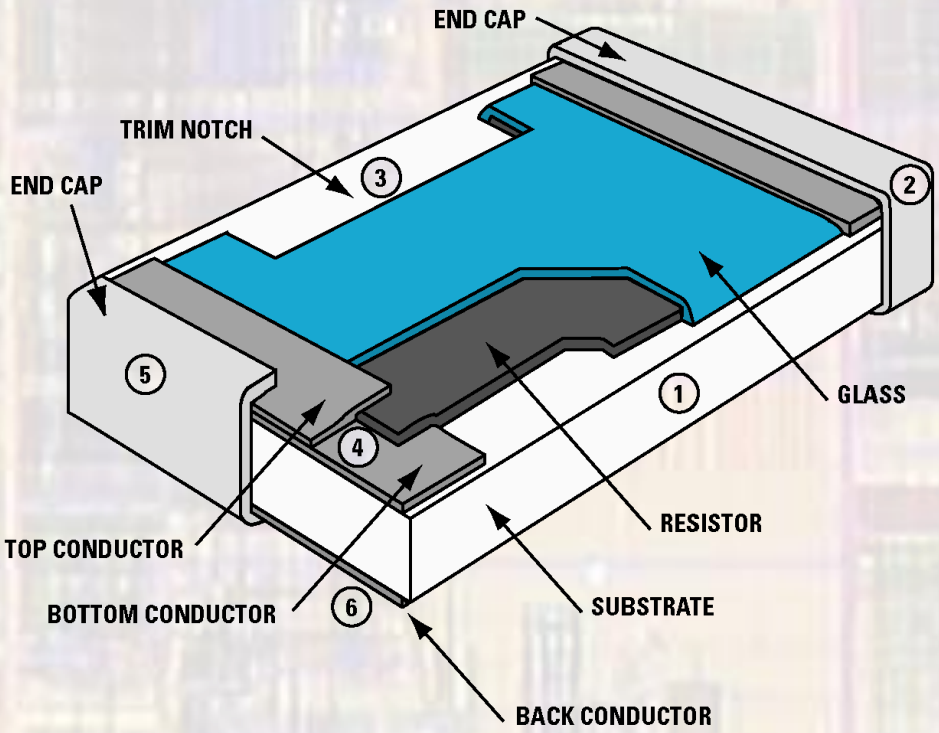
Packaging

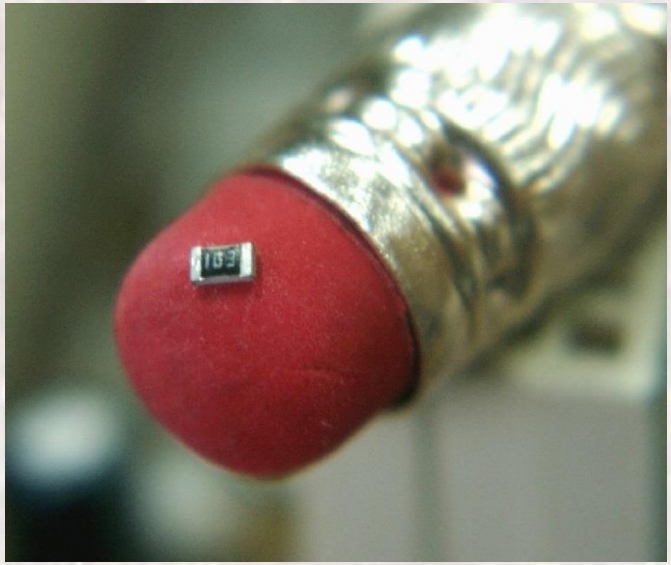
Last updated 6/17/19

Packaging

- Chip Resistor

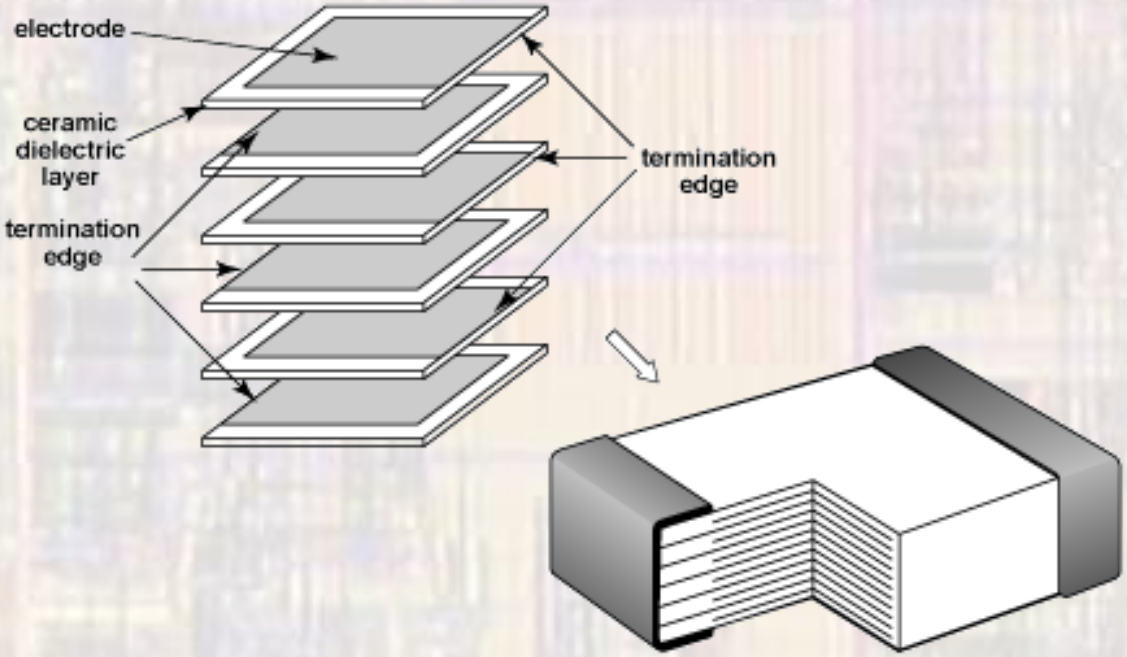


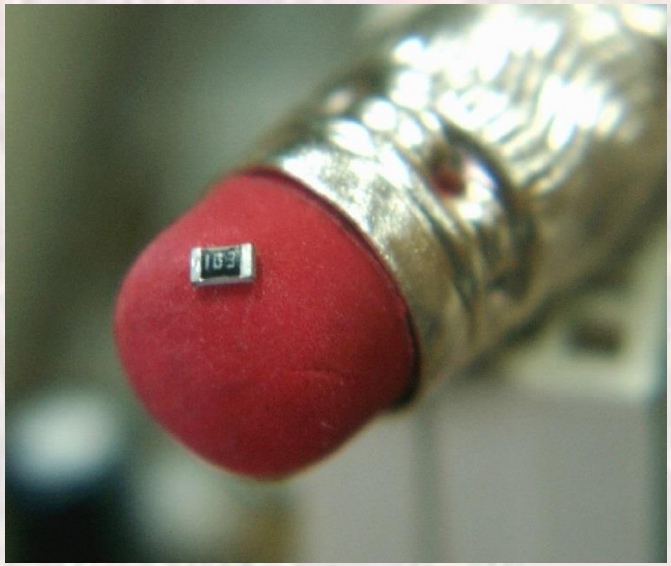
ANATOMY OF A HIGH RELIABILITY THICK FILM CHIP RESISTOR

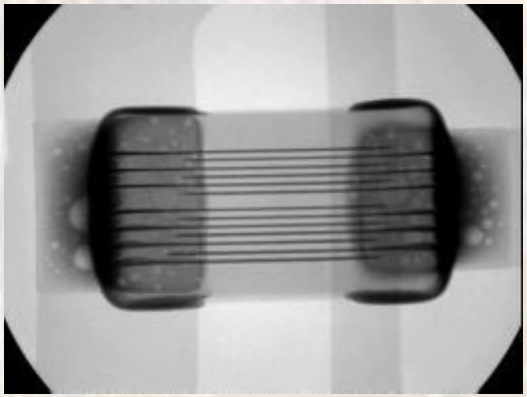


Packaging

- Chip Capacitor

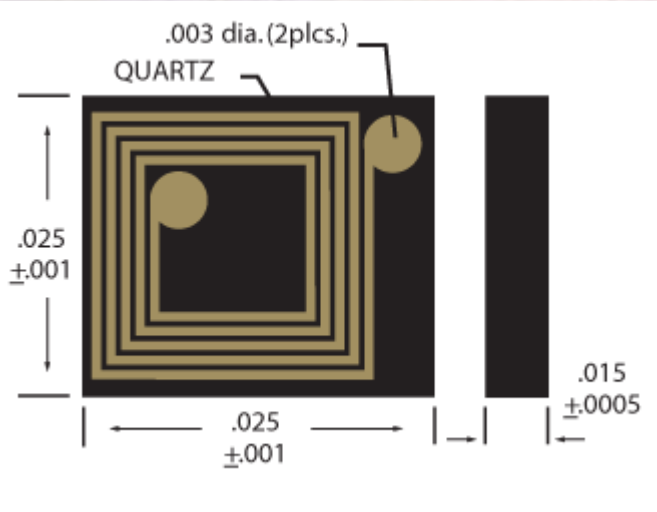


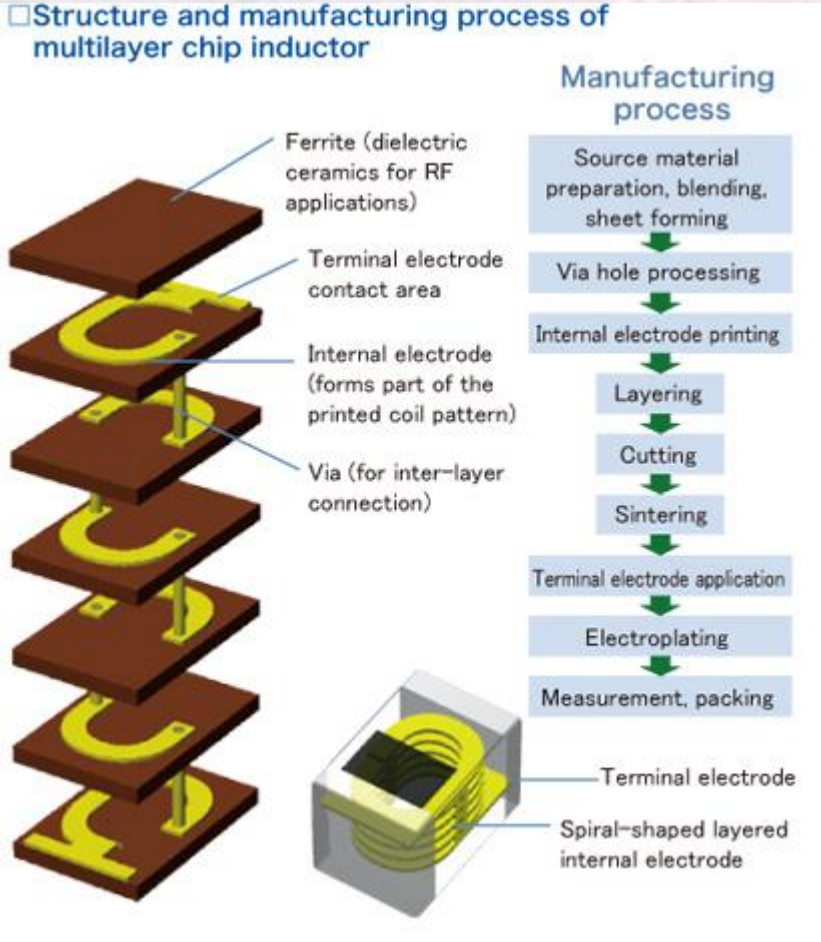




System Design

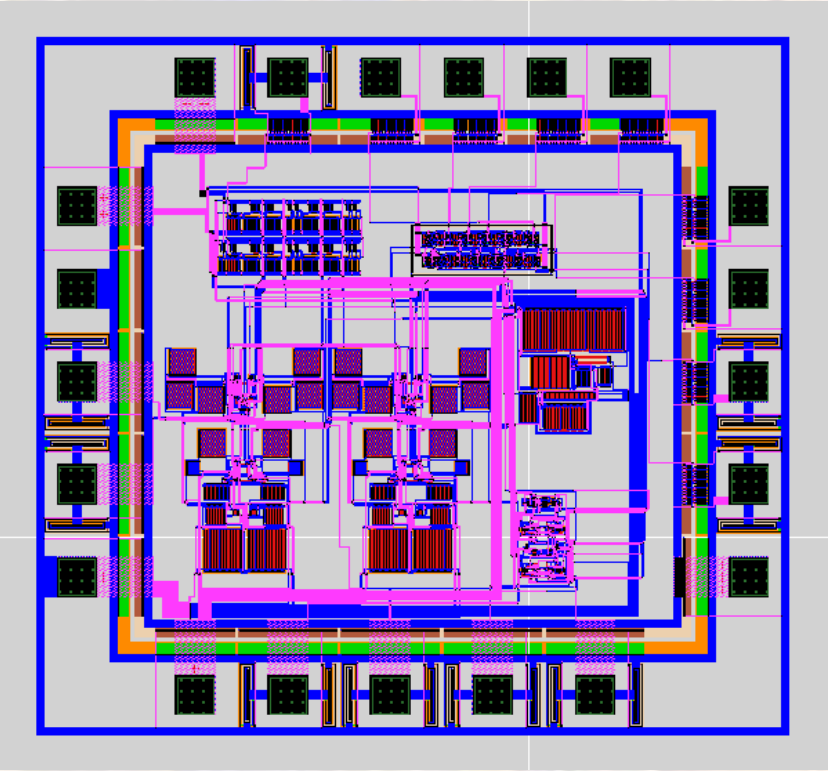
- Chip Inductor

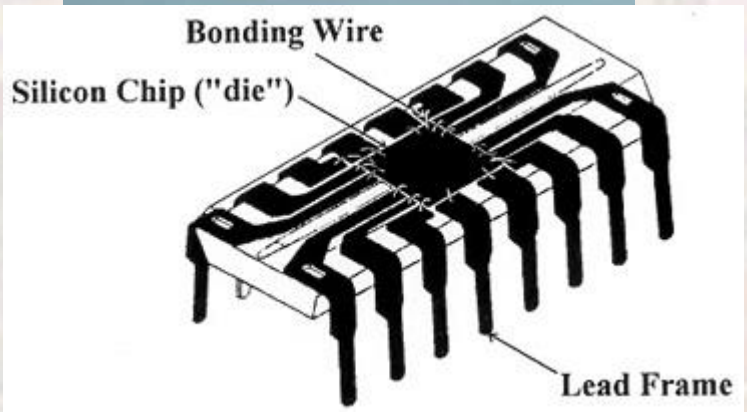




Packaging

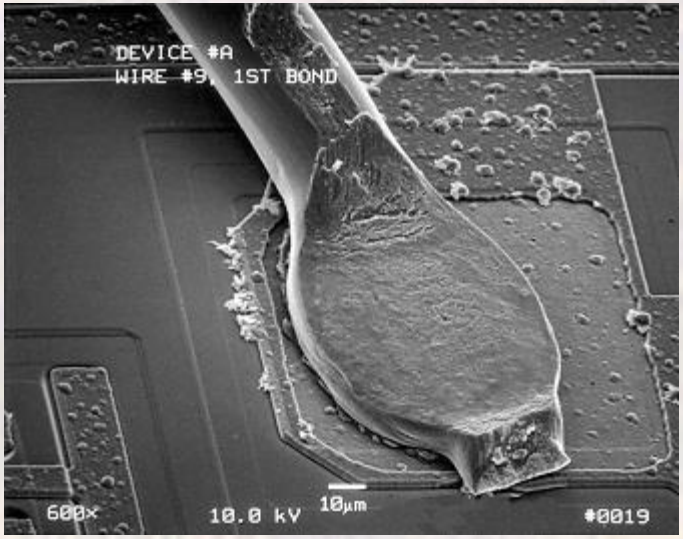
- Die Bond Pad
  Lead Frame

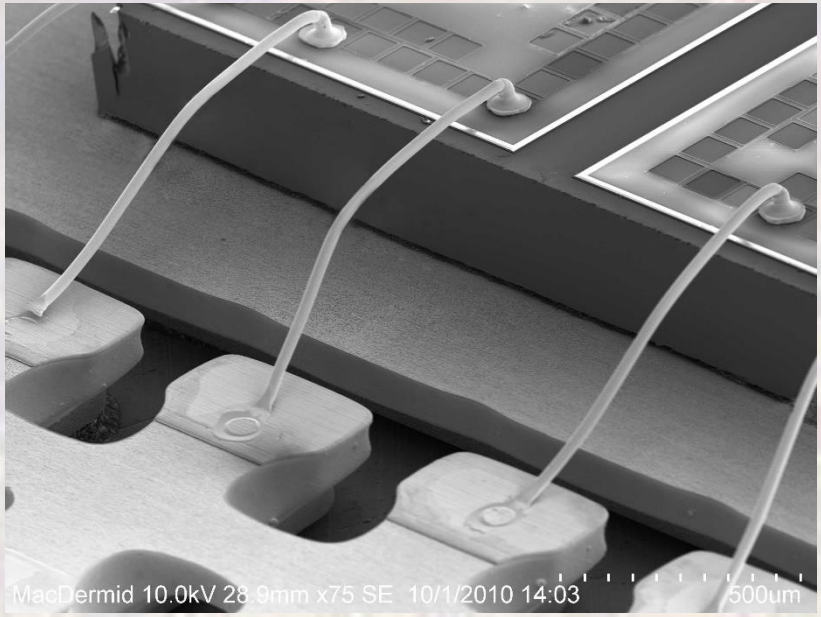


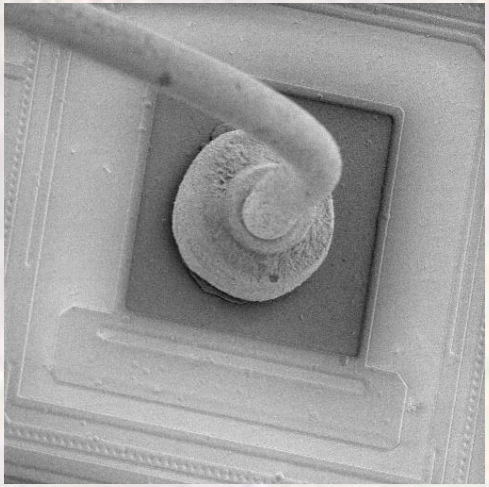


Packaging

- Die Bond Pad







Packaging

- Die Bond Pad

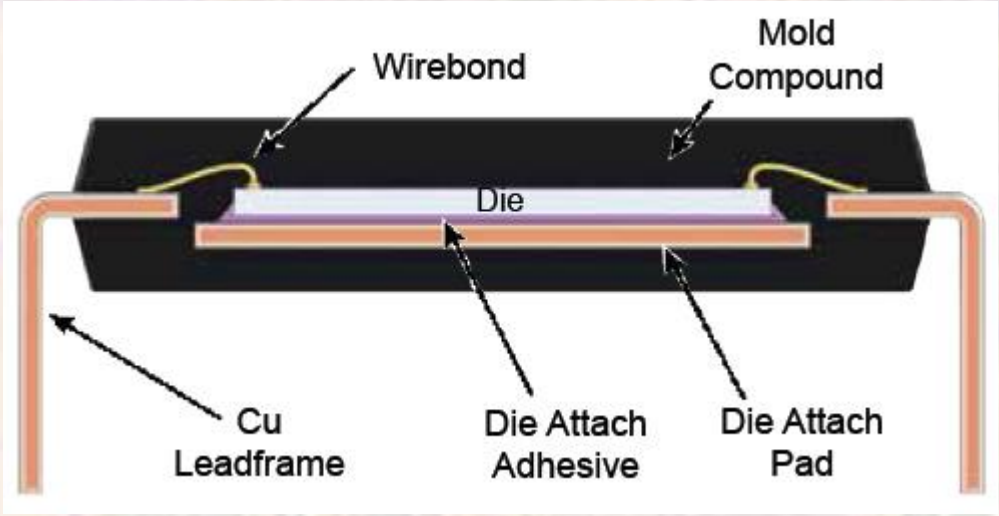
video

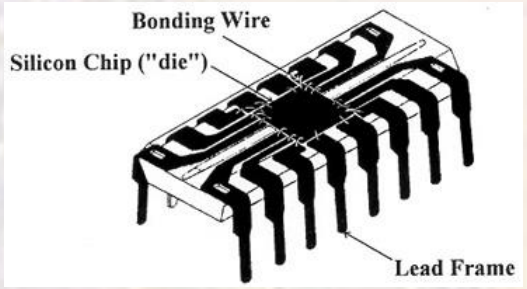
Packaging

- TO – Transistor Outline

Packaging

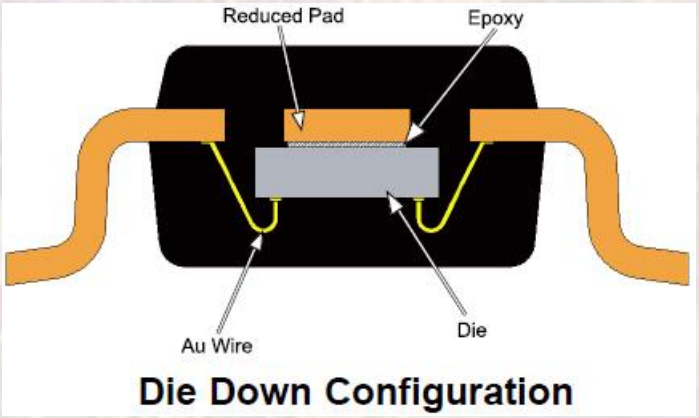
- PDIP – Plastic Dual Inline Package





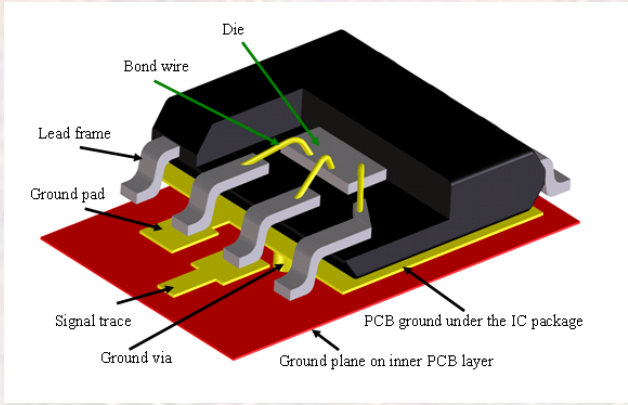
Packaging

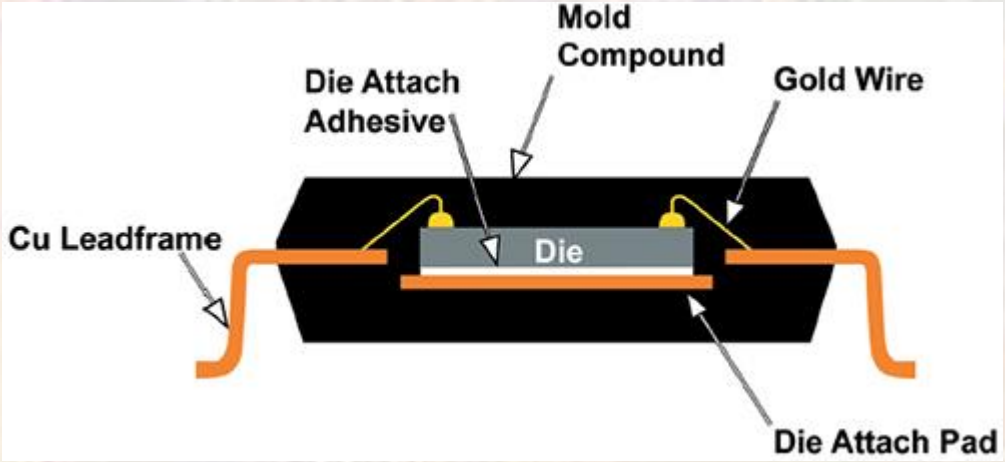
- SOT – Standard Outline Transistor



Packaging

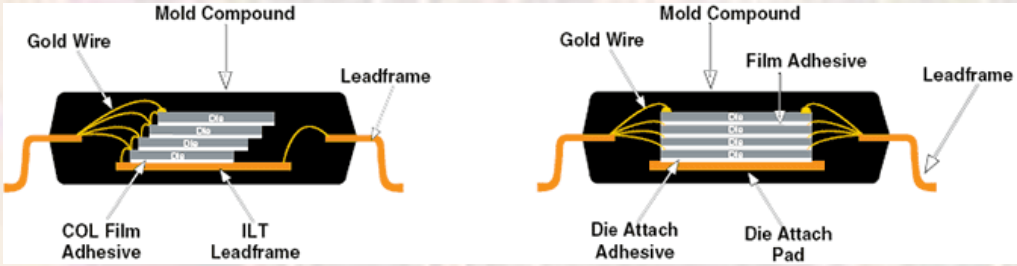
- SSOP – Shrink Small Outline





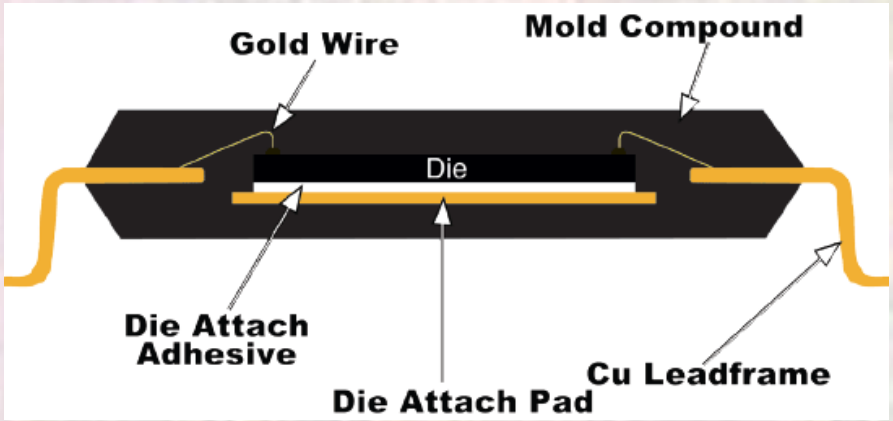
Packaging

- TSOP – Thin Small Outline



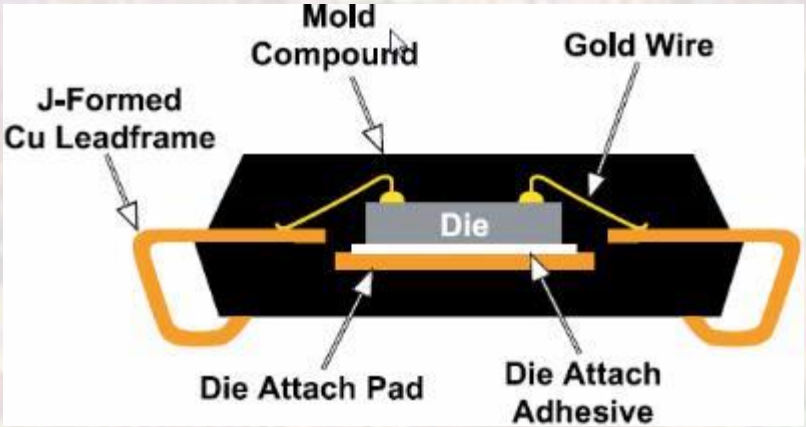
Packaging

- TQFP – Thin Quad Flat



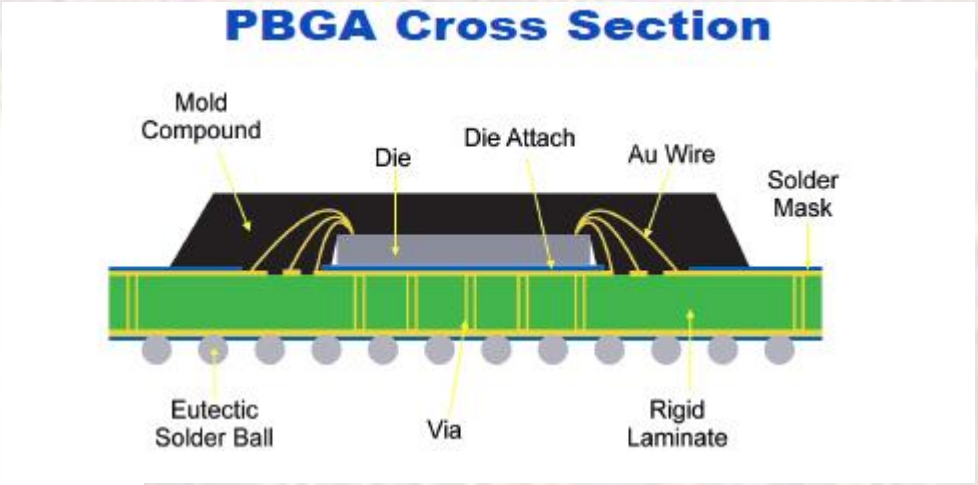
Packaging

- PLCC – Plastic Leaded Chip Carrier



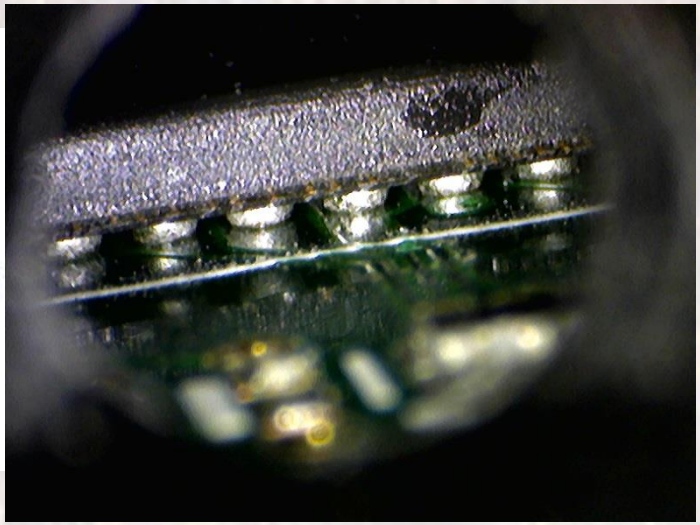
Packaging

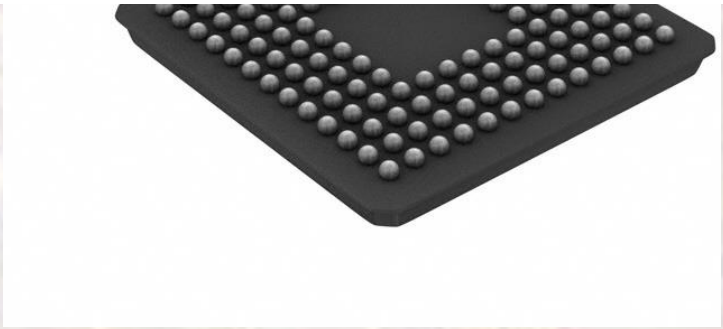
- Ball Grid Array (BGA)



Packaging

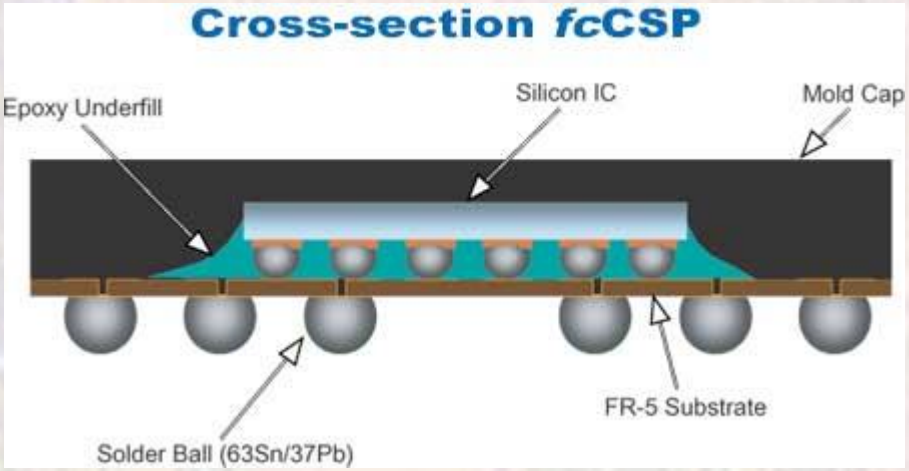
- Ball Grid Array (BGA)





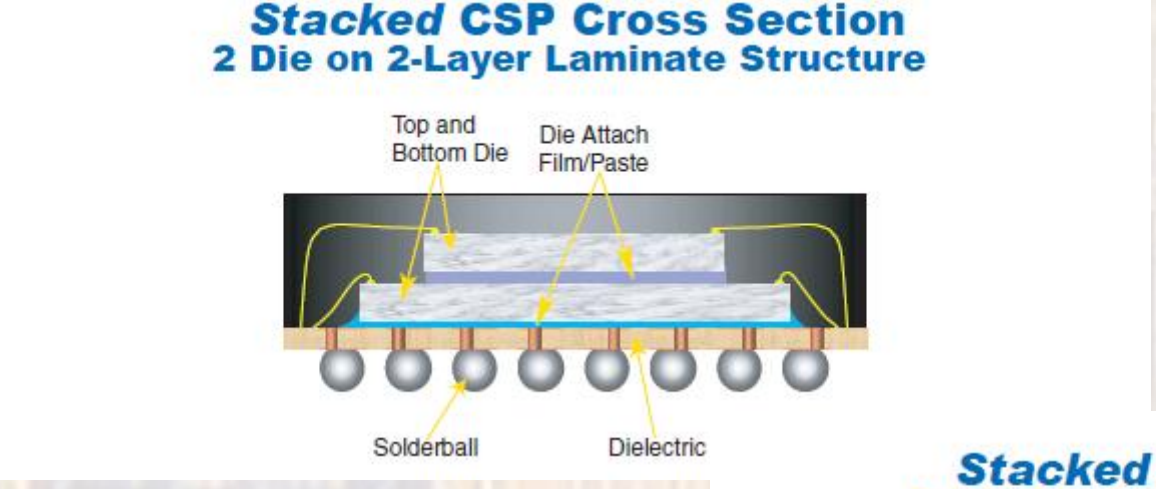
Packaging

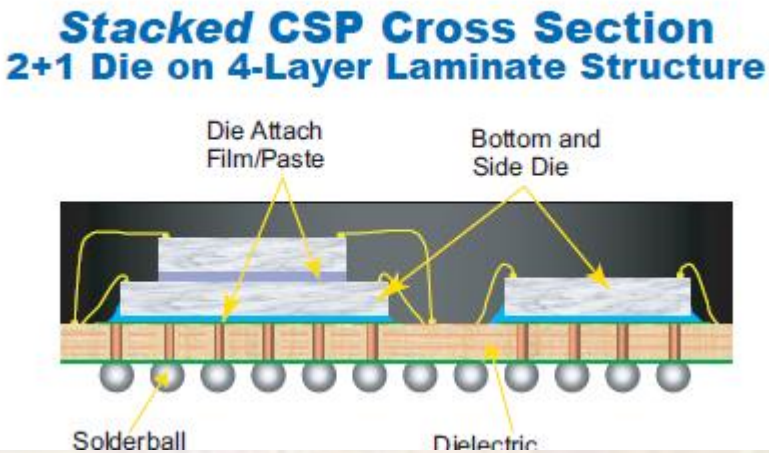
- Flip Chip BGA/CSP (Chip Scale Package)



Packaging

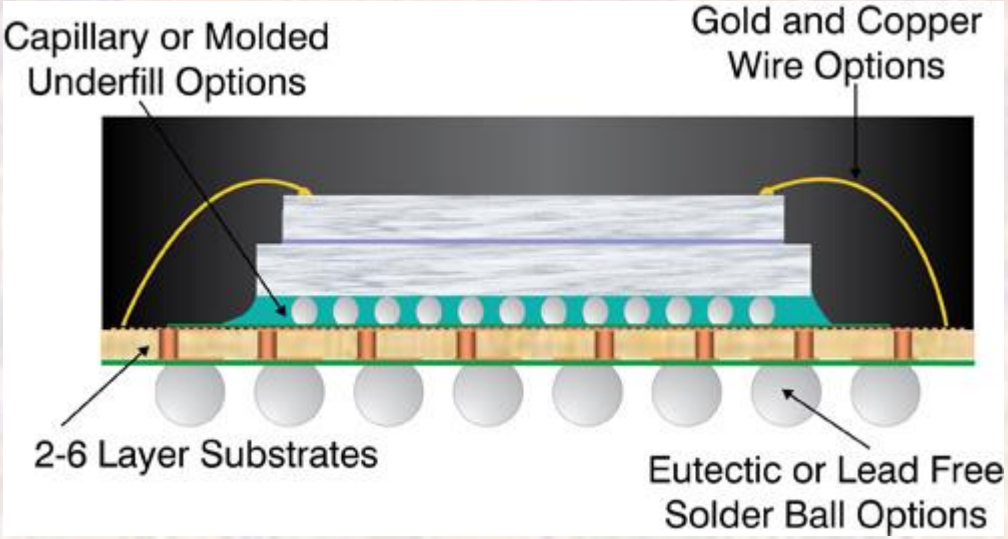
- Stacked CSP





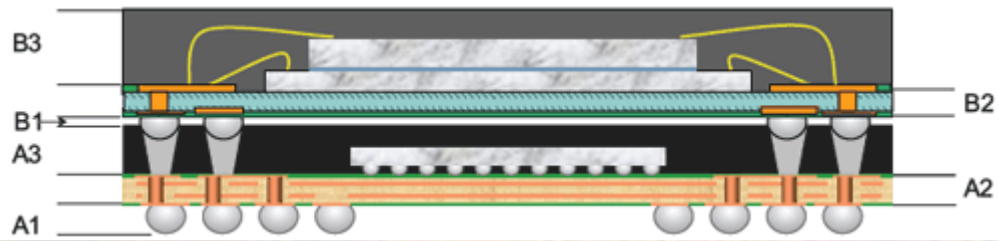
Packaging

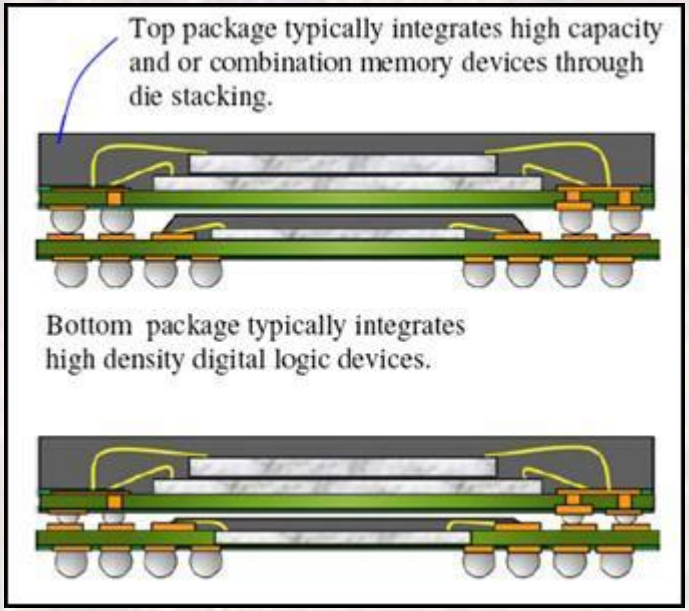
- Flip Chip Stacked



Packaging

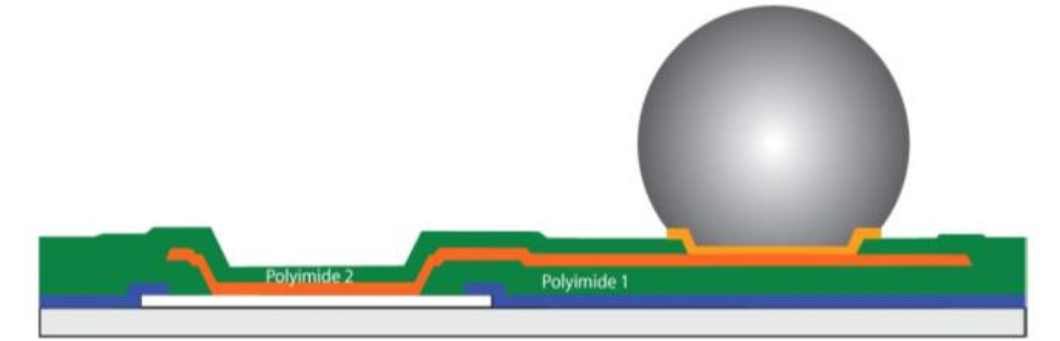
- Package on Package (PoP)



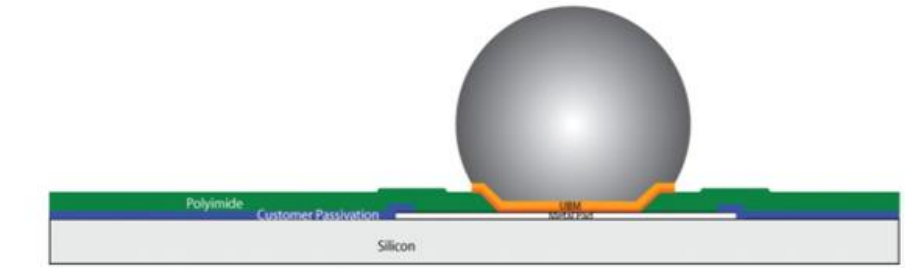


Packaging

- Wafer level CSP



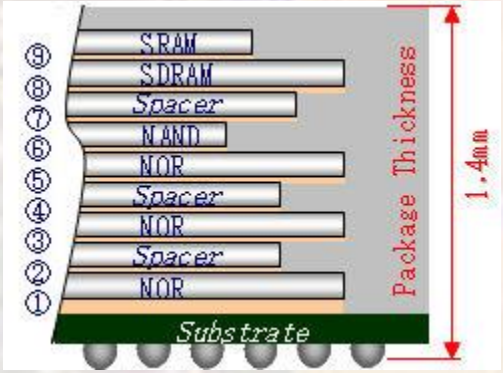
CSPnl – Bump on Redistribution

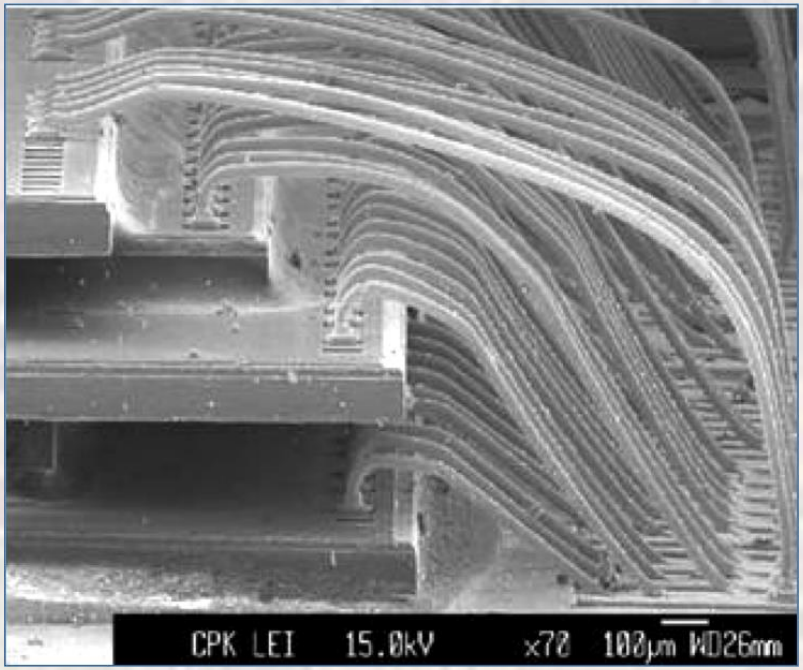


CSPnl – Bump on Repassivation

Packaging

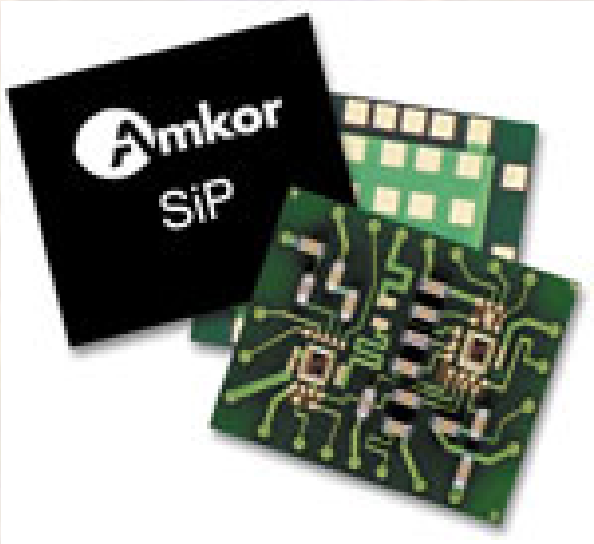
- Stacked Package

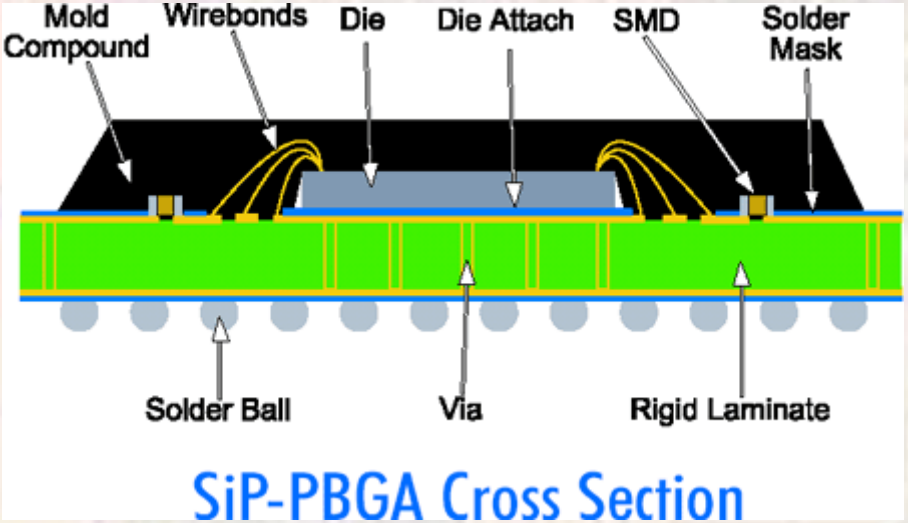




Packaging

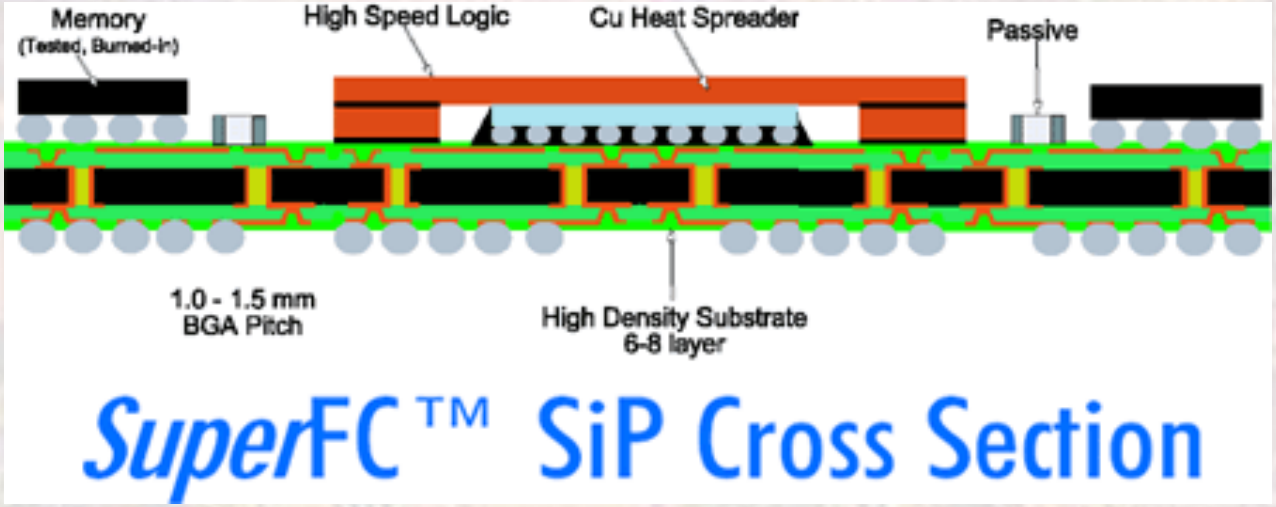
- SiP – System in Package





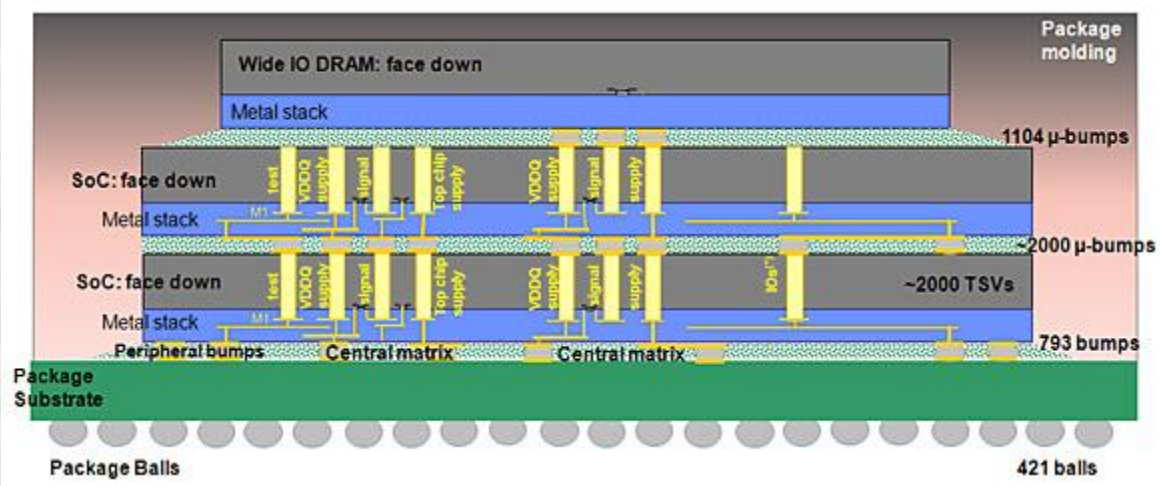
Packaging

- SiP – System in Package



Packaging

- Silicon Through Vias

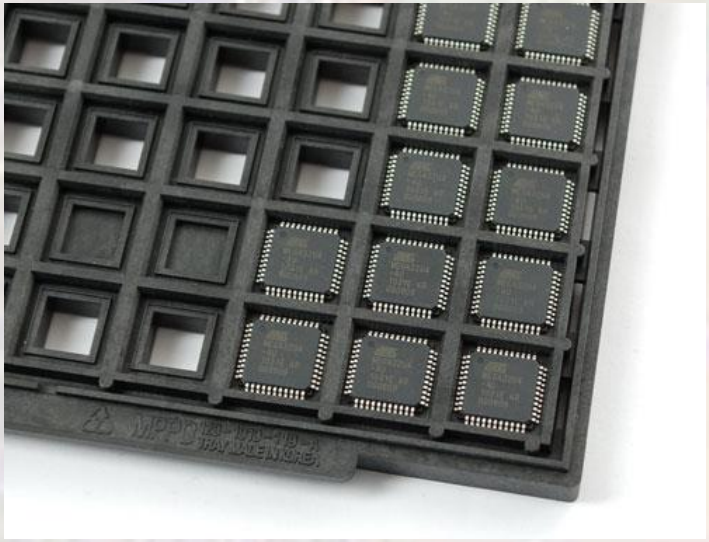


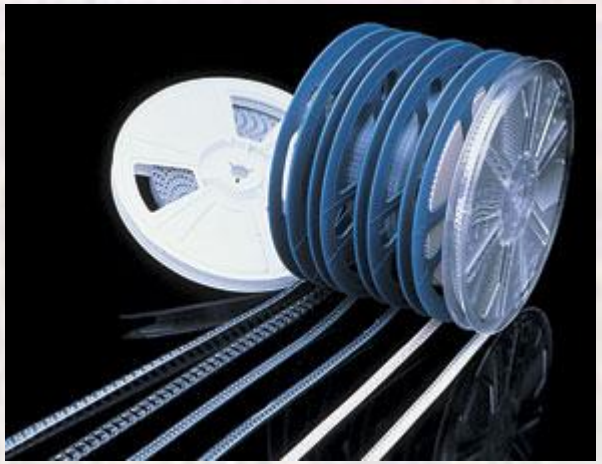
Packaging

- Micro-Electro-Mechanical Device

Packaging

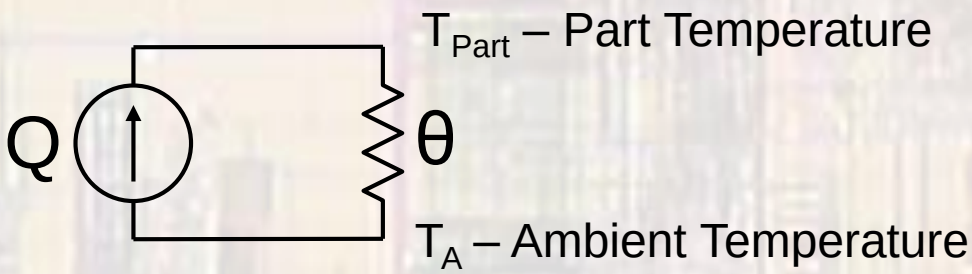
- SMT Carriers





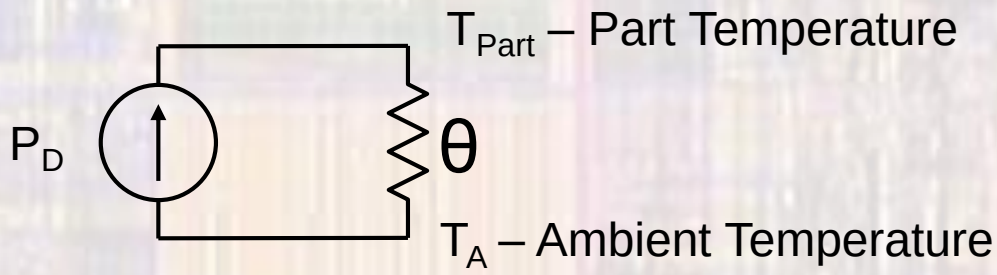
Packaging

- Power Dissipation
  - Power dissipated in a part that is not provided to some load is converted into heat
    - Electrical Analogy
      - Temp (ΔT) <-> Voltage
      - Heat Flow (Q) <-> Current
      - Thermal Resistance (θ) <-> Electrical Resistance
      - Where Q corresponds to power dissipated



Packaging

- Power Dissipation



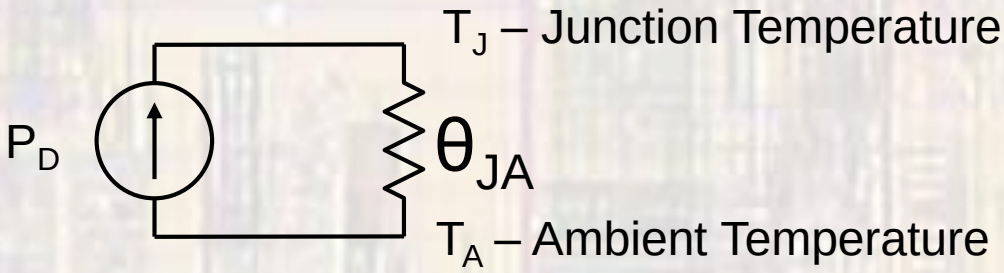
A regulator has a θ = 50°C/W

If it dissipates 1W in an area where the ambient temperature is 27°C

Its temperature will be: T_{part} = (Pd x θ) + T_A =
(1W x 50°C/W) + 27°C = 77°C

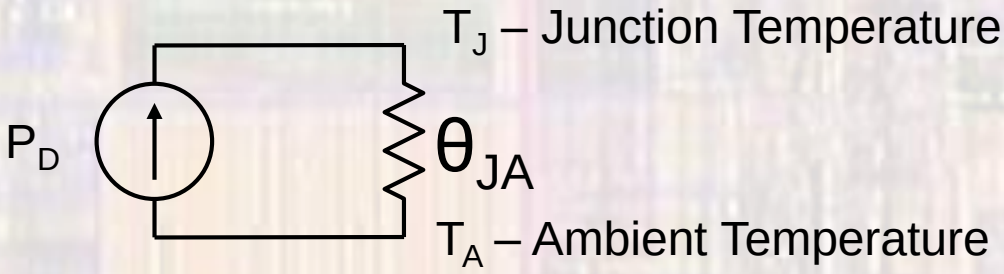
Packaging

- Power Dissipation
  - Semiconductor devices are typically characterized by two thermal resistances
    - θ_{JC} – thermal resistance from the junction to the case
    - θ_{CA} – thermal resistance from the case to the ambient
    - Since most users do not care about the intermediate temperature
      - Often combined to be θ_{JA}
      - e.g. θ_{JC} = 60°C/W, θ_{CA} = 180°C/W → θ_{JA} 240°C/W



Packaging

- Power Dissipation



A regulator has a θ_{JA} = 240°C/W and a T_{JMax} = 150°C

If it dissipates 1W in an area where the ambient temperature is 27°C

Its junction temperature will be: $T_J = (P_D \times \theta_{JA}) + T_A =$
$(1W \times 240°C/W) + 27°C =$ 267°C

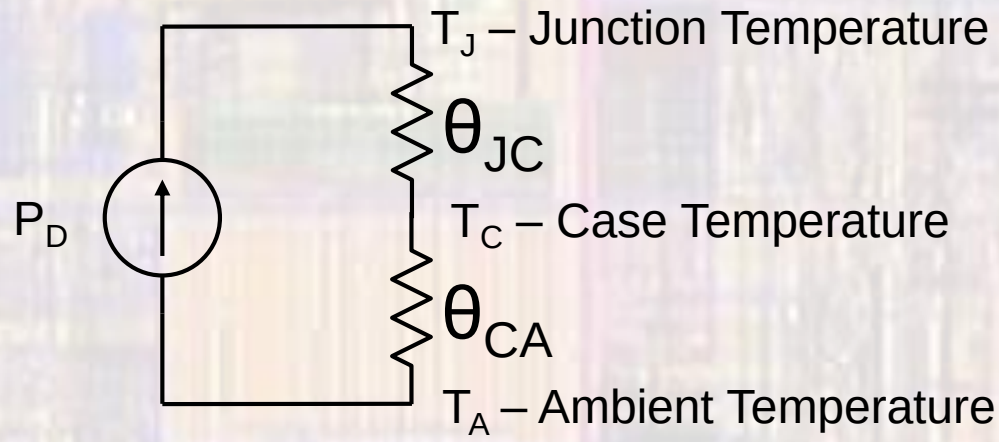
Packaging

- Power Dissipation
  - We can't impact the θ_{JC} but we can impact θ_{CA}
    - Attach a heat sink
  - Heat Sink
    - By increasing the air–heat interface area heat sinks allow more heat to be dissipated faster
    - Reduce the effective thermal resistance

θ_{CA} = 15 °C/W

Packaging

- Power Dissipation



A regulator has: θ_{JC} = 60°C/W, θ_{CA} = 180°C/W and T_{JMax} = 150°C
A heat sink is attached with θ_{CA} = 15°C/W

If it dissipates 1W in an area where the ambient temperature is 27°C

Its junction temperature will be: $T_J = (P_D \times (\theta_{JC} + \theta_{CA})) + T_A =$
$(1W \times (60°C/W + 15°C/W) + 27°C = 102°C$