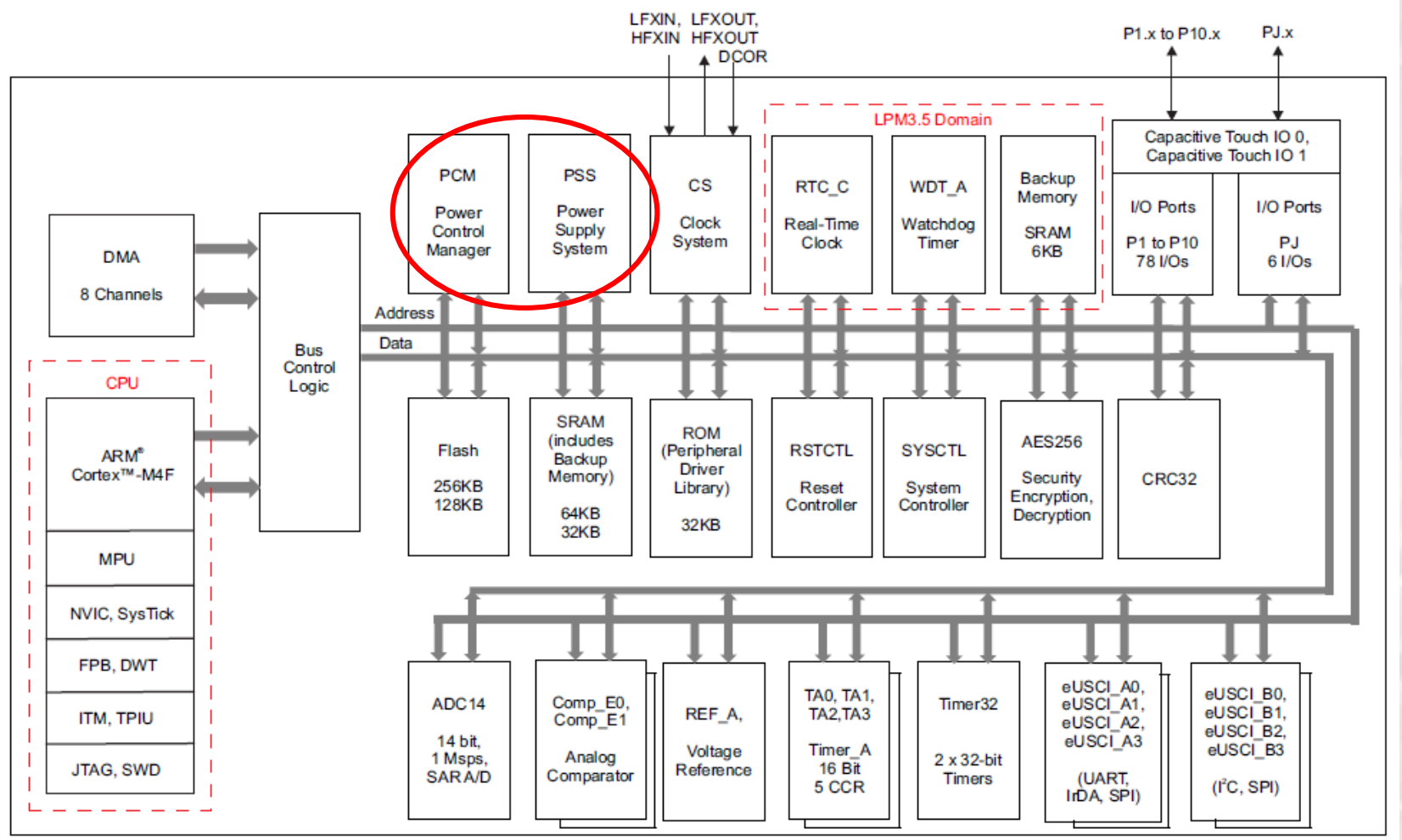
Power System

Last updated 7/8/19

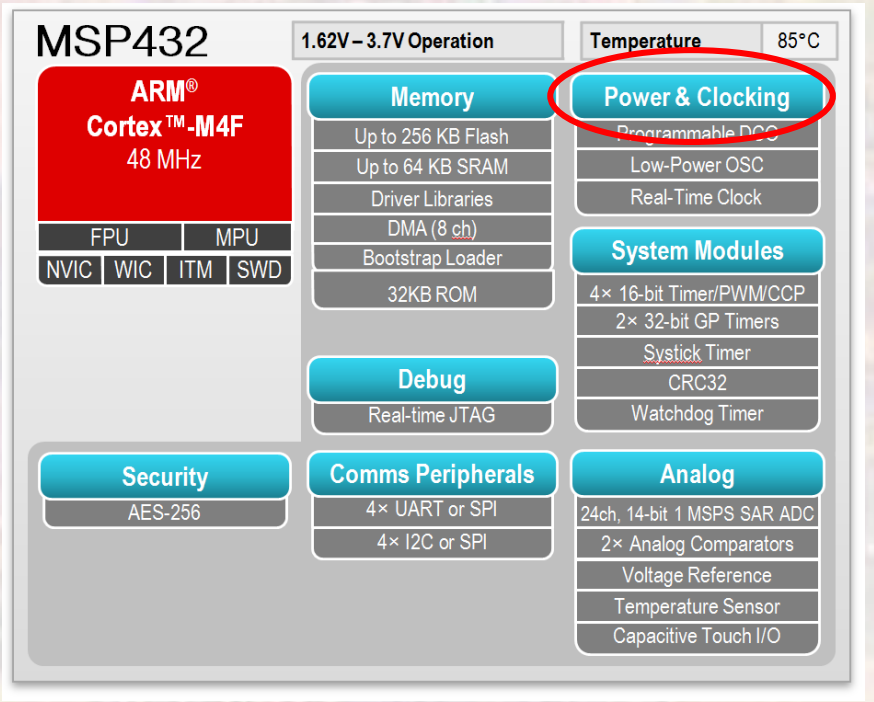
Power System

- MSP432 Power Systems



Power System

- MSP432 Power System
  - Power Supply System
    - 1.62V to 3.7V
    - Power status
    - Internal Core voltage generation
      - Allows for performance variations
  - Power Control Manager
    - Provides the necessary voltages to meet performance requirements
    - Collects inputs from various parts of the processor
      - Direct changes to power mode
      - Wake-up and interrupt events
      - Reset events
      - Debug



Power System

- MSP432 Power System
  - Supplies
    - VCC (DVCC)
      - External
      - Primary chip supply voltage
      - Supplies the I/Os and VCORE regulator
    - VCORE
      - Internal – programmable
      - Integrated voltage regulator to generate core voltage
      - Supplies the CPU, memories, and digital modules,
    - AVCC
      - External
      - Supplies the analog modules

Power System

- MSP432 Power System
  - Supply Voltage Supervisor/Monitor High Side (SVSMH)
    - High Side – Input to the chip – Vcc
    - Detects when the high side voltage drops below an acceptable level
      - Level required to maintain performance (clock frequency)
    - Supervisor mode – causes reset
    - Monitor mode – sets interrupt flag

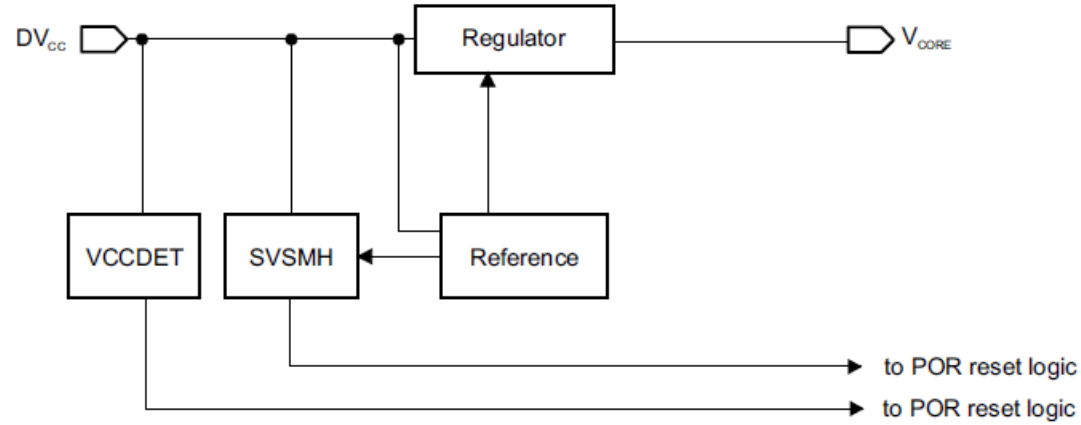


Figure 6-1. PSS Block Diagram

Power System

- MSP432 Power System
  - Supply Voltage Supervisor/Monitor High Side (SVSMH)
    - SVMHOUT – indicates the state of the monitor
    - SVSMH – Thresholds
      - Vcc rising threshold
      - Vcc falling threshold

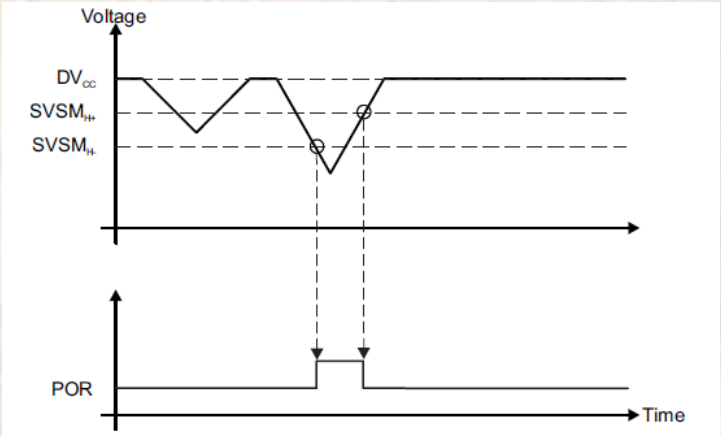


Figure 6-2. Supply Voltage Failure and Resulting PSS Action

Power System

- MSP432 Power System
  - Registers

Table 6-1. PSS Registers

Offset	Acronym	Register Name	Section
00h	PSSKEY	Key Register	Section 6.3.1
04h	PSSCTL0	Control 0 Register	Section 6.3.2
34h	PSSIE	Interrupt Enable Register	Section 6.3.3
38h	PSSIFG	Interrupt Flag Register	Section 6.3.4
3Ch	PSSCLRIFG	Clear Interrupt Flag Register	Section 6.3.5

PSS->KEY

…

PSS->CLRIFG

Power System

- MSP432 Power System
  - Key Register

Figure 6-4. PSSKEY Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
PSSKEY							
rw-1	rw-0	rw-1	rw-0	rw-0	rw-1	rw-0	rw-1
7	6	5	4	3	2	1	0
PSSKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0

Table 6-2. PSSKEY Register Description

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	Reserved. Always read 0.
15-0	PSSKEY	RW	A596h	PSS key. Always read as A596h. Must be written with 695Ah to unlock the PSS registers for writing. Any other write value locks the PSS registers. Note: Registers can be read even when locked.

Power System

- MSP432 Power System
  - Control Register

Figure 6-5. PSSCTL0 Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved		Reserved		Reserved	DCDC_FORCE	Reserved	
r-0	r-0	rw-1	rw-0	r-0	rw-0	r-0	r-0
7	6	5	4	3	2	1	0
SVMHOUTPOL AL	SVMHOE	SVSMHTH			SVSMHS	SVSMHLP	SVSMHOFF
rw-0	rw-0	rw-0 (1)	rw-0 (1)	rw-0 (1)	rw-0	rw-0 (1)	rw-0 (1)

Power System

- MSP432 Power System
  - Control Register

Table 6-3. PSSCTL0 Register Description

Bit	Field	Type	Reset	Description
31-14	Reserved	R	0h	Reserved. Always reads as 0.
13-12	Reserved	RW	2h	Internal configuration. Changing this may cause device to reset during core voltage level transitions.
11	Reserved	R	0h	Reserved. Always reads as 0.
10	DCDC_FORCE	RW	0h	Force DC-DC regulator operation. Refer to Power Control Manager (PCM) chapter for details about this feature. 0b = DC-DC regulator operation not forced. Automatic fail-safe mechanism switches the core voltage regulator from DC-DC to LDO when the supply voltage falls below the minimum supply voltage necessary for DC-DC operation. 1b = DC-DC regulator operation forced. Automatic fail-safe mechanism is disabled and device continues to operate out of DC-DC regulator.
9-8	Reserved	R	0h	Reserved. Always reads as 0.
7	SVMHOUTPOLAL	RW	0h	SVMHOUT pin polarity active low. 0b = SVMHOUT is active high. An error condition is signaled by a 1 at the SVMHOUT pin. 1b = SVMHOUT is active low. An error condition is signaled by a 0 at the SVMHOUT pin.
6	SVMHOE	RW	0h	SVSM high-side output enable 0b = SVSMHIFG bit is not output. 1b = SVSMHIFG bit is output to the device SVMHOUT pin. The device-specific port logic must be configured accordingly.
5-3	SVSMHTH	RW	0h	SVSM high-side reset voltage level. If DVCC falls short of the SVSMH voltage level selected by SVSMHTH, a reset is triggered (if SVSMHOFF = 0 and SVSMHS = 0) or interrupt is triggered (if SVSMHOFF = 0 and SVSMHS = 1). The voltage levels are defined in the device-specific data sheet.

Power System

- MSP432 Power System
  - Control Register - SVSMHTH values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SVSMH}	$SVSM_H$ current consumption, low-power mode	SVSMHOFF = 0, SVSMHLP = 1		200	400	nA
	$SVSM_H$ current consumption, high-performance mode	SVSMHOFF = 0, SVSMHLP = 0		7	10	µA
$V_{SVSMH-,HP}$	$SVSM_H$ threshold level during high-performance mode (falling DV_{CC})	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s)	2.0	2.06	2.12	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s)	2.2	2.26	2.32	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s)	2.4	2.47	2.54	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s)	2.7	2.79	2.88	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s)	2.9	3.0	3.1	
$V_{SVSMH+,HP}$	$SVSM_H$ threshold leve, high-performance mode (rising DV_{CC})	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s)	2.02	2.07	2.14	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s)	2.22	2.27	2.34	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s)	2.42	2.48	2.56	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s)	2.72	2.8	2.9	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s)	2.92	3.01	3.12	

Power System

- MSP432 Power System
  - Control Register

Bit	Field	Type	Reset	Description
2	SVSMHS	RW	0h	Supply supervisor or monitor selection for the high-side 0b = Configure as SVSH 1b = Configure as SVMH
1	SVSMHLP	RW	0h	SVSM high-side low power normal performance mode 0b = Full performance mode. See the device-specific data sheet for response times. 1b = Low power normal performance mode in LPM3, LPM4, and LPMx.5, full performance in all other modes. See the device-specific data sheet for response times.
0	SVSMHOFF	RW	0h	SVSM high-side off 0b = The SVSMH is on. 1b = The SVSMH is off. Note: If the SVSMH is kept disabled in Active Mode, and is enabled before entering a low power mode of the device (LPM3/LPM4/LPMx.5) care should be taken that sufficient time has elapsed since enabling of the module until entry into the device low power mode to allow for successful wakeup of SVSMH module as per 'SVSMH on/off delay time' spec in respective device datasheet. Otherwise, SVSMH may trip, causing device to get a Reset and wakeup from the Low Power Mode. Note: If the SVSMH is disabled when in LPM4.5, and the supply goes below default SVSMH limits, the device may get an SVSMH-triggered Reset if woken up while the supply is low. Note: If SVSMH is disabled by setting this bit, and immediately enabled due to RSTn pin reset within 200ns, the reset source may get elevated to a Reset High side due to insufficient power down time allowed for SVSMH.

Power System

- MSP432 Power System
  - Interrupt Enable Register

Figure 6-6. PSSIE Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved						SVSMHIE	Reserved
r0	r0	r0	r0	r0	r0	rw-0	r-0

Table 6-4. PSSIE Register Description

Bit	Field	Type	Reset	Description
31-2	Reserved	R	0h	Reserved. Always read 0.
1	SVSMHIE	RW	0h	High-side SVSM interrupt enable, when set as a monitor (SVSMHS = 1). 0b = Interrupt disabled 1b = Interrupt enabled Make sure that the SVSMHIFG bit is cleared before enabling interrupt. Otherwise an unexpected NMI may be seen due to an earlier dip in DVCC while interrupt was disabled.
0	Reserved	R	0h	Reserved. Always read 0.

Power System

- MSP432 Power System
  - Flag Register

Figure 6-7. PSSIFG Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved						SVSMHIFG	Reserved
r0	r0	r0	r0	r0	r-0	r-0	r-0

Table 6-5. PSSIFG Register Description

Bit	Field	Type	Reset	Description
31-2	Reserved	R	0h	Reserved. Always read 0.
1	SVSMHIFG	R	0h	High-side SVSM interrupt flag. SVSMH = 0 (supervisor mode): The SVSMHIFG interrupt flag is not active. SVSMH = 1 (monitor mode): The SVSMHIFG interrupt flag is set if DVCC drops below the SVSMH power-down level and an interrupt is generated. The bit is cleared by software. 0b = No interrupt pending 1b = Interrupt due to SVSMH The interrupts generated by the PSS can be classified either as NMI or regular interrupts at the device level. For more details, refer to the system control section in the appropriate device datasheet.
0	Reserved	R	0h	Reserved. Always read 0.

Power System

- MSP432 Power System
  - Clear Flag Register

Figure 6-8. PSSCLRIFG Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved						CLRSVSMHIFG	Reserved
r0	r0	r0	r0	r0	r0	w-0	r-0

Table 6-6. PSSCLRIFG Register Description

Bit	Field	Type	Reset	Description
31-2	Reserved	R	0h	Reserved. Always read 0.
1	CLRSVSMHIFG	W	0h	SVSMH clear interrupt flag 0b = No effect 1b = Clear pending interrupt flag
0	Reserved	R	0h	Reserved. Always read 0.

Power System

- MSP432 Power Control Manager
  - Provides the necessary voltages to meet performance requirements
  - Collects inputs from various parts of the processor
    - Direct changes to power mode
    - Wake-up and interrupt events
    - Reset events
    - Debug

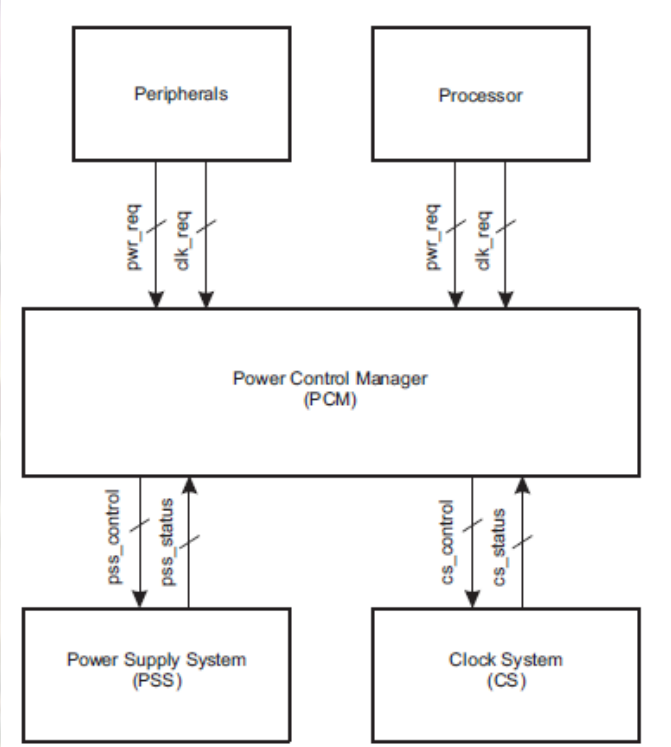


Figure 7-1. Power Control Manager Interaction

Power System

- MSP432 Power Control Manager
  - Controls the VCORE regulator
    - Provide minimum voltage necessary to meet performance requirements
  - MSP432 has 2 choices for the regulator
    - Linear regulator(LDO)
      - Few parts, less efficient
      - Default mode
    - DCDC
      - More parts, more efficient

Power System

- MSP432 Power Control Manager
  - Power Modes – Active Mode (AM)
    - CPU can be active
    - 2 VCORE levels, 3 modes each
    - VCORE1 – highest VCORE level
      - Supports clock frequencies up to 48MHz
    - VCORE 0 – lower VCORE level
      - Supports clock frequencies up to 24MHz
    - LDO mode
    - DCDC mode
    - LF mode
      - Clock frequency limited to 128KHz

Power System

- MSP432 Power Control Manager
  - Power Modes – Active Mode (AM)
    - AM_LDO_VCORE0
    - AM_LDO_VCORE1
    - AM_DCDC_VCORE0
    - AM_DCDC_VCORE1
    - AM_LF_VCORE0
    - AM_LF_VCORE1

Power System

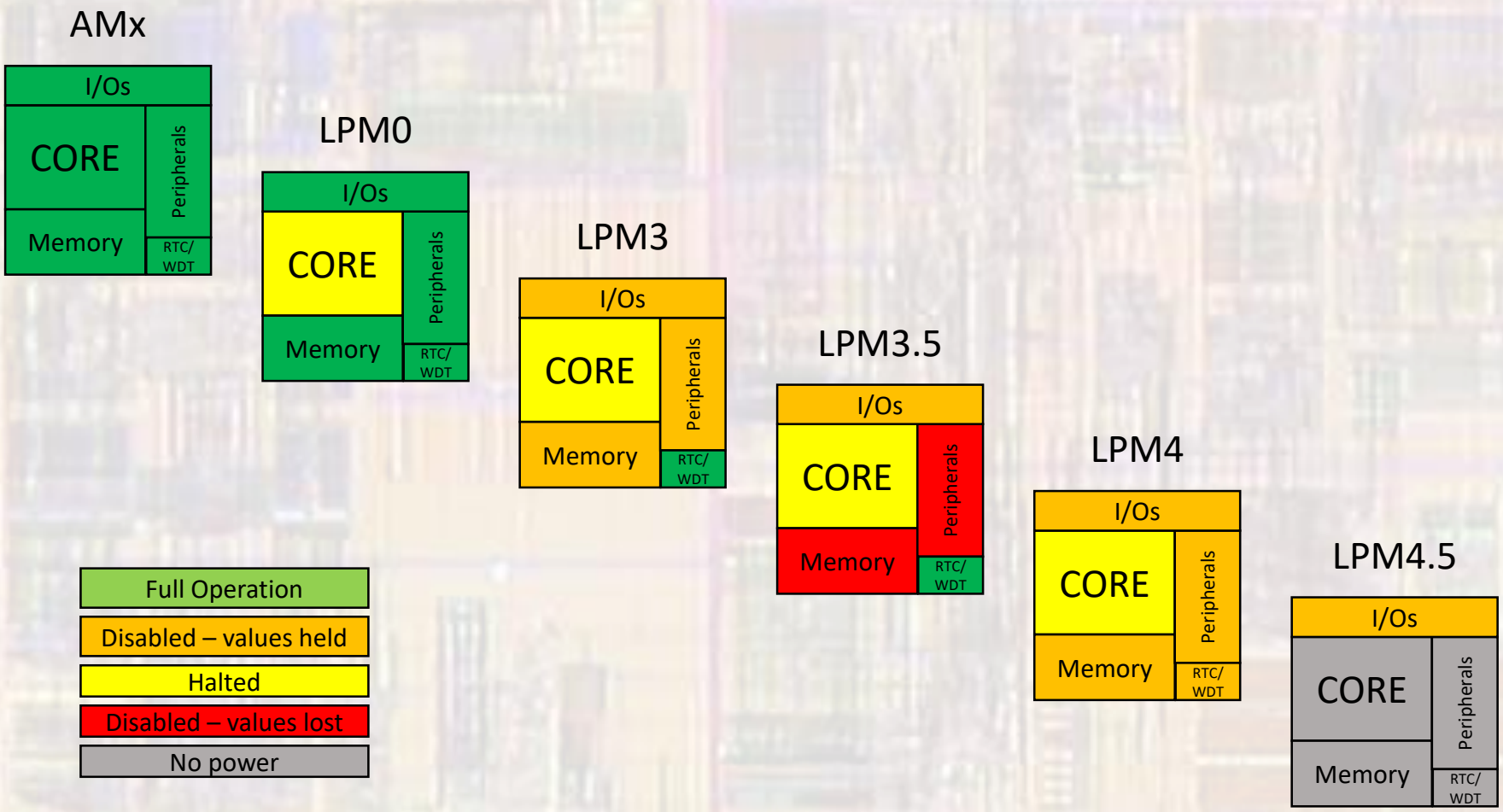
- MSP432 Power Control Manager
  - Power Modes – Low Power Mode (LPM)
    - LPM0
      - Processor is halted
      - All peripherals, memories, registers, I/Os enabled
      - Accessible from any of the Active Modes
    - LPM3, LPM4
      - Processor is halted
      - Memories, registers and I/Os retained
      - Accessible only when operating at 32KHz
      - LPM3 – only RTC and WDT enabled
      - LPM4 – no peripherals enabled

Power System

- MSP432 Power Control Manager
  - Power Modes – Low Power Mode (LPM)
    - LPM3.5
      - Processor halted
      - RTC and WDT enabled
      - All other peripherals disabled and registers NOT retained
      - SRAM not retained
      - I/Os latched
    - LPM4.5
      - VCORE shut off – no internal power
      - Nothing retained except I/Os

Power System

- MSP432 Power Control Manager



Power System

- MSP432 Power Control Manager

Table 7-1. Power Modes Summary

Power Mode	Operating State	Features and Application Constraints
Active Mode (Run Mode)	AM_LDO_VCORE0	LDO or DC-DC regulator based active modes at core voltage level 0. CPU is active and full peripheral functionality is available. CPU and DMA maximum operating frequency is 24 MHz. Peripherals maximum input clock frequency is 12 MHz. All low and high-frequency clock sources can be active. Flash memory and all enabled SRAM banks are active.
	AM_DCDC_VCORE0	
	AM_LDO_VCORE1	LDO or DC-DC regulator based active modes at core voltage level 1. CPU is active and full peripheral functionality is available. CPU and DMA maximum operating frequency is 48 MHz. Peripherals maximum input clock frequency is 24 MHz. All low and high-frequency clock sources can be active. Flash memory and all enabled SRAM banks are active.
	AM_DCDC_VCORE1	
	AM_LF_VCORE0	LDO based low-frequency active modes at core voltage level 0 or 1. CPU is active and full peripheral functionality is available. CPU, DMA and peripherals maximum operating frequency is 128 kHz. Only low-frequency clock sources (LFXT, REFO, and VLO) can be active. All high-frequency clock sources need to be disabled by application. Flash memory and all enabled SRAM banks are active. Flash erase/program operations and SRAM bank enable or retention enable configuration changes must not be performed by application. DC-DC regulator can not be used.
	AM_LF_VCORE1	
LPM0 (Sleep)	LPM0_LDO_VCORE0	LDO or DC-DC regulator based operating modes at core voltage level 0. CPU is inactive but full peripheral functionality is available. DMA maximum operating frequency is 24 MHz. Peripherals maximum input clock frequency is 12 MHz. All low and high-frequency clock sources can be active. Flash memory and all enabled SRAM banks are active.
	LPM0_DCDC_VCORE0	
	LPM0_LDO_VCORE1	LDO or DC-DC regulator based operating modes at core voltage level 1. CPU is inactive but full peripheral functionality is available. DMA maximum operating frequency is 48 MHz. Peripherals maximum input clock frequency is 24 MHz. All low and high-frequency clock sources can be active. Flash memory and all enabled SRAM banks are active.
	LPM0_DCDC_VCORE1	
	LPM0_LF_VCORE0	LDO based low-frequency operating modes at core voltage level 0 or 1. CPU is inactive but full peripheral functionality is available. DMA and peripherals maximum operating frequency is 128 kHz. Only low-frequency clock sources (LFXT, REFO, and VLO) can be active. All high-frequency clock sources need to be disabled by application. Flash memory and all enabled SRAM banks are active. Flash erase/program operations and SRAM bank enable or retention enable configuration changes must not be performed by application. DC-DC regulator can not be used.
	LPM0_LF_VCORE1	

Table 7-1. Power Modes Summary (continued)

Power Mode	Operating State	Features and Application Constraints
LPM3 (Deep Sleep)	LDO_VCORE0	LDO based operating modes at core voltage level 0 or 1. CPU is inactive and peripheral functionality is reduced. Only RTC and WDT modules can be functional with maximum input clock frequency of 32.768 kHz. All other peripherals and retention enabled SRAM banks are kept under state retention power gating.
	LDO_VCORE1	Flash memory is disabled. SRAM banks not configured for retention are disabled. Only low-frequency clock sources (LFXT, REFO, and VLO) can be active. All high-frequency clock sources are disabled. Device I/O pin states are latched and retained. DC-DC regulator can not be used.
LPM4 (Deep Sleep)	LDO_VCORE0	LDO based operating modes at core voltage level 0 or 1. Achieved by entering LPM3 with RTC and WDT modules disabled. CPU is inactive with no peripheral functionality. All peripherals and retention enabled SRAM banks are kept under state retention power gating.
	LDO_VCORE1	Flash memory is disabled. SRAM banks not configured for retention are disabled. All low and high-frequency clock sources are disabled. Device I/O pin states are latched and retained. DC-DC regulator can not be used.
LPM3.5 (Stop or Shut Down)	LDO_VCORE0	LDO based operating mode at core voltage level 0. Only RTC and WDT modules can be functional with maximum input clock frequency of 32.768 kHz. CPU and all other peripherals are powered down. Only Bank-0 of SRAM is under data retention. All other SRAM banks and flash memory are powered down. Only low-frequency clock sources (LFXT, REFO, and VLO) can be active. All high-frequency clock sources are disabled. Device I/O pin states are latched and retained. DC-DC regulator can not be used.
LPM4.5 (Stop or Shut Down)	VCORE_OFF	Core voltage is turned off. CPU, flash memory, all SRAM banks, and all peripherals are powered down. All low and high-frequency clock sources are powered down. Device I/O pin states are latched and retained.

Power System

- MSP432 Power Control Manager

Table 7-8. Wake-up Sources from Low Power Modes

Peripheral	Wake-up Source	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
eUSCI_A	Any enabled interrupt	Yes	–	–	–	–
eUSCI_B	Any enabled interrupt	Yes	–	–	–	–
Timer_A	Any enabled interrupt	Yes	–	–	–	–
Timer32	Any enabled interrupt	Yes	–	–	–	–
Comparator_E	Any enabled interrupt	Yes	–	–	–	–
ADC14	Any enabled interrupt	Yes	–	–	–	–
AES256	Any enabled interrupt	Yes	–	–	–	–
DMA	Any enabled interrupt	Yes	–	–	–	–
Clock System (CS)	Any enabled interrupt	Yes	–	–	–	–
Power Control Manager (PCM)	Any enabled interrupt	Yes	–	–	–	–
FLCTL	Any enabled interrupt	Yes	–	–	–	–
WDT_A in Watchdog Mode(1)	Watchdog driven reset	Yes	–	–	–	–
RTC_C	Any enabled interrupt (2)	Yes	Yes	–	Yes	–
WDT_A in Interval Timer Mode	Enabled interrupt	Yes	Yes	–	Yes	–
I/O Ports	Any enabled interrupt	Yes	Yes	Yes	Yes	Yes
NMI at Device Pin(3)	External NMI event	Yes	Yes	Yes	–	–
SVSMH in Monitor Mode (PSS)(4)	Enabled interrupt	Yes	Yes	Yes	–	–
Debugger Power up Request	SYSPWRUPREQ event	–	Yes	Yes	Yes	Yes
Debugger Reset Request	DBGRSTREQ event(5)(6)	Yes	Yes	Yes	Yes	Yes
RSTn at Device Pin	External reset event (5)(6)	Yes	Yes	Yes	Yes	Yes
SVSMH in Supervisor Mode (PSS)	SVSMH driven reset (5)(6)	Yes	Yes	Yes	Yes	Yes
Power Cycle	Power on/off(5)(6)	Yes	Yes	Yes	Yes	Yes

Power System

- MSP432 Power Control Manager
  - PCM Registers

Table 7-9. PCM Registers

Offset	Acronym	Register Name	Type	Reset	Section
00h	PCMCTL0	Control 0 Register	Read/write	A5960000h	Section 7.24.1
04h	PCMCTL1	Control 1 Register	Read/write	A5960000h	Section 7.24.2
08h	PCMIE	Interrupt Enable register	Read/write	00000000h	Section 7.24.3
0Ch	PCMIFG	Interrupt Flag Register	Read	00000000h	Section 7.24.4
10h	PCMCLRIFG	Clear Interrupt Flag Register	Write	00000000h	Section 7.24.5

Power System

- MSP432 Power Control Manager
  - PCM Control Register 0

Figure 7-8. PCMCTL0 Register

31	30	29	28	27	26	25	24
PCMKEY							
rw-1	rw-0	rw-1	rw-0	rw-0	rw-1	rw-0	rw-1
23	22	21	20	19	18	17	16
PCMKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
15	14	13	12	11	10	9	8
Reserved			CPM				
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
LPMR				AMR			
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Power System

- MSP432 Power Control Manager
  - PCM Control Register 0

Table 7-10. PCMCTL0 Register Description

Bit	Field	Type	Reset	Description
31-16	PCMKEY	RW	A596h	PCM key. Must write proper key to allow write access to PMR. Any incorrect key does not allow PMR to be written, and the power change request is not generated. Write PCMKEY = 695A_xxxxh to unlock for write access. Always reads back A596h. This is a word-accessible register. Any other type of access (half-word or byte access) is ignored by the PCM.
15-14	Reserved	R	0h	Reserved. Always read as 0.
13-8	CPM	R	0h	Current Power Mode. These bits reflect the current power mode and are updated when the power mode request completes. 0h = AM_LDO_VCORE0. LDO based Active Mode at Core voltage setting 0. 1h = AM_LDO_VCORE1. LDO based Active Mode at Core voltage setting 1. 2h = Reserved 3h = Reserved 4h = AM_DCDC_VCORE0. DC-DC based Active Mode at Core voltage setting 0. 5h = AM_DCDC_VCORE1. DC-DC based Active Mode at Core voltage setting 1. 6h = Reserved 7h = Reserved 8h = AM_LF_VCORE0. Low-Frequency Active Mode at Core voltage setting 0. 9h = AM_LF_VCORE1. Low-Frequency Active Mode at Core voltage setting 1. Ah-Fh = Reserved 10h = LPM0_LDO_VCORE0. LDO based LPM0 at Core voltage setting 0. 11h = LPM0_LDO_VCORE1. LDO based LPM0 at Core voltage setting 1. 12h = Reserved 13h = Reserved 14h = LPM0_DCDC_VCORE0. DC-DC based LPM0 at Core voltage setting 0. 15h = LPM0_DCDC_VCORE1. DC-DC based LPM0 at Core voltage setting 1. 16h = Reserved 17h = Reserved 18h = LPM0_LF_VCORE0. Low-frequency LPM0 at Core voltage setting 0. 19h = LPM0_LF_VCORE1. Low-frequency LPM0 at Core voltage setting 1. 1Ah-3Fh = Reserved.

Power System

- MSP432 Power Control Manager
  - PCM Control Register 0

Bit	Field	Type	Reset	Description
7-4	LPMR	RW	0h	Low Power Mode Request. Used to request low power modes LPM3, LPM3.5, and LPM4.5. These bits can only be modified while PMR_BUSY = 0 of the PCMCTL1. 0h = LPM3. Core voltage setting is similar to the mode from which LPM3 is entered. 1h-9h = Reserved (1) Ah = LPM3.5. Core voltage setting 0. Bh = Reserved. (1) Ch = LPM4.5 Dh-Fh = Reserved (1)
3-0	AMR	RW	0h	Active Mode Request. Used to request active modes. These bits can only be modified while PMR_BUSY = 0 of the PCMCTL1. 0h = AM_LDO_VCORE0. LDO based Active Mode at Core voltage setting 0. 1h = AM_LDO_VCORE1. LDO based Active Mode at Core voltage setting 1. 2h-3h = Reserved (2) 4h = AM_DCDC_VCORE0. DC-DC based Active Mode at Core voltage setting 0. 5h = AM_DCDC_VCORE1. DC-DC based Active Mode at Core voltage setting 1. 6h-7h = Reserved (2) 8h = AM_LF_VCORE0. Low-Frequency Active Mode at Core voltage setting 0. 9h = AM_LF_VCORE1. Low-Frequency Active Mode at Core voltage setting 1. Ah-Fh = Reserved (2)

Power System

- MSP432 Power Control Manager
  - PCM Control Register 1

Figure 7-9. PCMCTL1 Register

31	30	29	28	27	26	25	24
PCMKEY							
rw-1	rw-0	rw-1	rw-0	rw-0	rw-1	rw-0	rw-1
23	22	21	20	19	18	17	16
PCMKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
15	14	13	12	11	10	9	8
Reserved							PMR_BUSY
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved					FORCE_LPM_ ENTRY	LOCKBKUP	LOCKLPM5
r-0	r-0	r-0	r-0	r-0	rw-0	rw-(0)	rw-(0)

Power System

- MSP432 Power Control Manager
  - PCM Control Register 1

Table 7-11. PCMCTL1 Register Description

Bit	Field	Type	Reset	Description
31-16	PCMKEY	RW	A596h	PCM key. Must write proper key to allow write access to PCMCTL1 . Any incorrect key does not allow PCMCTL1 to be written, and the write is ignored. Write PCMKEY = 695A_xxxxh to unlock for write access. Always reads back A596h. This is a word-accessible register. Any other type of access (half-word or byte access) is ignored by the PCM.
15-9	Reserved	R	0h	Reserved. Reads back 0.
8	PMR_BUSY	R	0h	Power mode request busy flag. This flag is set while a power change request is being processed. The flag is cleared when the request has completed. Writes to the PCMCTL0 or Clock System registers are ignored while PMR_BUSY = 1. Reads to the PCMCTL0 or Clock System registers are possible while PMR_BUSY = 1.
7-3	Reserved	R	0h	Reserved. Reads back 0.
2	FORCE_LPM_ENTRY	RW	0h	Bit selection for the application to determine whether the entry into LPM3/LPMx.5 should be forced even if there are active system clocks running which do not meet the LPM3/LPMx.5 criteria. This bit by itself does not cause a LPM3/LPMx.5 by itself, but is a pre-requisite before the CPU executes WFI. This bit needs to be programmed prior to LPMR bits in PCMCTL0 register. 0b = PCM aborts LPM3 or LPMx.5 transition if the active clock configuration does not meet the LPM3 or LPMx.5 entry criteria. PCM generates the LPM_INVALID_CLK flag on abort to LPM3 or LPMx.5 entry. 1b = PCM enters LPM3 or LPMx.5 after shutting off the clocks forcefully. The application must make sure that the RTC and WDT are clocked using BCLK tree to keep these modules active in LPM3 in LPM3.5. In LPM4.5, all clocks are turned off and the core voltage is turned off.

Power System

- MSP432 Power Control Manager
  - PCM Control Register 1

Bit	Field	Type	Reset	Description
1	LOCKBKUP	RW	0h	Lock Backup. After this bit is set, it can be cleared only by the application or by a power cycle. This bit is automatically set upon LPM3.5 entry. The application cannot set this bit. In the write mode, this bit should always be written with a value of 0 to clear it. Writing a value of 1 has no effect on the system and these writes are ignored. 0b = Backup domain configuration defaults to reset condition. 1b = Backup domain configuration remains locked during LPM3.5 entry and exit.
0	LOCKLPM5	RW	0h	Lock LPM5. When this bit is set, it can be cleared only by the application or by a power cycle. This bit is automatically set upon LPM3.5 or LPM4.5 entry. The application cannot set this bit. In the write mode, this bit should always be written with a value of 0 to clear it. Writing a value of 1 has no effect on the system and these writes are ignored. 0b = LPMx.5 configuration defaults to reset condition. 1b = LPMx.5 configuration remains locked during LPMx.5 entry and exit.

Power System

- MSP432 Power Control Manager
  - PCM Interrupt Enable Register

Figure 7-10. PCMIE Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved	DCDC_ERROR_IE	Reserved			AM_INVALID_TR_IE	LPM_INVALID_CLK_IE	LPM_INVALID_TR_IE
r-0	rw-0	r-0	r-0	r-0	rw-0	rw-0	rw-0

Table 7-12. PCMIE Register Description

Bit	Field	Type	Reset	Description
31-7	Reserved	R	0h	Reserved. Reads back 0.
6	DCDC_ERROR _IE	RW	0h	DC-DC error interrupt enable. Setting this bit enables an interrupt/NMI when DC-DC operation cannot be achieved or maintained. 0b = Disabled 1b = Enabled
5-3	Reserved	R	0h	Reserved. Reads back 0.
2	AM_INVALID_TR_IE	RW	0h	Active mode invalid transition interrupt enable. Setting this bit enables an interrupt/NMI on an invalid transition setting during an active power mode request. 0b = Disabled 1b = Enabled
1	LPM_INVALID_CLK_IE	RW	0h	LPM invalid clock interrupt enable. Setting this bit enables an interrupt/NMI on an invalid clock setting during a LPM3/LPMx.5 transition from an active mode when FORCE_LPM_ENTRY = 0. This bit has not effect when FORCE_LPM_ENTRY = 1. 0b = Disabled 1b = Enabled
0	LPM_INVALID_TR_IE	RW	0h	LPM invalid transition interrupt enable. Setting this bit enables an interrupt/NMI on an invalid transition from Active Mode to LPM3 (LPMx.5 all transitions are allowed). 0b = Disabled 1b = Enabled

Power System

- MSP432 Power Control Manager
  - PCM Interrupt Flag Register

Figure 7-11. PCMIFG Register

31	30	29	28	27	26	25	24
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
23	22	21	20	19	18	17	16
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
15	14	13	12	11	10	9	8
Reserved							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved	DCDC_ERROR_IFG	Reserved			AM_INVALID_TR_IFG	LPM_INVALID_CLK_IFG	LPM_INVALID_TR_IFG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

Table 7-13. PCMIFG Register Description

Bit	Field	Type	Reset	Description
31-7	Reserved	R	0h	Reserved. Reads back 0.
6	DCDC_ERROR_IFG	R	0h	DC-DC error flag. This flag is set if DC-DC operation cannot be achieved or maintained. Flag remains set until cleared by software.
5-3	Reserved	R	0h	Reserved. Reads back 0.
2	AM_INVALID_TR_IFG	R	0h	Active mode invalid transition flag. This flag is set if the active mode request is an invalid transition. Flag remains set until cleared by software.
1	LPM_INVALID_CLK_IFG	R	0h	LPM invalid clock flag. This flag is set if the LPM request is invalid due to a clock request active before the LPM3/LPMx.5 entry while the FORCE_LPM_ENTRY = 0. Flag remains set until cleared by software.
0	LPM_INVALID_TR_IFG	R	0h	LPM invalid transition flag. This flag is set if the requested Active Mode to LPM3 transition is invalid. Flag remains set until cleared by software.

Power System

- MSP432 Power Control Manager
  - PCM Interrupt Clear Flag Register

Figure 7-12. PCMCLRIFG Register

31	30	29	28	27	26	25	24
Reserved							
w1	w1	w1	w1	w1	w1	w1	w1
23	22	21	20	19	18	17	16
Reserved							
w1	w1	w1	w1	w1	w1	w1	w1
15	14	13	12	11	10	9	8
Reserved							
w1	w1	w1	w1	w1	w1	w1	w1
7	6	5	4	3	2	1	0
Reserved	CLR_DCDC_ERROR_IFG	Reserved			CLR_AM_INVALID_TR_IFG	CLR_LPM_INVALID_CLK_IFG	CLR_LPM_INVALID_TR_IFG
w1	w1	w1	w1	w1	w1	w1	w1

Table 7-14. PCMCLRIFG Register Description

Bit	Field	Type	Reset	Description
31-7	Reserved	W	0h	Reserved. Write 1 only. Reads back 0.
6	CLR_DCDC_ERROR_IFG	W	0h	Clear DC-DC error flag. 0b = No effect 1b = Clear flag
5-3	Reserved	W	0h	Reserved. Write 1 only. Reads back 0.
2	CLR_AM_INVALID_TR_IFG	W	0h	Clear active mode invalid transition flag. 0b = No effect 1b = Clear flag
1	CLR_LPM_INVALID_CLK_IFG	W	0h	Clear LPM invalid clock flag. 0b = No effect 1b = Clear flag
0	CLR_LPM_INVALID_TR_IFG	W	0h	Clear LPM invalid transition flag. 0b = No effect 1b = Clear flag

Power System

- MSP432 Power Control Manager
  - Programming Example
    - Change power mode

1) Make sure Power control Module is inactive
2) Write the key and desired state into the control register
3) Check to see if transition is complete
4) Check to make sure correct new mode is set
5) Clear the change key – prevent unintended changes

Power System

- MSP432 Power Control Manager
  - Programming Example
    - set Active, LDO, Vcore 1 modes

```
// Power mode cannot be changed until the Power Control Module (PCM)
// is not active. Status is held in PCMCTL1 register bit 8 (PMR_BUSY)
// Power mode can be changed when this bit is zero (idle)
// Wait for  PMR to be idle

uint32_t PMR_fail = 100000; // set # of attempts
while(PCM->CTL1 & 0x00000100){
  PMR_fail--;
  if(PMR_fail == 0)// Attempt Failed - no changes made - return 1
    return -1;
} // end while
```

8	PMR_BUSY	R	0h	Power mode request busy flag. This flag is set while a power change request is being processed. The flag is cleared when the request has completed. Writes to the PCMCTL0 or Clock System registers are ignored while PMR_BUSY = 1. Reads to the PCMCTL0 or Clock System registers are possible while PMR_BUSY = 1.

Power System

- MSP432 Power Control Manager
  - Programming Example
    - set Active, LDO, Vcore 1 modes

```
// The Power Control Module requires a special value (Key) to be written to
// to change the power mode. Default mode does not support 48MHz operation.
// Key is 0x695A_xxxx and loads into PCMCTL0
//
// Simultaneously set the PCM to active mode, LDO Vcore 1 (highest voltage)
// to support 48MHz operation - PCMCTL0, bit 0 = high

//              Force 0's in key       force 1's in key   force mode to 1
PCM->CTL0 = (PCM->CTL0 & ~0xFFFF000F) |   0x695A0000    |   0x00000001;
```

3-0	AMR	RW	0h	Active Mode Request. Used to request active modes. These bits can only be modified while PMR_BUSY = 0 of the PCMCTL1. 0h = AM_LDO_VCORE0. LDO based Active Mode at Core voltage setting 0. 1h = AM_LDO_VCORE1. LDO based Active Mode at Core voltage setting 1. 2h-3h = Reserved (2) 4h = AM_DCDC_VCORE0. DC-DC based Active Mode at Core voltage setting 0. 5h = AM_DCDC_VCORE1. DC-DC based Active Mode at Core voltage setting 1. 6h-7h = Reserved (2) 8h = AM_LF_VCORE0. Low-Frequency Active Mode at Core voltage setting 0. 9h = AM_LF_VCORE1. Low-Frequency Active Mode at Core voltage setting 1. Ah-Fh = Reserved (2)

Power System

- MSP432 Power Control Manager
  - Programming Example
    - set Active, LDO, Vcore 1 modes

```
// There is a flag to indicate transition to active mode is NOT valid
// PCMIFG bit 2 (AM_INVALID_TR_IFG)
if(PCM->IFG & 0x00000004){
  PCM->CLRIFG = 0x00000004;// Attempt failed - clear flag and return 2
  return -2;
} // end if
```

Table 7-13. PCMIFG Register Description

Bit	Field	Type	Reset	Description
31-7	Reserved	R	0h	Reserved. Reads back 0.
6	DCDC_ERROR_IFG	R	0h	DC-DC error flag. This flag is set if DC-DC operation cannot be achieved or maintained. Flag remains set until cleared by software.
5-3	Reserved	R	0h	Reserved. Reads back 0.
2	AM_INVALID_TR_IFG	R	0h	Active mode invalid transition flag. This flag is set if the active mode request is an invalid transition. Flag remains set until cleared by software.
1	LPM_INVALID_CLK_IFG	R	0h	LPM invalid clock flag. This flag is set if the LPM request is invalid due to a clock request active before the LPM3/LPMx.5 entry while the FORCE_LPM_ENTRY = 0. Flag remains set until cleared by software.
0	LPM_INVALID_TR_IFG	R	0h	LPM invalid transition flag. This flag is set if the requested Active Mode to LPM3 transition is invalid. Flag remains set until cleared by software.

Power System

- MSP432 Power Control Manager
  - Programming Example
    - set Active, LDO, Vcore 1 modes

```
uint32_t AM_LDO_VCORE1_fail = 500000; // set # of attempts
// Check the actual mode, and wait for AM LDO VCORE1 to be set
// Status is in PCMCTL0, AM_LDO_VCORE1 mode is 0x01 on bits 13:8
while((PCM->CTL0 & 0x00003F00) != 0x00000100){
  AM_LDO_VCORE1_fail--;
  if(AM_LDO_VCORE1_fail == 0)
    return -3;// Attempt failed - return 3
} // end while
```

13-8	CPM	R	0h	Current Power Mode. These bits reflect the current power mode and are updated when the power mode request completes. 0h = AM_LDO_VCORE0. LDO based Active Mode at Core voltage setting 0. 1h = AM_LDO_VCORE1. LDO based Active Mode at Core voltage setting 1. 2h = Reserved 3h = Reserved

Power System

- MSP432 Power Control Manager
  - Programming Example
    - set Active, LDO, Vcore 1 modes

```
// Power mode change is complete
// Clear the change key to prevent unintended changes
PCM->CTL1 &= ~0xFFFF0000;
```