Timer A

Last updated 6/17/19

Timer A

- Advanced Timer Functions
  - Output Compare
    - Sets a flag and/or creates an interrupt when the counter value matches a value programmed into a separate register
  - Input Capture
    - Captures the counter value when a trigger event occurs
    - Sets a flag and/or creates an interrupt
  - Pulse Width Modulation (PWM)
    - Creates an automated PWM signal

© tj

Timer A

- Advanced Timer Function
  - Output Compare
    - Sets a flag and/or creates an interrupt when the counter value matches a value programmed into a separate register
  - Delay Counter – in Periodic Mode
    - Count up or down - to or from – the Max Value
  - Compare Register
    - Holds the value to compare with the counter value
    - When matched – create a flag/interrupt

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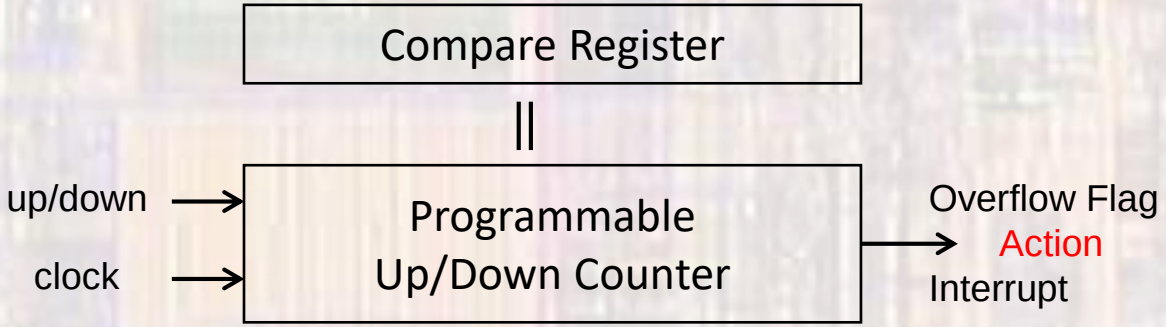
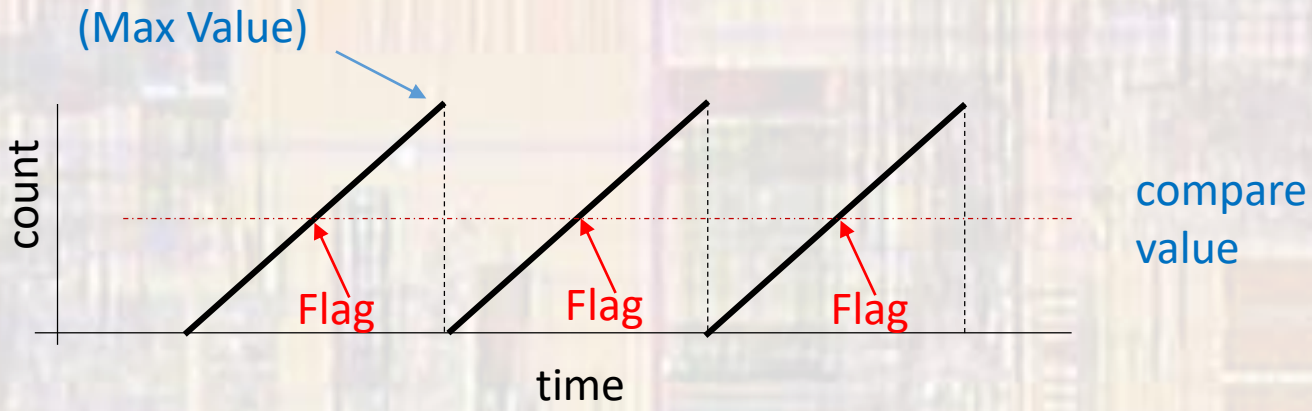
Timer A

- Advanced Timer Function
  - Output Compare





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Timer A

- Advanced Timer Function
  - Input Capture
    - Captures the timer count when an input event occurs
    - Sets a flag and/or creates an interrupt
  - Delay Counter – in Periodic Mode
    - Count up or down - to or from – the Max Value
  - Capture Register
    - Holds the value of the counter when an input event occurs

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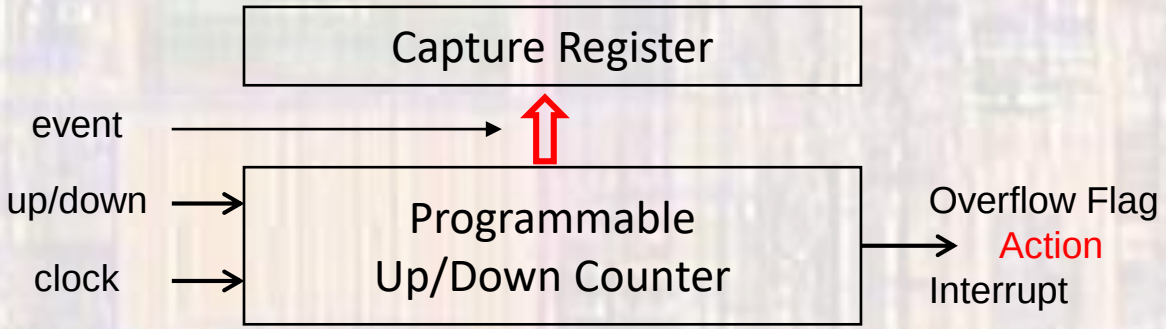
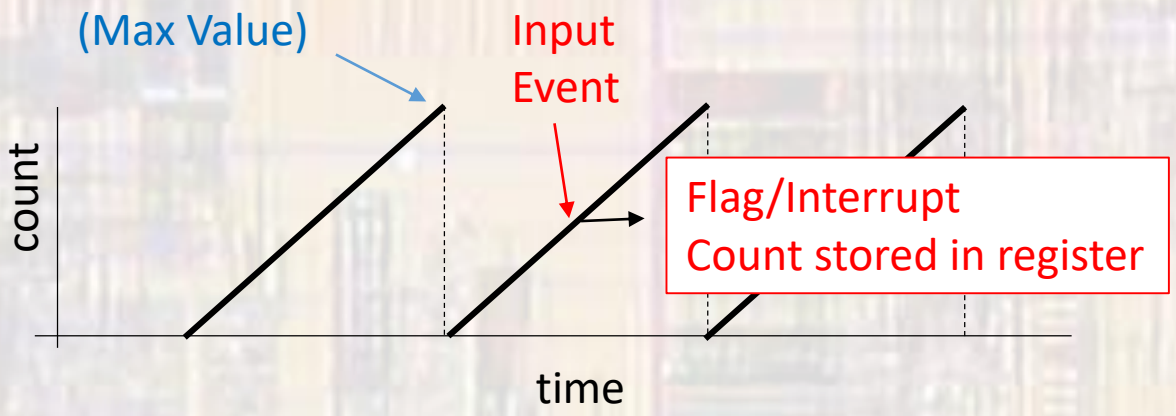
Timer A

- Advanced Timer Function
  - Input Capture





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Timer A

- Advanced Timer Function
  - Pulse Width Modulation (PWM)
    - Create an output waveform based on two counter values
    - Many variations
  - Delay Counter – in Periodic Mode
    - Count up or down - to or from – the Max Value
  - Compare Register(s)
    - Holds the value to compare with the counter value
    - When matched – create a flag/interrupt
  - Waveform Generator
    - Creates output transitions based on timer events

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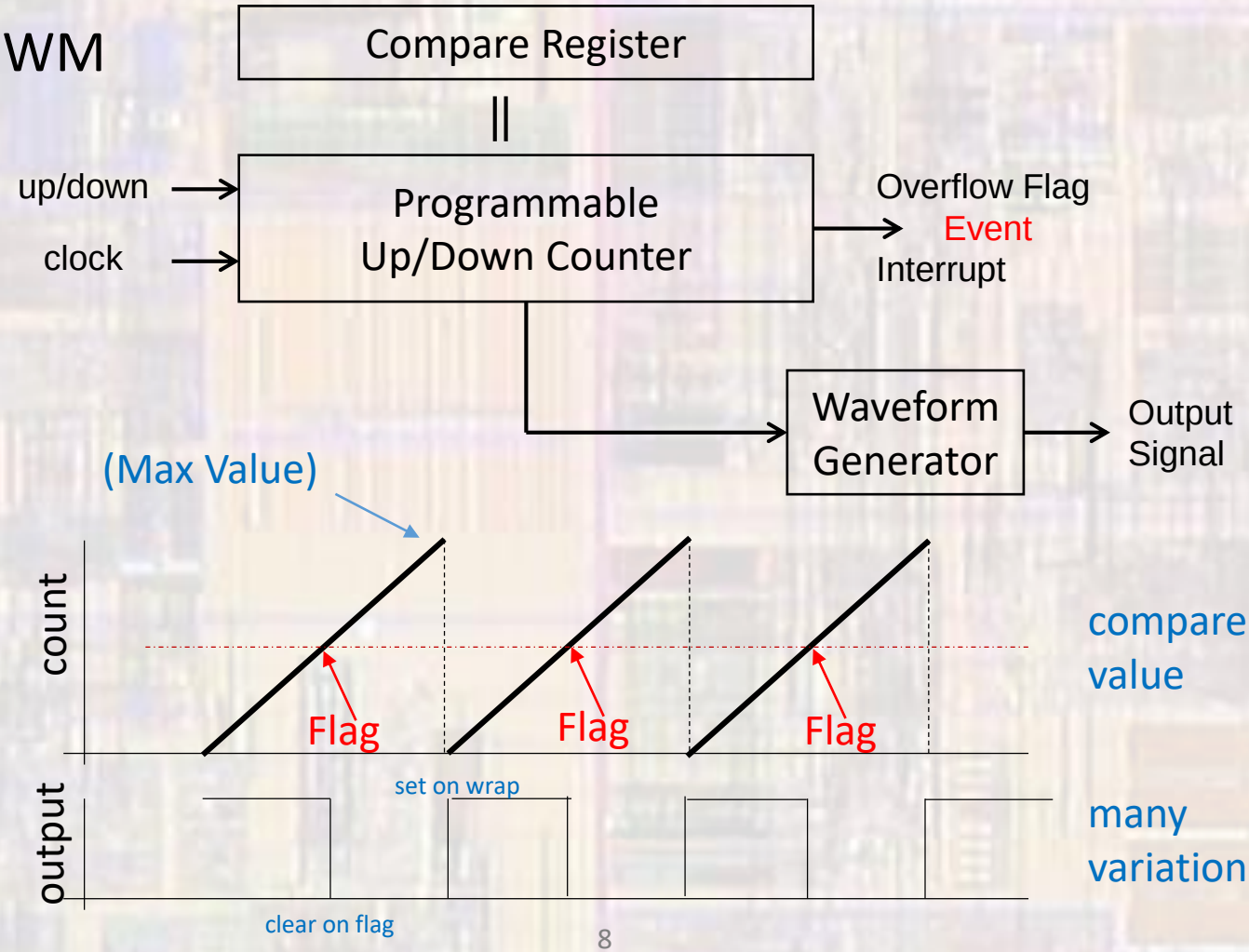
Timer A

- Advanced Timer Function
  - PWM



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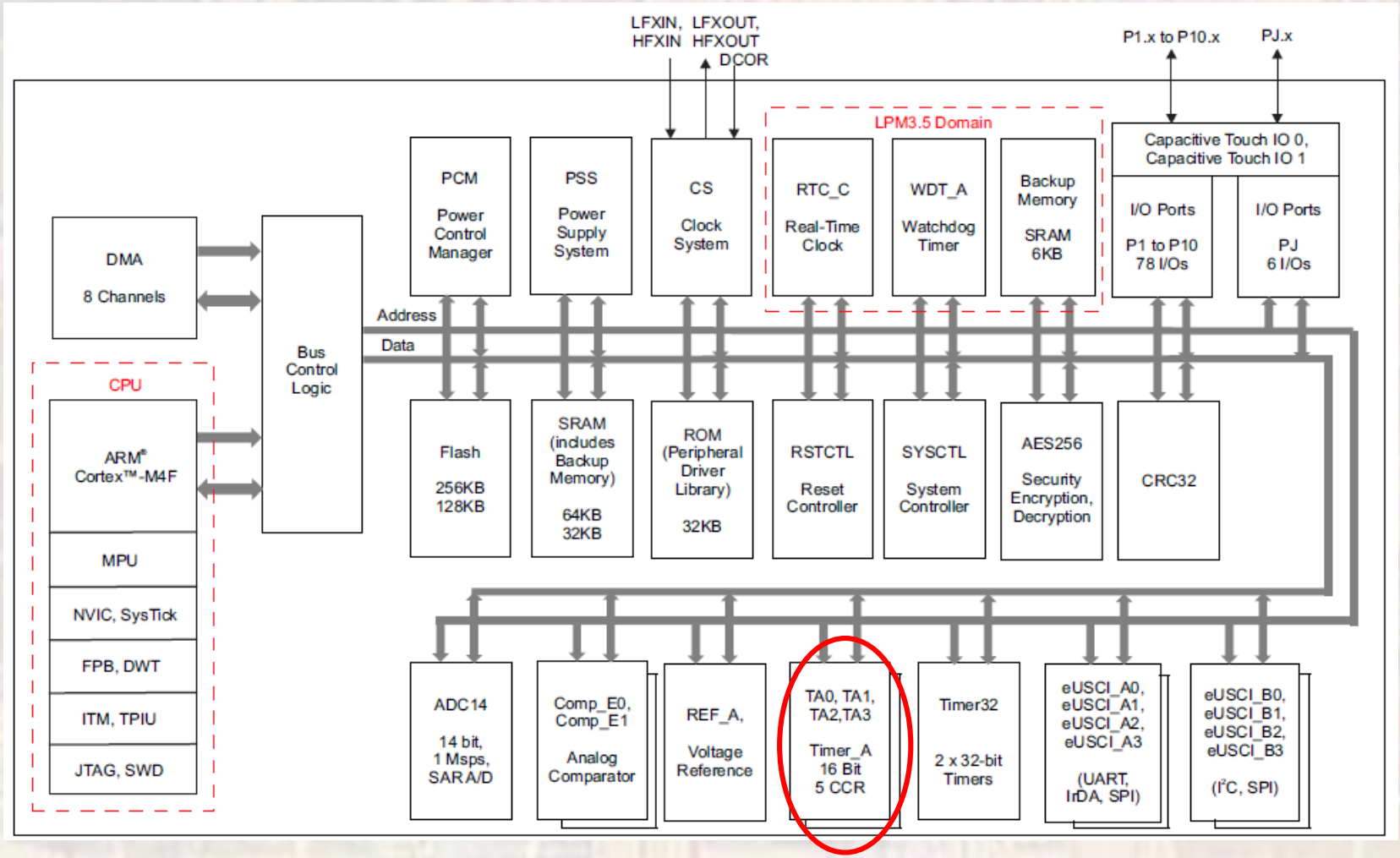
Timer A

- MSP432 Timer A



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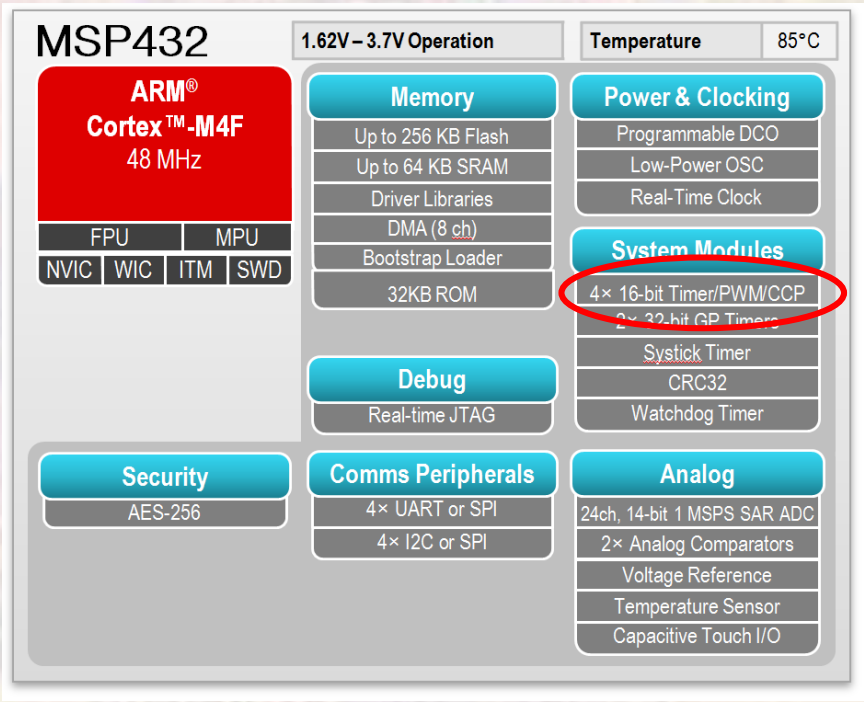
Timer A

- MSP432 Timer A
  - ARM (AMBA Compliant) timer
  - 4 – 16 bit timers
  - 3 Timer Modes
    - Up
    - Continuous
    - Up/Down
  - 4 Capture/Compare Modes
    - Timer
    - Capture
    - Compare
    - PWM



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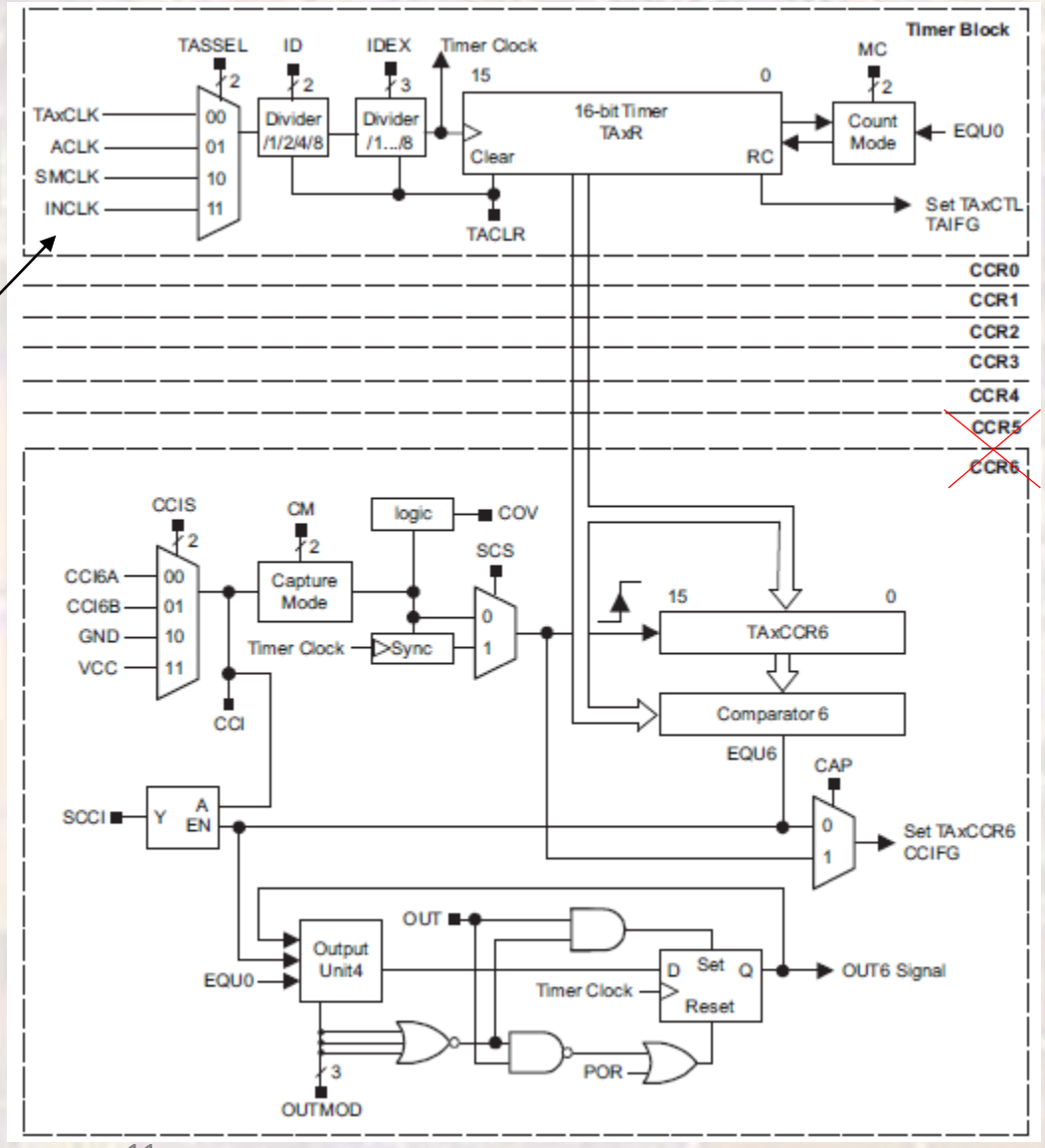
Timer A

- MSP432 Timer A
  - 4 Timers - each with 5 capture/compare blocks

Timer

1 of 5 Capture/Compare Blocks



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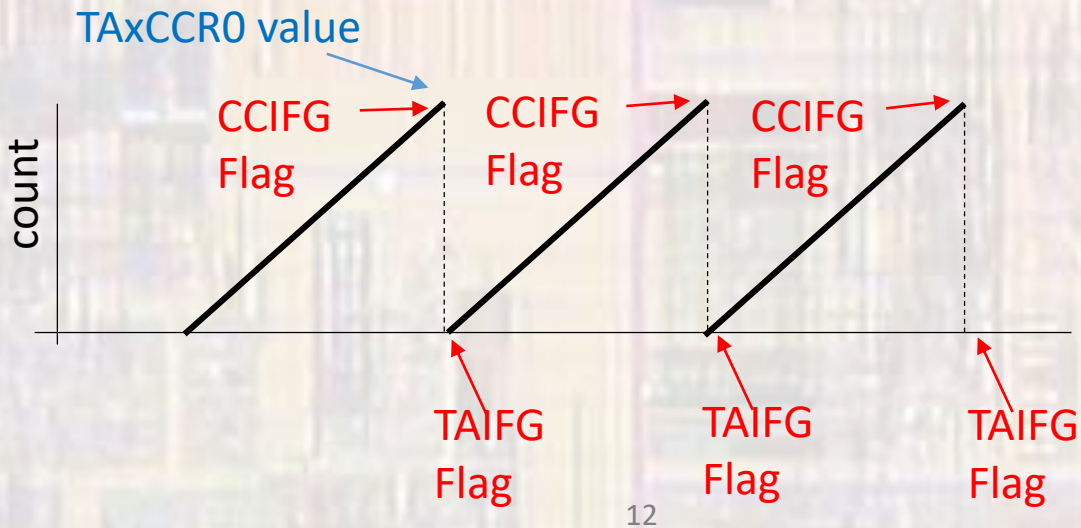
Timer A

- MSP432 Timer A
  - Timer - Up mode
    - Max count value is 2^{16}
    - TAxCCR0 register – holds the upper limit for the count
    - 2 Flags
      - CCIFG – set when counter reaches TAxCCR0value
      - TAIFG – set when the counter wraps around to 0



1 clock separation between the two flags

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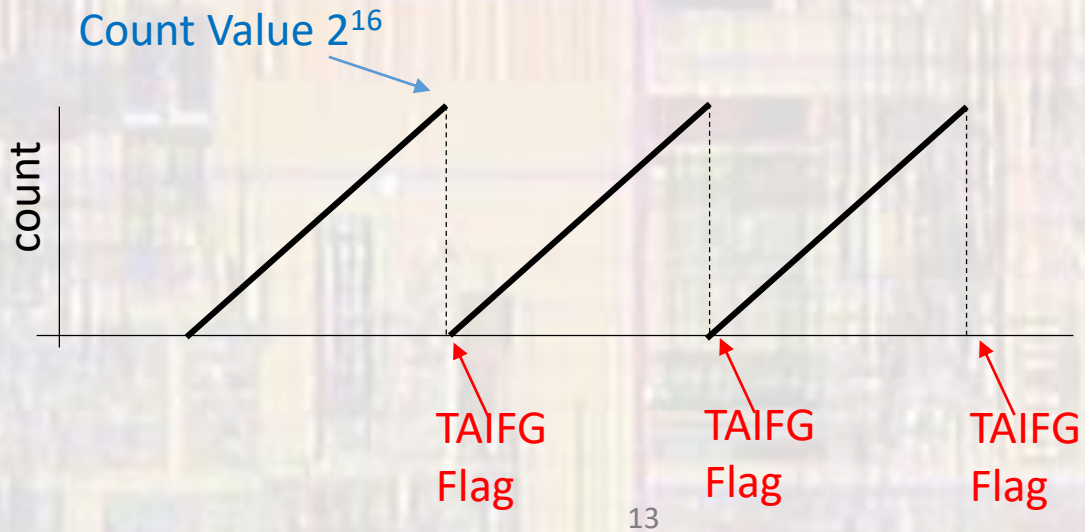
Timer A

- MSP432 Timer A
  - Timer - Continuous mode
    - Count value is 2^{16}
    - TAIFG – set when the counter wraps around to 0



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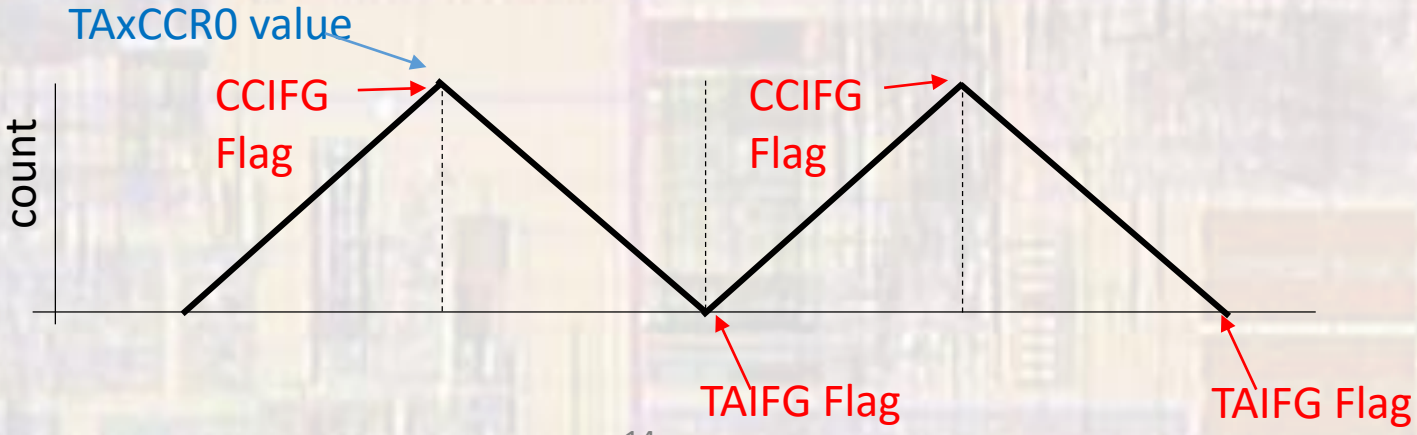
Timer A

- MSP432 Timer A
  - Timer - Up/Down mode
    - Max count value is 2^{16}
    - Allows for 2x period
    - TAxCCR0 register – holds the upper limit for the count
    - 2 Flags
      - CCIFG – set when counter reaches TAxCCR0value
      - TAIFG – set when the counter reaches 0



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Timer A

- MSP432 Timer A
  - Capture/Compare Block – Capture Mode
    - 5 Capture blocks in each timer
    - 2 trigger inputs
      - CCIxA, CCIxB
      - Can be tied to internal or external signals (pins)
      - Can select rising edge trigger, falling edge trigger or both
    - Captured timer value stored in TAxCCRn
    - CCIFG flag is set
    - Input value is visible as the CCI bit
    - Overflow bit (COV) to indicate a second trigger has been received prior to clearing the first trigger

© tj

Timer A

- MSP432 Timer A
  - Capture/Compare Block – Compare Mode/PWM Mode
    - 5 Compare blocks in each timer
    - Desired Compare values stored in TAxCCRn (n = 0:4)
    - CCIFG flag is set
    - Internal signal EQUn is set – modifies output modes
    - Input signal CCI is latched into SCCI
    - Used to create periodic interrupts or PWM signals

© tj

Timer A

- MSP432 Timer A
  - Timer Output Block
    - Automatically create output signals
    - 8 modes – set by OUTMODx bits
    - Outputs based on EQU0 (count matches CCR0) and EQUn (count matches CCRn)

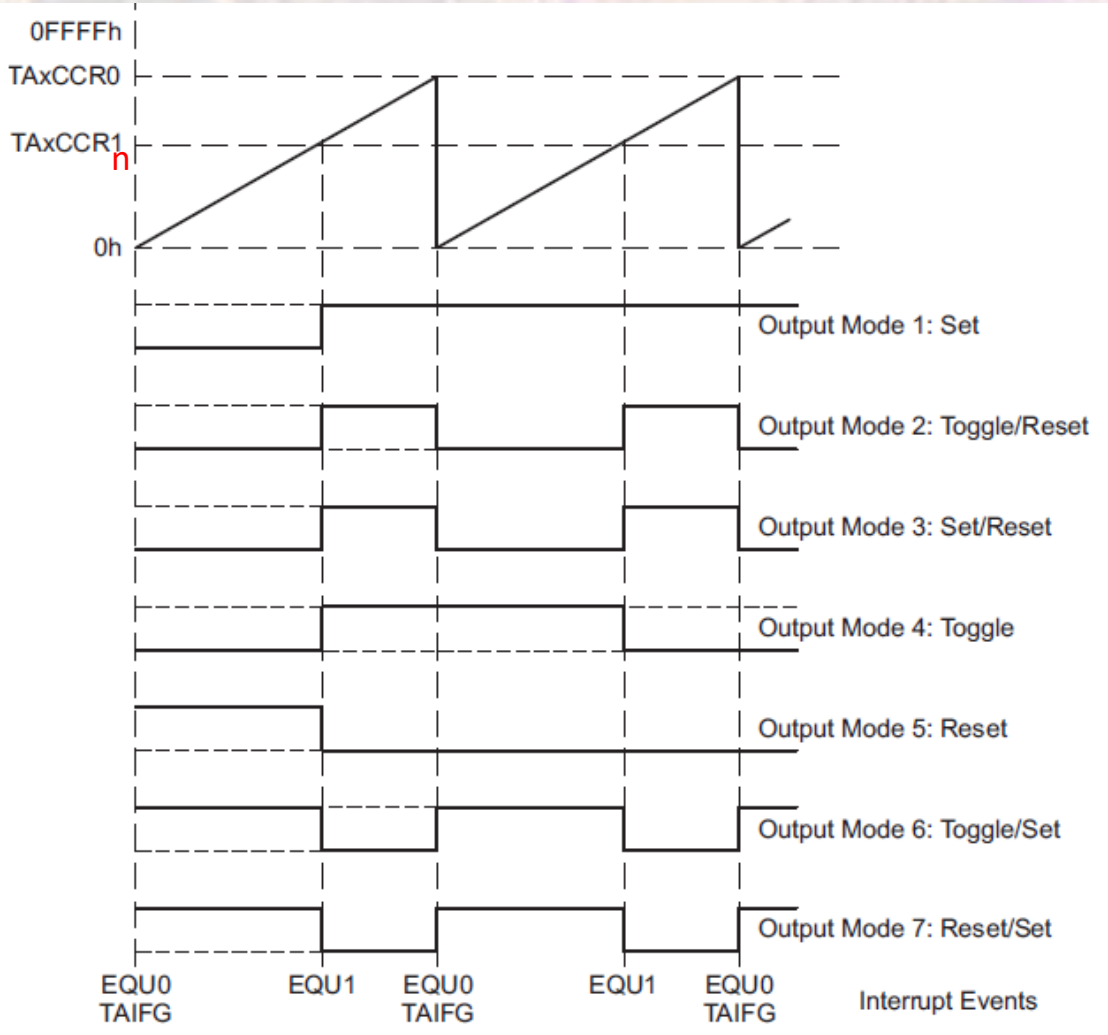
Table 17-2. Output Modes

OUTMODx	Mode	Description
000	Output	The output signal OUTn is defined by the OUT bit. The OUTn signal updates immediately when OUT is updated.
001	Set	The output is set when the timer *counts* to the TAxCCRn value. It remains set until a reset of the timer, or until another output mode is selected and affects the output.
010	Toggle/Reset	The output is toggled when the timer *counts* to the TAxCCRn value. It is reset when the timer *counts* to the TAxCCR0 value.
011	Set/Reset	The output is set when the timer *counts* to the TAxCCRn value. It is reset when the timer *counts* to the TAxCCR0 value.
100	Toggle	The output is toggled when the timer *counts* to the TAxCCRn value. The output period is double the timer period.
101	Reset	The output is reset when the timer *counts* to the TAxCCRn value. It remains reset until another output mode is selected and affects the output.
110	Toggle/Set	The output is toggled when the timer *counts* to the TAxCCRn value. It is set when the timer *counts* to the TAxCCR0 value.
111	Reset/Set	The output is reset when the timer *counts* to the TAxCCRn value. It is set when the timer *counts* to the TAxCCR0 value.

Timer A

- MSP432 Timer A

Timer in UP mode



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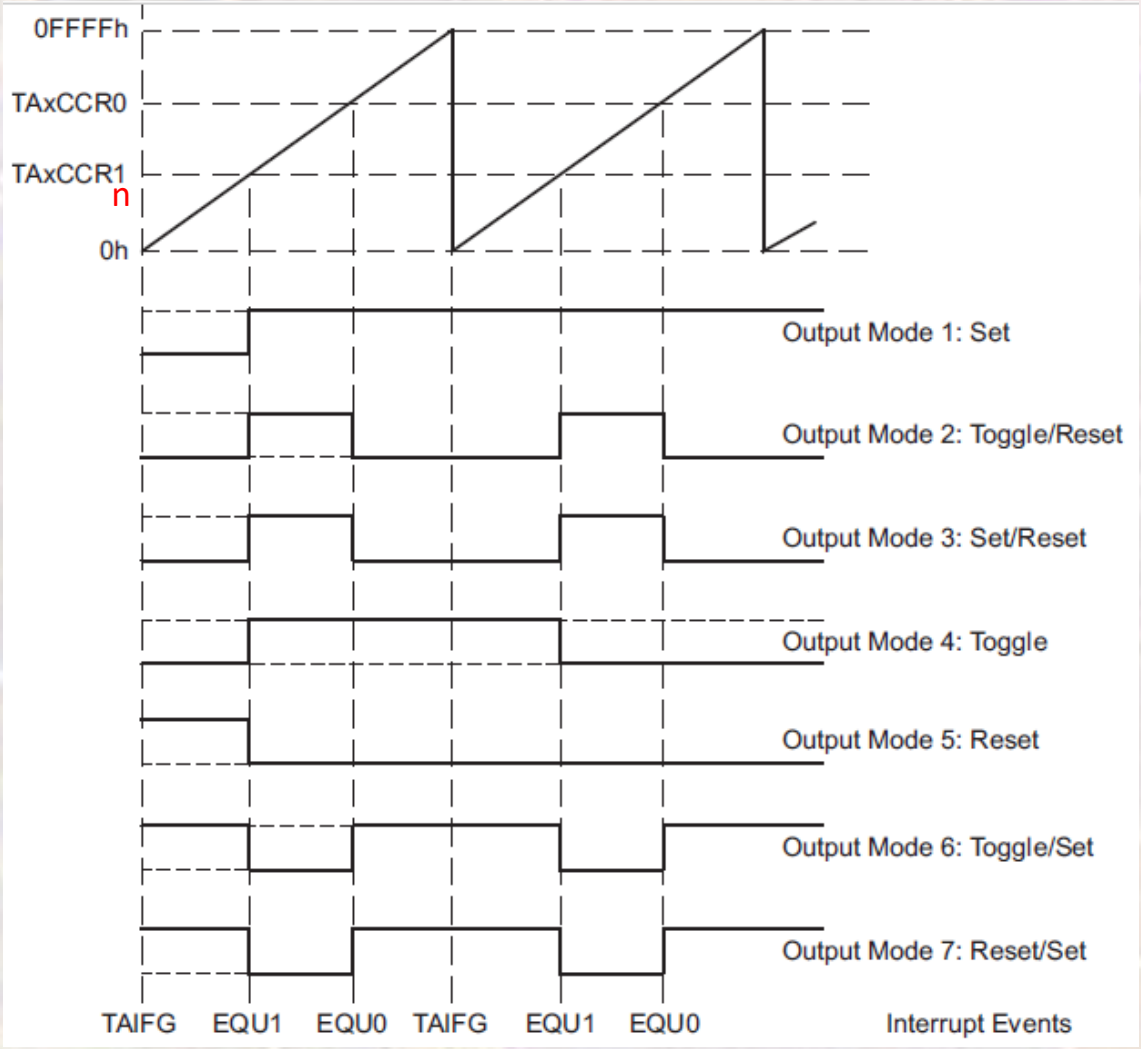
Timer A

- MSP432 Timer A

Timer in Continuous mode



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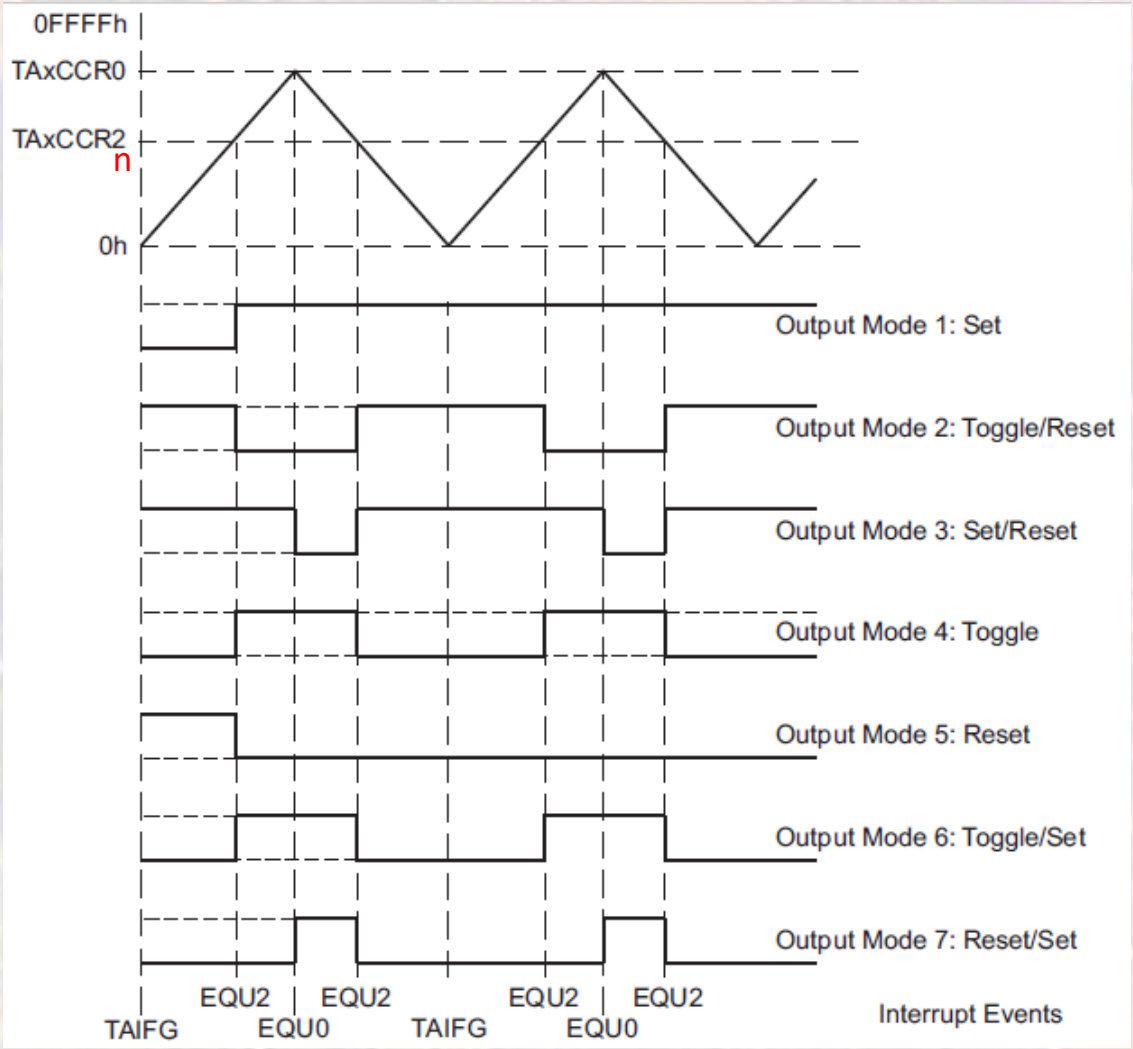
Timer A

- MSP432 Timer A

Timer in Up/Down mode



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Timer A

- MSP432 Timer A
  - Interrupts
    - 2 interrupt vectors
    - TAxCCR0 vector
      - Used for the CCIFG flag for TAxCCR0 only
    - TAxIV vector
      - CCIFG flag set in capture mode on TAxCCRn
      - CCIFG flag set in compare mode on TAxCCRn
      - TAIFG flag

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Timer A

- MSP432 Timer A
  - Interrupts
    - TAxIV vector generator
      - CCIFG and TAIFG flags are combined into a single interrupt vector
      - The highest priority enabled interrupt generator is stored in the TAxIV register
        - Can be evaluated or added to PC to execute the ISR
      - Reading TAxIV clears the current interrupt flag and activates the next highest pending interrupt

© tj

Timer A

- MSP432 Timer A
  - Calculation examples
    - Desire a 1KHz 50% duty cycle square wave
    - Timer in UP mode
    - Tclk = 12MHz

    12MHz clk → 83.33ns/clk
    1KHz → 1ms period
    →12,000 12MHz clks / 1KHz period
    for a square wave – 6000 12MHz clks low, 6000 12MHz clks high
    12,000 clks is well within our 65,536 maximum limit

© tj

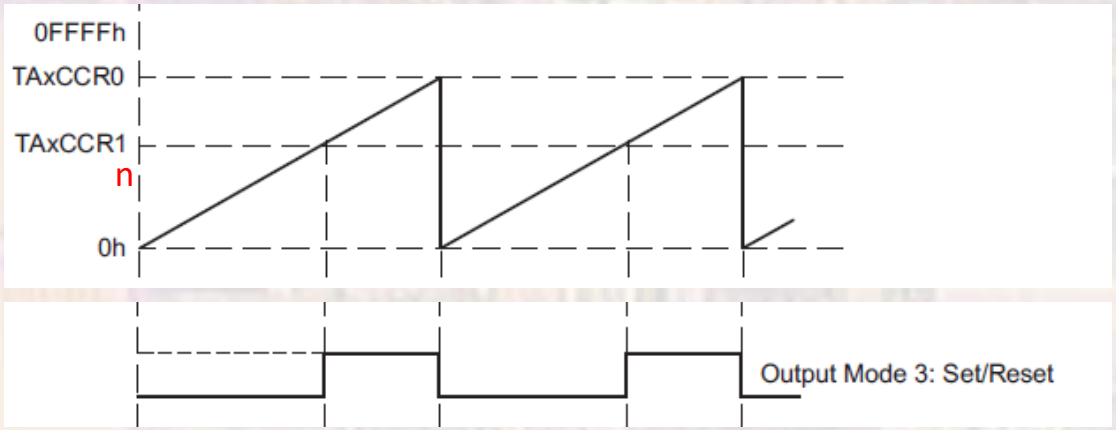
Timer A

- MSP432 Timer A
  - Calculation examples
    for a square wave – 6000 12MHz clks low, 6000 12MHz clks high

    Choose set/reset mode
    Max = 12,000 clks
    Target = 6000 clks

    Up mode
    Fcounter = 12MHz
    TA0CCR0 = 12000
    TA0CCR1 = 6000

    → 1KHz Square wave



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Timer A

- MSP432 Timer A
  - Calculation examples
    - Timer in UP mode
    - Tclk = 12MHz
    - Desire a 1KHz 25% duty cycle square wave

Solution

© tj

Timer A

- MSP432 Timer A
  - Calculation examples
    - Timer in UP mode
    - Tclk = 12MHz
    - Desire a 100Hz 75% duty cycle square wave

Solution

© tj

Timer A

- MSP432 Timer A
  - Timer A Registers

Table 17-3. Timer_A Registers

Offset	Acronym	Register Name	Section
00h	TAxCTL	Timer_Ax Control	Section 17.3.1
02h to 0Eh	TAxCCTL0 to TAxCCTL6	Timer_Ax Capture/Compare Control 0 to Timer_Ax Capture/Compare Control 6	Section 17.3.3
10h	TAxR	Timer_Ax Counter	Section 17.3.2
12h to 1Eh	TAxCCR0 to TAxCCR6	Timer_Ax Capture/Compare 0 to Timer_Ax Capture/Compare 6	Section 17.3.4
2Eh	TAxIV	Timer_Ax Interrupt Vector	Section 17.3.5
20h	TAxEX0	Timer_Ax Expansion 0	Section 17.3.6

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Timer A

- MSP432 Timer A
  - Control Register

Figure 17-15. TAxCTL Register

15	14	13	12	11	10	9	8
Reserved						TASSEL	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
ID		MC		Reserved	TACLR	TAIE	TAIFG
rw-0	rw-0	rw-0	rw-0	rw-0	w-0	rw-0	rw-0

© tj

Timer A

- MSP432 Timer A
  - Control Register

Table 17-4. TAxCTL Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	RW	0h	Reserved
9-8	TASSEL	RW	0h	Timer_A clock source select 00b = TAxCLK 01b = ACLK 10b = SMCLK 11b = INCLK
7-6	ID	RW	0h	Input divider. These bits along with the TAIDEX bits select the divider for the input clock. 00b = /1 01b = /2 10b = /4 11b = /8
5-4	MC	RW	0h	Mode control. Setting MCx = 00h when Timer_A is not in use conserves power. 00b = Stop mode: Timer is halted 01b = Up mode: Timer counts up to TAxCCR0 10b = Continuous mode: Timer counts up to 0FFFFh 11b = Up/down mode: Timer counts up to TAxCCR0 then down to 0000h
3	Reserved	RW	0h	Reserved
2	TACLR	RW	0h	Timer_A clear. Setting this bit resets TAxR, the timer clock divider logic, and the count direction. The TACLR bit is automatically reset and is always read as zero.
1	TAIE	RW	0h	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
0	TAIFG	RW	0h	Timer_A interrupt flag 0b = No interrupt pending 1b = Interrupt pending

$$Fclk = CLK_{src} / 2^{ID} / TAIDEX$$

© tj

Timer A

- MSP432 Timer A
  - Counter Register

Figure 17-16. TAxR Register

15	14	13	12	11	10	9	8
TAxR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
TAxR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 17-5. TAxR Register Description

Bit	Field	Type	Reset	Description
15-0	TAxR	RW	0h	Timer_A register. The TAxR register is the count of Timer_A.

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Timer A

- MSP432 Timer A
  - Capture/Compare Control Register

4

Figure 17-17. TAxCCTL0 to TAxCCTL6 Register

15	14	13	12	11	10	9	8
CM		CCIS		SCS	SCCI	Reserved	CAP
rw-0	rw-0	rw-0	rw-0	rw-0	r-0	r-0	rw-0
7	6	5	4	3	2	1	0
OUTMOD			CCIE	CCI	OUT	COV	CCIFG
rw-0	rw-0	rw-0	rw-0	r	rw-0	rw-0	rw-0

4

Table 17-6. TAxCCTL0 to TAxCCTL6 Register Description

Bit	Field	Type	Reset	Description
15-14	CM	RW	0h	Capture mode 00b = No capture 01b = Capture on rising edge 10b = Capture on falling edge 11b = Capture on both rising and falling edges
13-12	CCIS	RW	0h	Capture/compare input select. These bits select the TAxCCR0 input signal. See the device-specific data sheet for specific signal connections. 00b = CCIxA 01b = CCIxB 10b = GND 11b = VCC
11	SCS	RW	0h	Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock. 0b = Asynchronous capture 1b = Synchronous capture

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Timer A

- MSP432 Timer A
  - Capture/Compare Control Register

10	SCCI	RW	0h	Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit.
9	Reserved	R	0h	Reserved. Reads as 0.
8	CAP	RW	0h	Capture mode 0b = Compare mode 1b = Capture mode
7-5	OUTMOD	RW	0h	Output mode. Modes 2, 3, 6, and 7 are not useful for TAxCCR0 because EQUx = EQU0. 000b = OUT bit value 001b = Set 010b = Toggle/reset 011b = Set/reset 100b = Toggle 101b = Reset 110b = Toggle/set 111b = Reset/set
4	CCIE	RW	0h	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0b = Interrupt disabled 1b = Interrupt enabled
3	CCI	R	0h	Capture/compare input. The selected input signal can be read by this bit.
2	OUT	RW	0h	Output. For output mode 0, this bit directly controls the state of the output. 0b = Output low 1b = Output high

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Timer A

- MSP432 Timer A
  - Capture/Compare Control Register

Bit	Field	Type	Reset	Description
1	COV	RW	0h	Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software. 0b = No capture overflow occurred 1b = Capture overflow occurred
0	CCIFG	RW	0h	Capture/compare interrupt flag 0b = No interrupt pending 1b = Interrupt pending

© tj

Timer A

- MSP432 Timer A
  - Capture/Compare Register

Figure 17-18. TAxCCR0 to TAxCCR6 Register 4

15	14	13	12	11	10	9	8
TAxCCRn							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
TAxCCRn							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 17-7. TAxCCR0 to TAxCCR6 Register Description 4

Bit	Field	Type	Reset	Description
15-0	TAxCCR0	RW	0h	Compare mode: TAxCCRn holds the data for the comparison to the timer value in the Timer_A Register, TAxR. Capture mode: The Timer_A Register, TAxR, is copied into the TAxCCRn register when a capture is performed.

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Timer A

- MSP432 Timer A
  - Interrupt Register

Figure 17-19. TAxIV Register

15	14	13	12	11	10	9	8
TAIV							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
TAIV							
r0	r0	r0	r0	r-0	r-0	r-0	r0

Table 17-8. TAxIV Register Description

Bit	Field	Type	Reset	Description
15-0	TAIV	R	0h	Timer_A interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: Capture/compare 1; Interrupt Flag: TAxCCR1 CCIFG; Interrupt Priority: Highest 04h = Interrupt Source: Capture/compare 2; Interrupt Flag: TAxCCR2 CCIFG 06h = Interrupt Source: Capture/compare 3; Interrupt Flag: TAxCCR3 CCIFG 08h = Interrupt Source: Capture/compare 4; Interrupt Flag: TAxCCR4 CCIFG ~~0Ah = Interrupt Source: Capture/compare 5; Interrupt Flag: TAxCCR5 CCIFG~~ ~~0Ch = Interrupt Source: Capture/compare 6; Interrupt Flag: TAxCCR6 CCIFG~~ 0Eh = Interrupt Source: Timer overflow; Interrupt Flag: TAxCTL TAIFG; Interrupt Priority: Lowest

Timer A

- MSP432 Timer A
  - Clock Divider Register

Figure 17-20. TAxEX0 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved					TAIDEX[1]		
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0

(1) After programming TAIDEX bits and configuration of the timer, set TACLR bit to ensure proper reset of the timer divider logic.

Table 17-9. TAxEX0 Register Description

Bit	Field	Type	Reset	Description
15-3	Reserved	R	0h	Reserved. Reads as 0.
2-0	TAIDEX	RW	0h	Input divider expansion. These bits along with the ID bits select the divider for the input clock. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b = Divide by 5 101b = Divide by 6 110b = Divide by 7 111b = Divide by 8

$Fclk = CLK_{src} / 2^{ID} / TAIDEX$

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