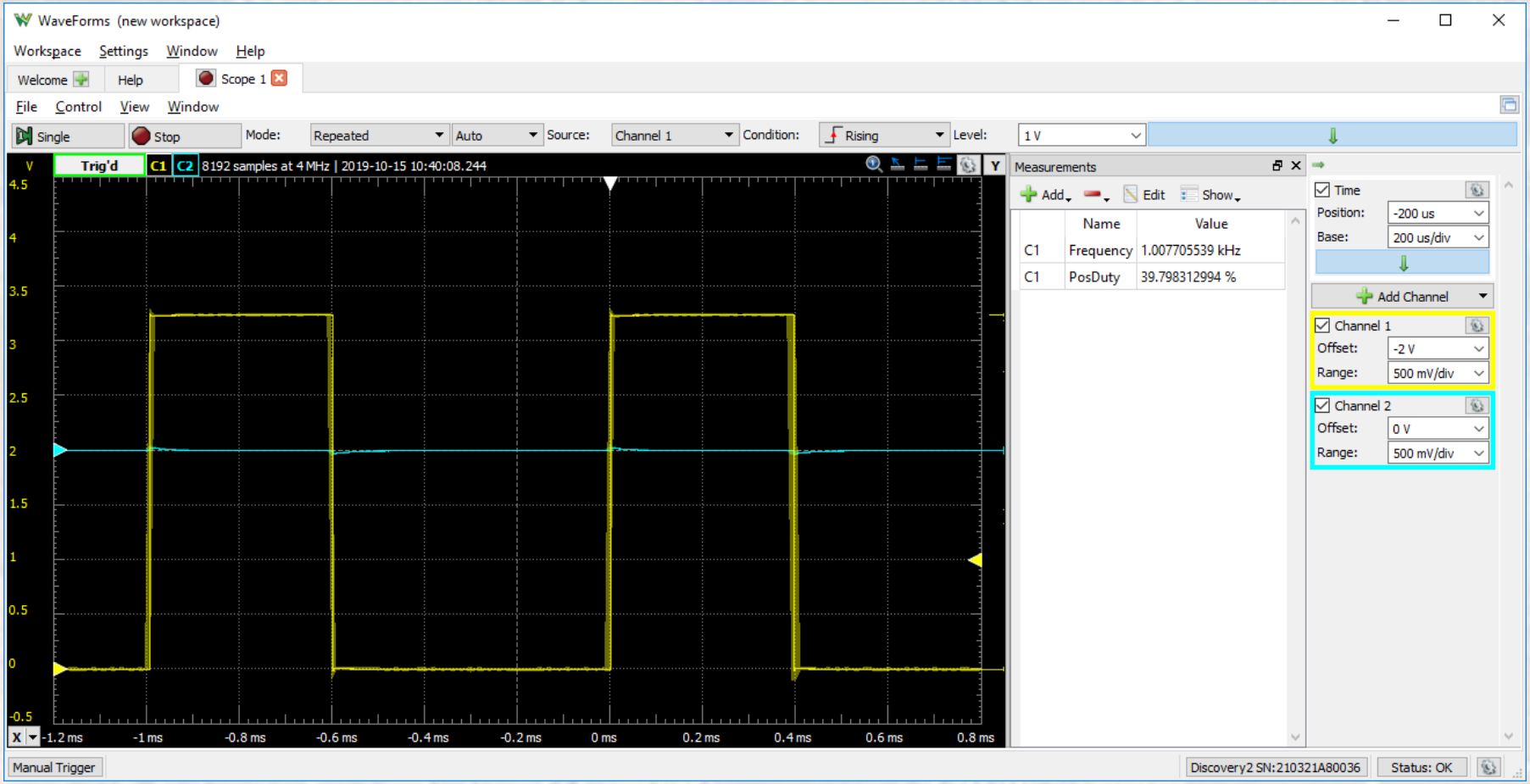
Timer A

Last updated 8/7/18

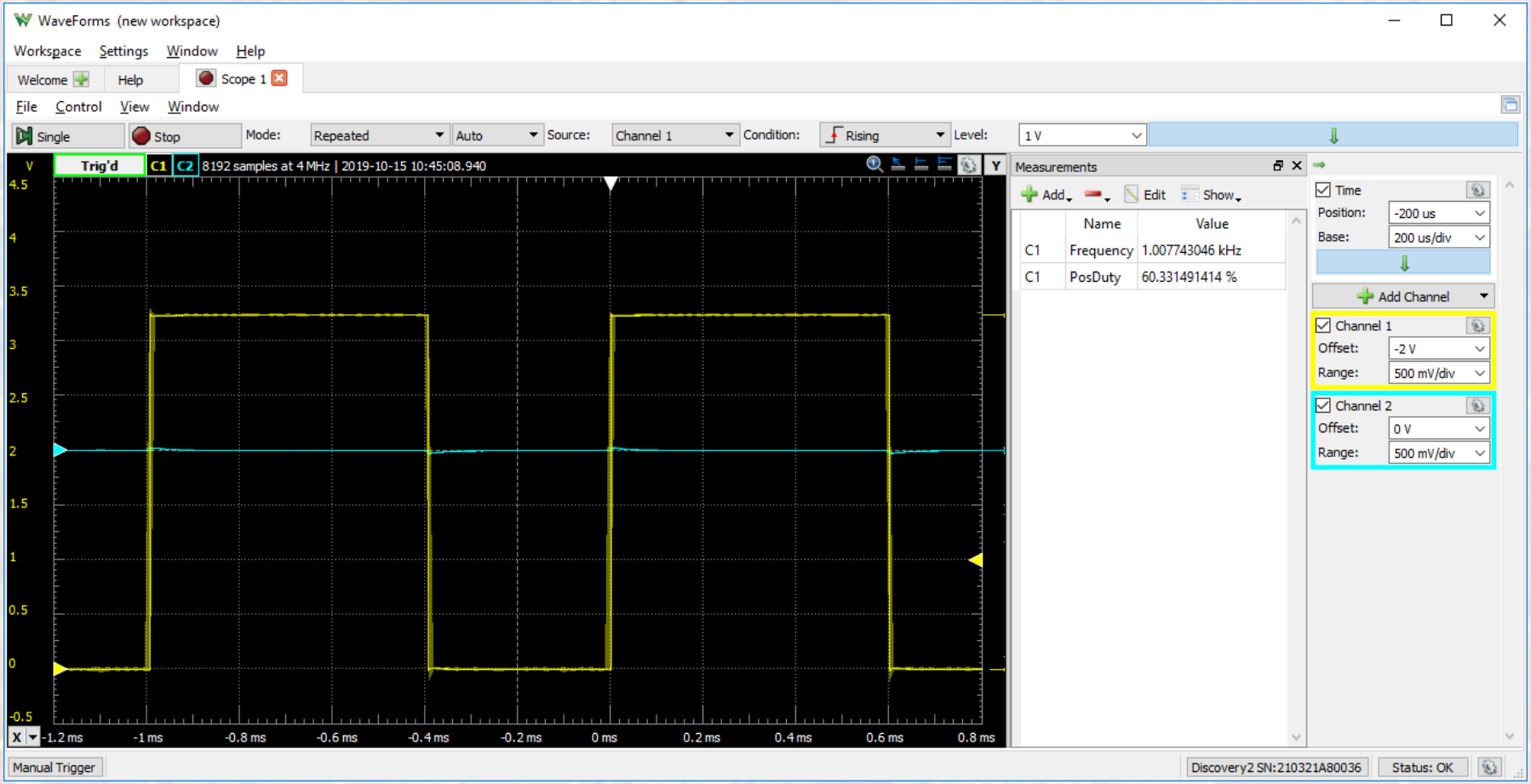
Timer_A Examples

- 40% duty cycle bit-banged output – method 1



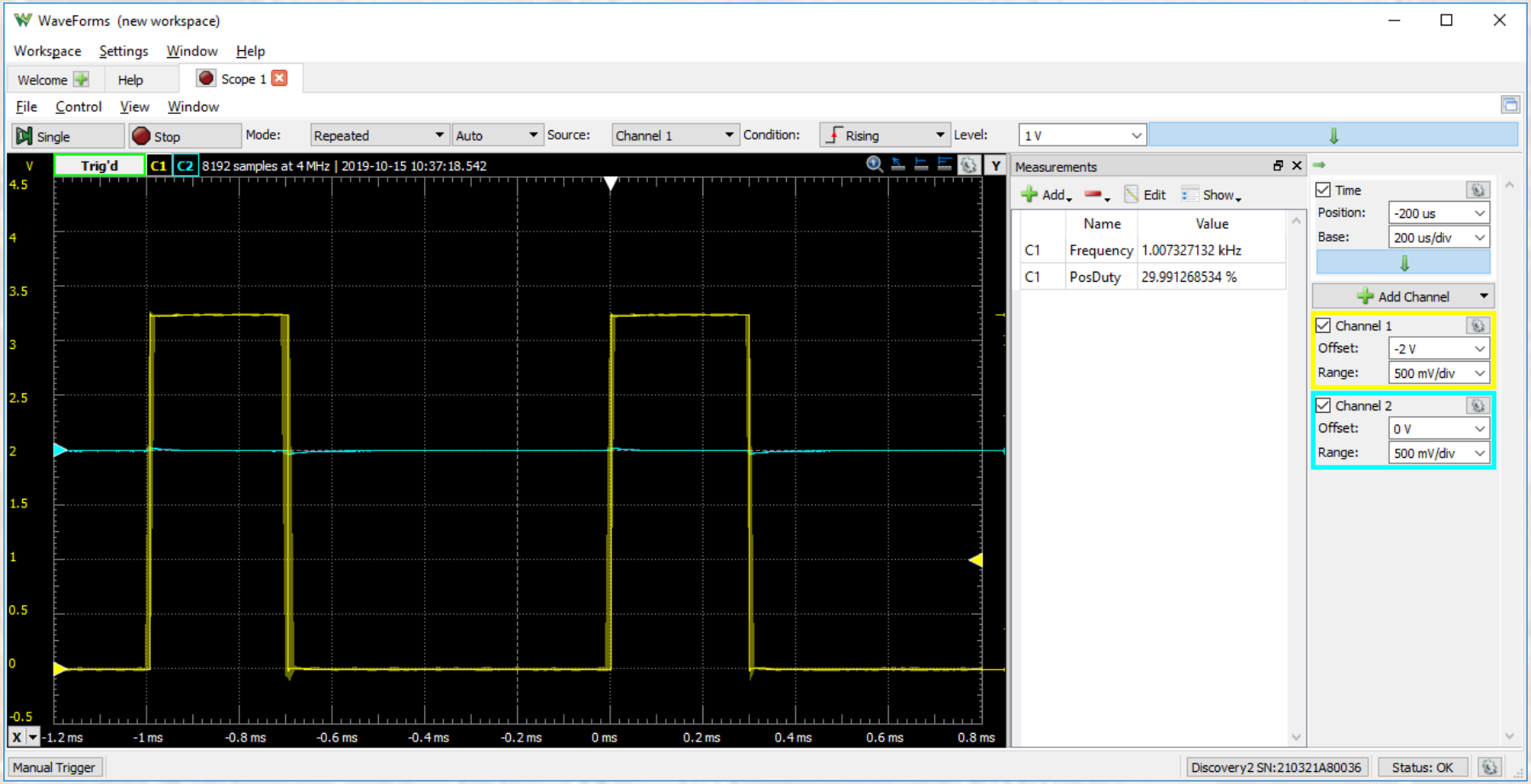
Timer_A Examples

- 60% duty cycle bit-banged output – method 2



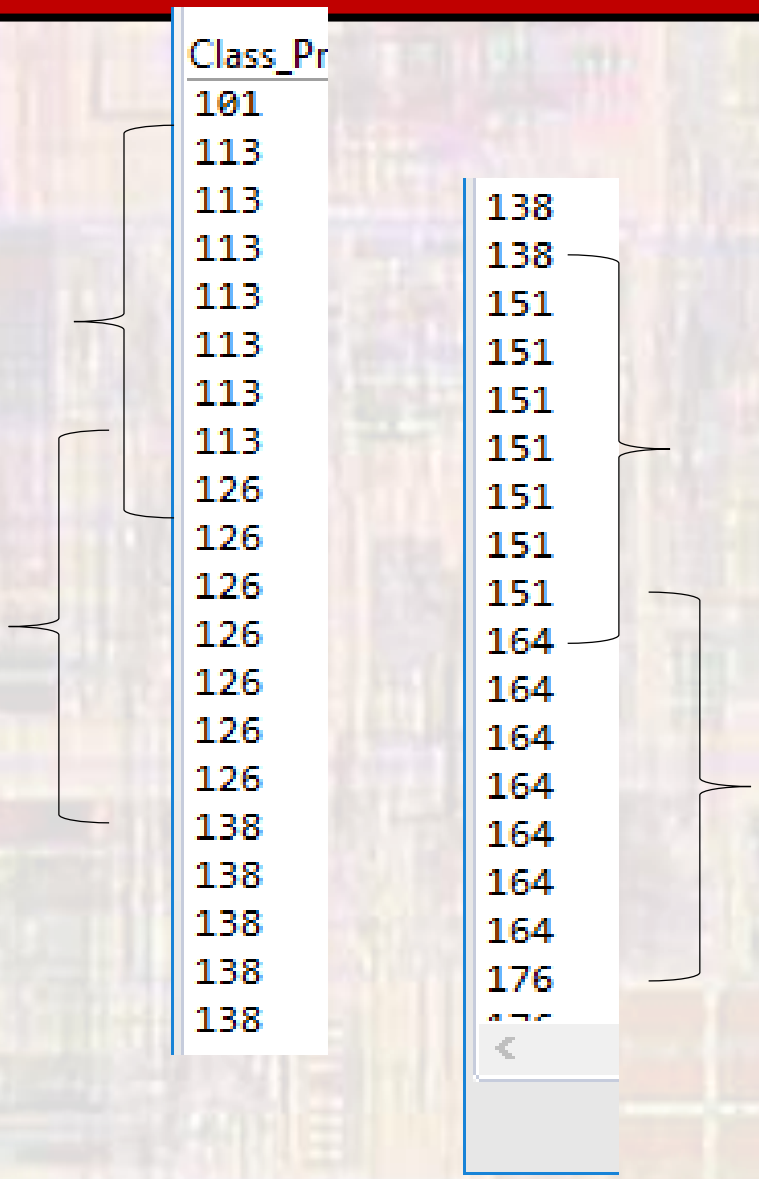
Timer_A Examples

- xx% duty cycle PWM (30%)



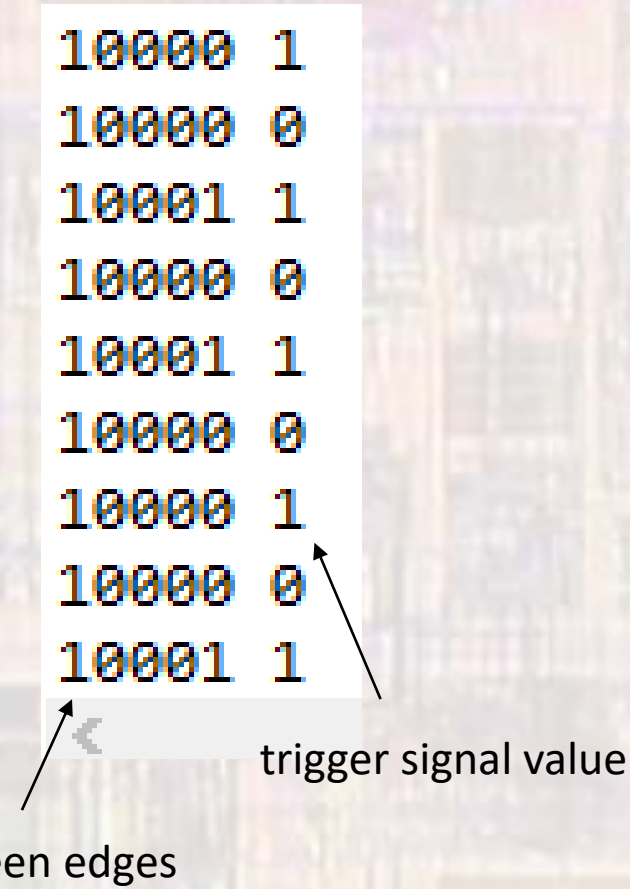
Timer_A Examples

- Input Capture
  - 3MHz/12 clk
    - 4us period
  - Both edges
  - 10KHz input signal
    - 100us period
    - 50us between edges
  - 12.5 clks /edge
  - 25 clks every other edge



Timer_A Examples

- Input Capture 2
  - 3MHz/12 clk
    - 4us period
  - Both edges
  - 12.5Hz input signal
    - 80ms period
    - 40ms between edges
  - 10000 clks /edge



Timer_A Examples

- Clock input example
  - 2KHz PWM signal
  - Used as clock input to second counter
  - Count edges in 5 sec period

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Class_Project:CIO
Counts in 5 sec = 9993, frequency = 1998Hz
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