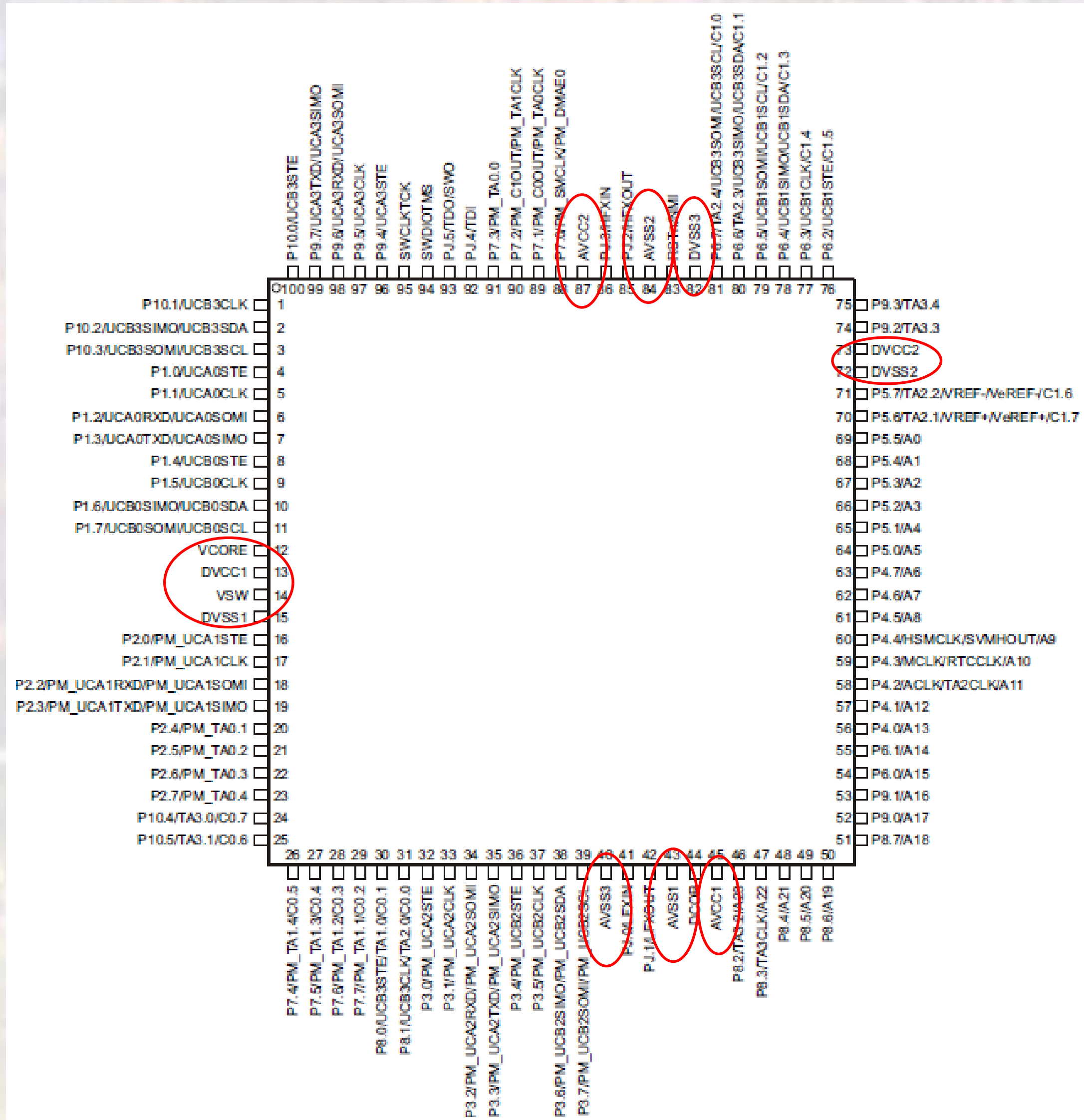
Voltage Supplies

Last updated 6/17/19

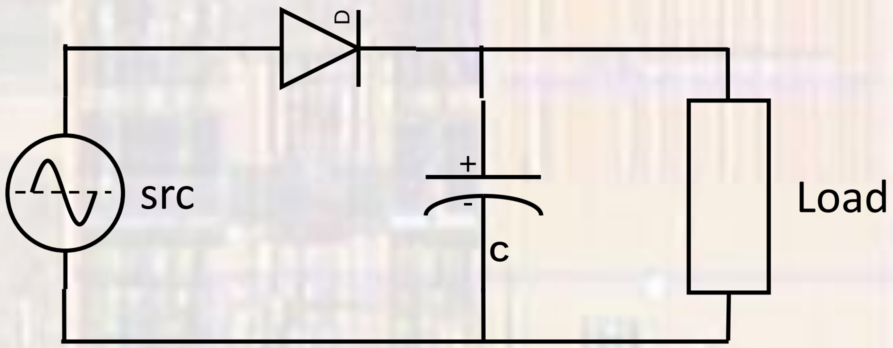
Voltage Supplies

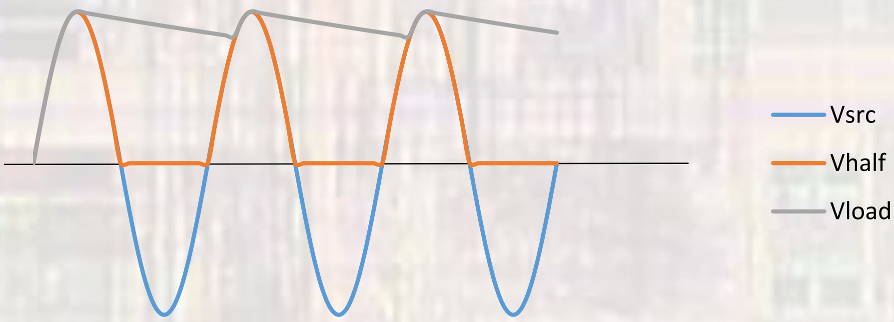
- Pinout



Voltage Supplies

- Rectifiers
  - Convert AC to DC
  - Half Wave topology

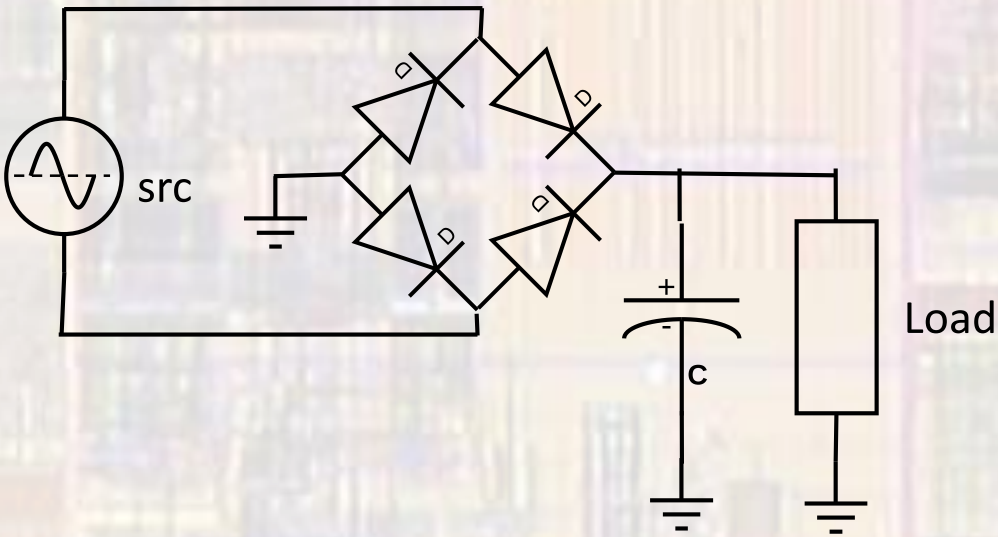


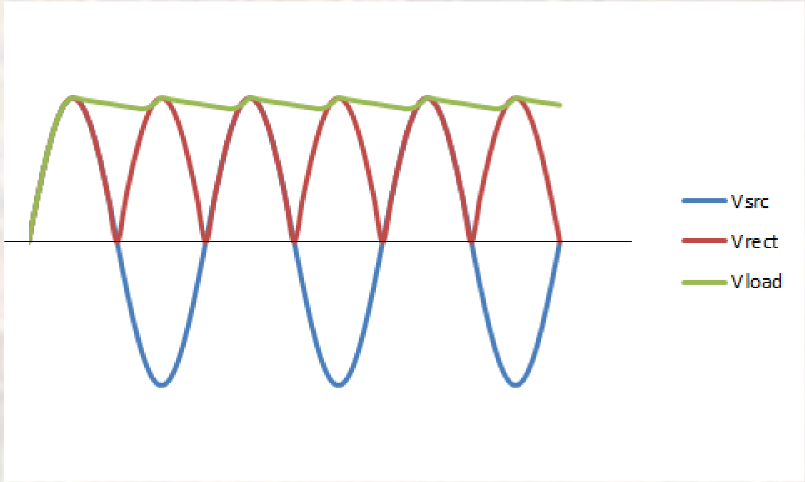


Ideal Diode

Voltage Supplies

- Rectifiers
  - Convert AC to DC
  - Full Wave topology



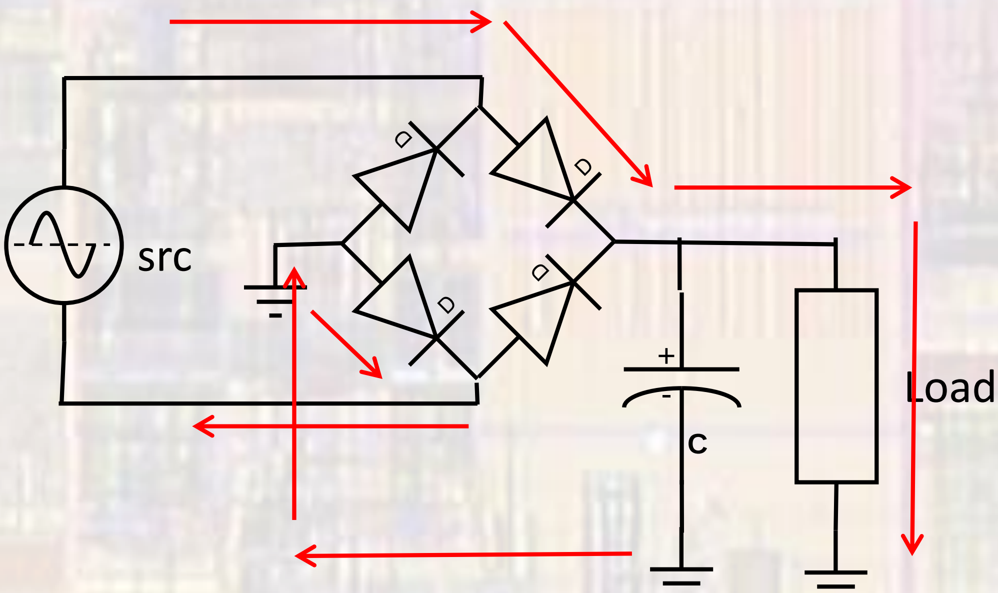


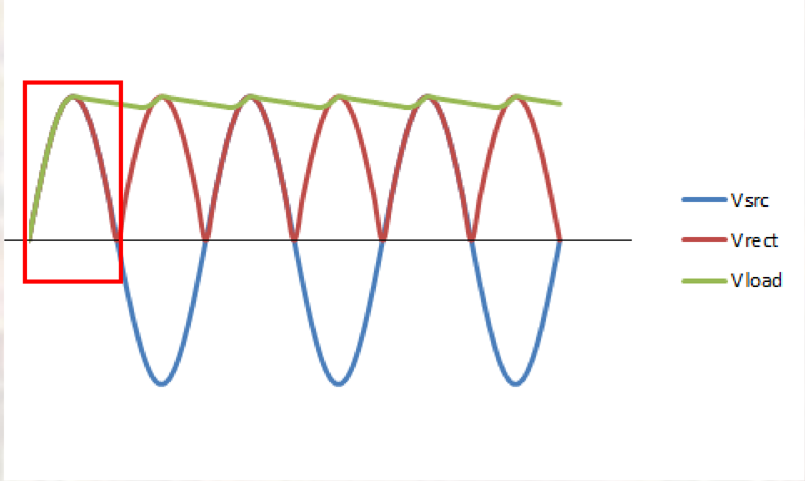
Ideal Diode

Voltage Supplies

- Rectifiers
  - Convert AC to DC

  - Full Wave topology – positive half cycle

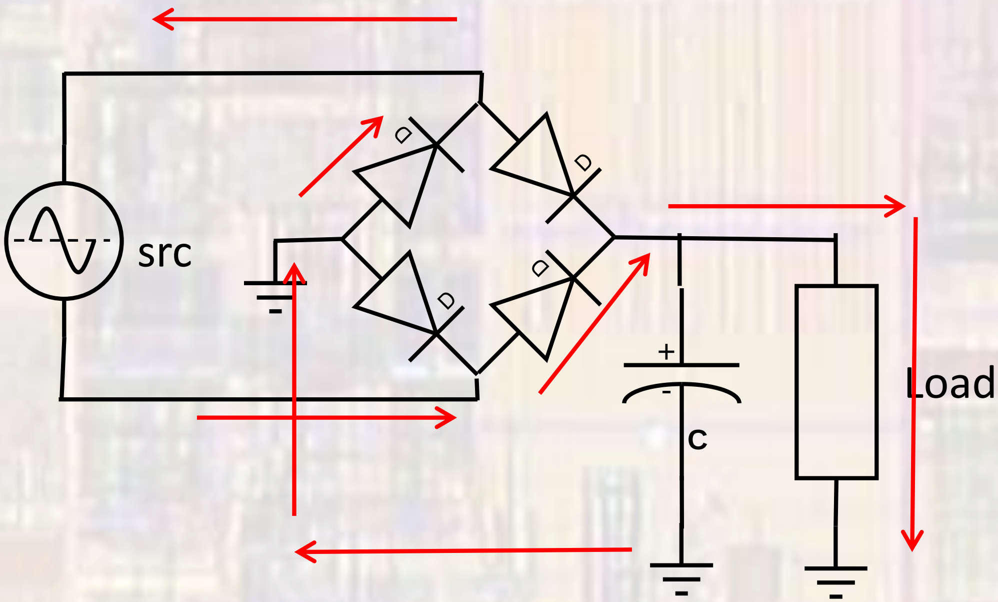


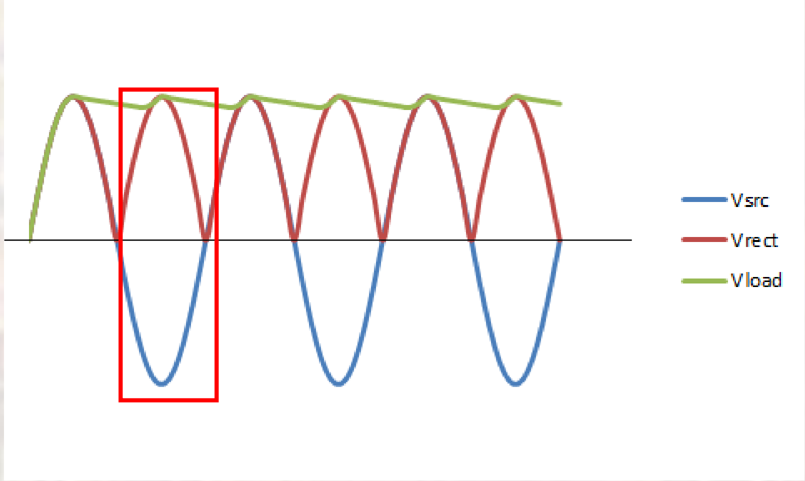


Ideal Diode

Voltage Supplies

- Rectifiers
  - Convert AC to DC
  - Full Wave topology – negative half cycle

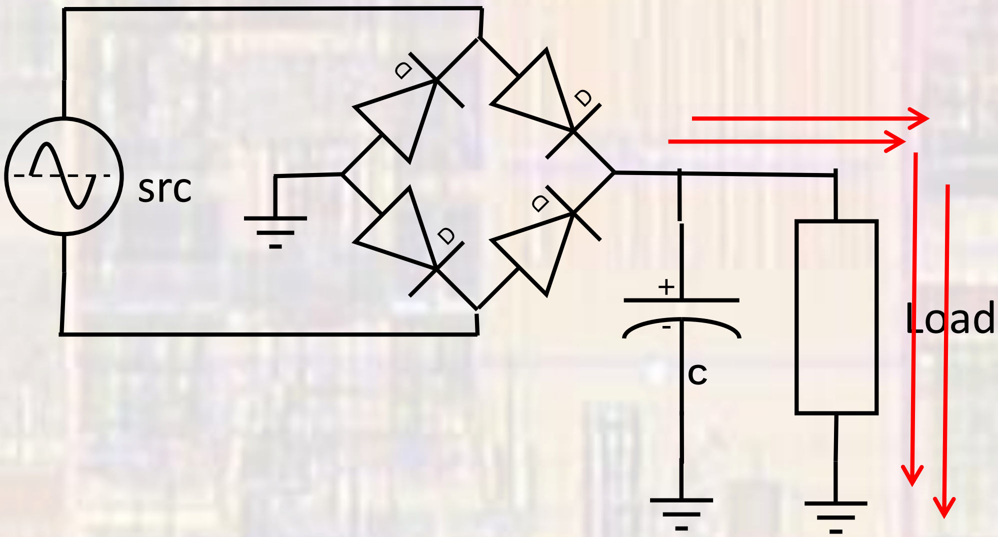


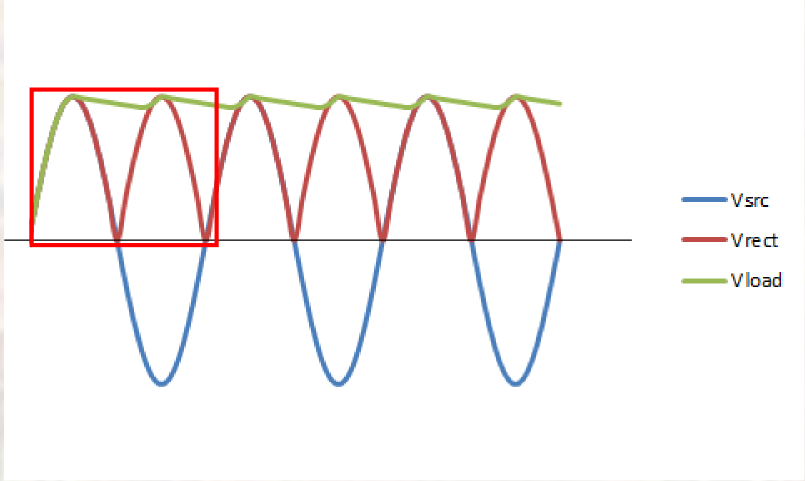


Ideal Diode

Voltage Supplies

- Rectifiers
  - Convert AC to DC
  - Full Wave topology – both cycles provide current to the load



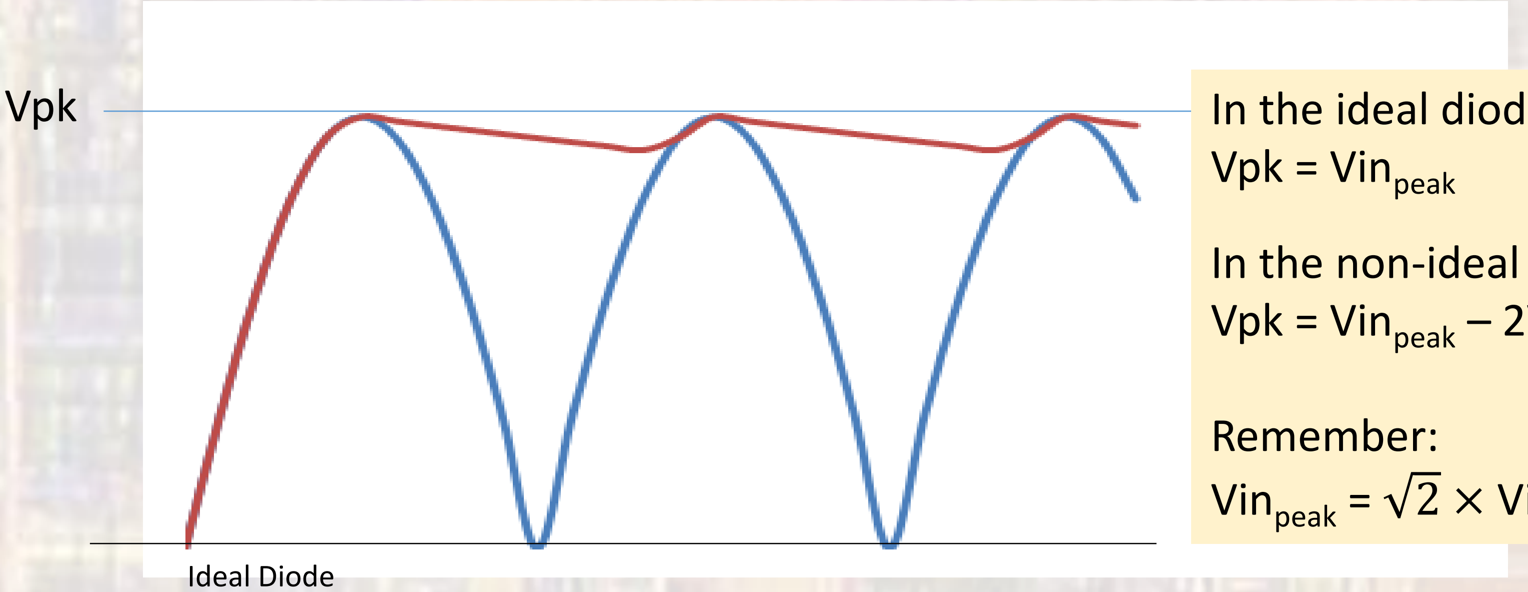


Ideal Diode

Voltage Supplies

- Rectifiers
  - Convert AC to DC

  - Full Wave topology – Vpeak (Vpk)



In the ideal diode case:
$Vpk = Vin_{peak}$

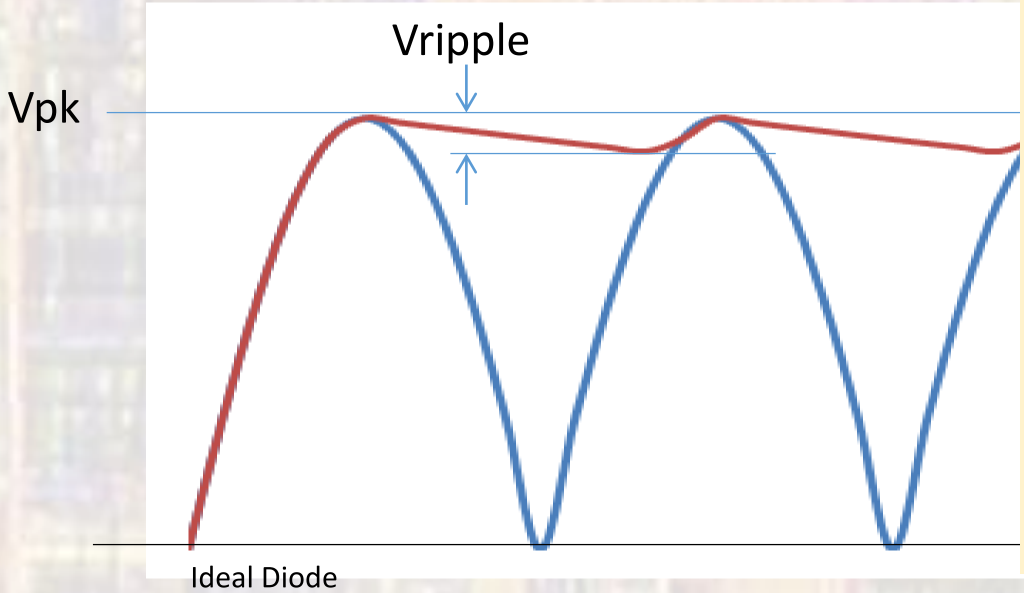
In the non-ideal diode case:
$Vpk = Vin_{peak} - 2Vd$

Remember:
$Vin_{peak} = \sqrt{2} \times Vin_{rms}$

Voltage Supplies

- Rectifiers
  - Convert AC to DC

  - Full Wave topology – Vripple



Assume a resistive load R_L

R_L and C form an RC circuit with time constant $\tau = R_L C$

$$Vout = Vpk \times e^{-t/\tau}$$

during the decay time

so

$$Vripple < 2 \times Vpk \times (1 - e^{-T/4\tau})$$

where T is the period of the input sine wave

Voltage Supplies

- Rectifiers
  - Example

    - A 100Hz, $8v_{rms}$ sine wave is rectified using an ideal full wave rectifier. Assuming the load impedance is 1KΩ and the filter capacitor is 100uF:

      1) what is the approximate amount of ripple on the output?

$8v_{rms}$ → 11.3v peak   100Hz → T=10ms

$\tau = RC = (100uF)(1K\Omega) = 100ms$

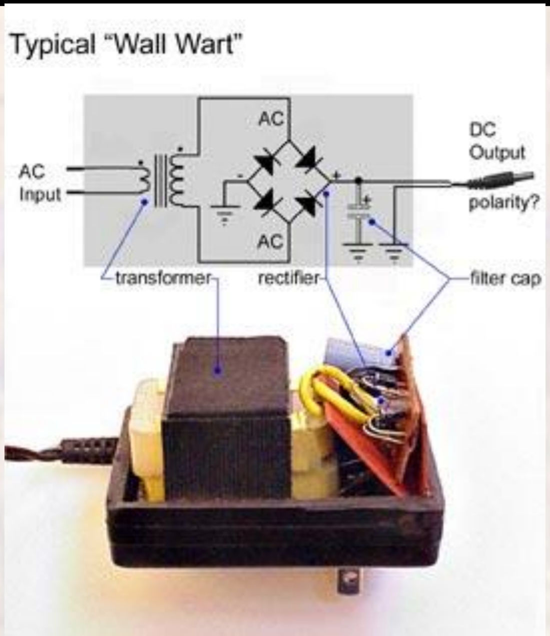
$$Vripple < 2 \times Vpk \times (1 - e^{-T/4\tau})$$

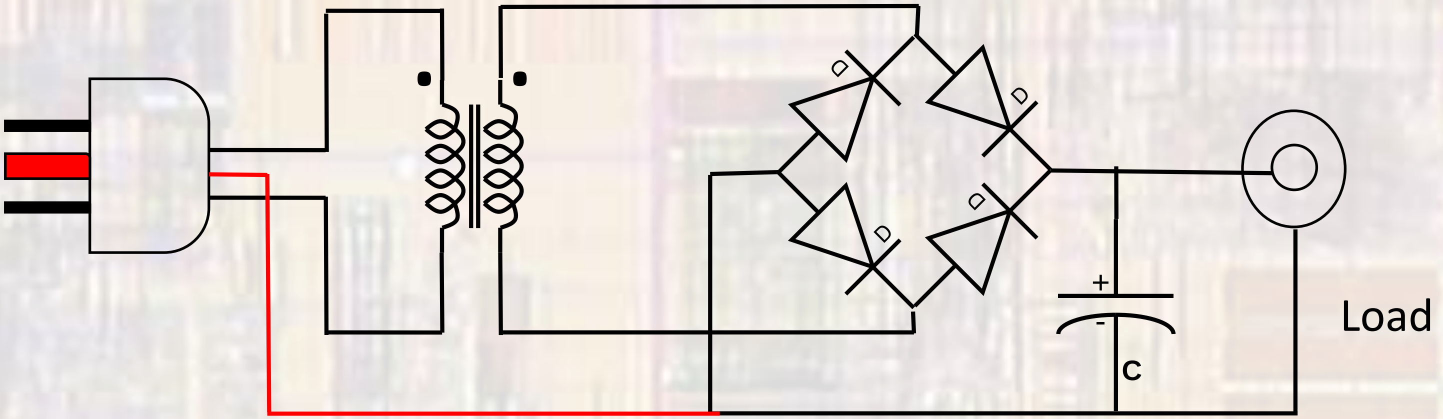
$$Vripple < 2 \times 11.3v \times (1 - e^{-10ms/4(100ms)}) = 558mv$$

$Vout_{min}$ = Vpeak – Vripple = 11.3v – 558mv = 10.74v

Voltage Supplies

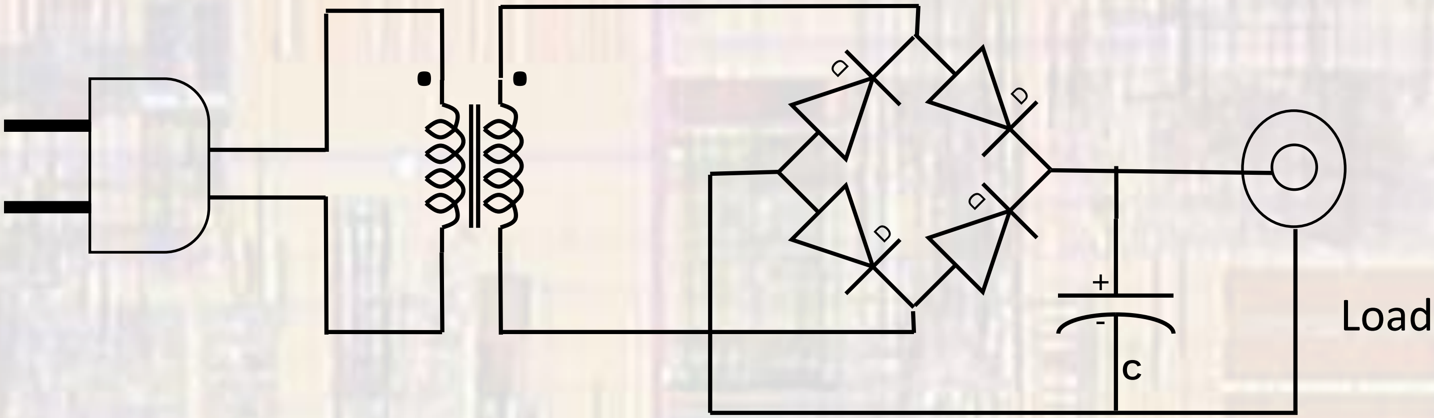
- Unregulated Supply
  - Wall Wart





Voltage Supplies

- Unregulated Supply
  - Wall Wart
  - US residential power standards
    - 120vrms +/- 5% → 114vrms – 126vrms
    - 60Hz +/- 0.05Hz

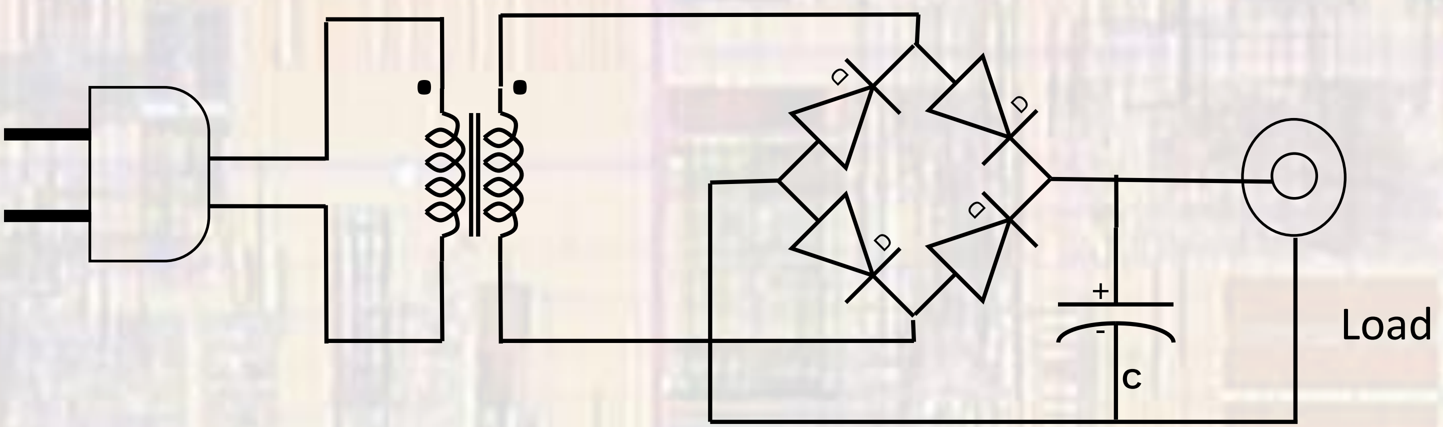


Voltage Supplies

- Unregulated Supply

  - Example
    - Desire 12v dc output from a typical wall wart

assume Vd = 0.7v for the diodes → need 12v + 1.4v = 13.4v for Vpk
allow for 200mv of ripple → 13.4v + 0.2v = 13.6v for Vpk
Vpk = 13.6v → 9.61v_{rms} for the transformer output
9.61vrms → 120vrms / 9.61vrms = 12.48 turns ratio for the transformer



Voltage Supplies

This design actually varies from 13.1V at high temp, low load, to 8.7V at low temp, high load
50% variation
→ need regulation

- Unregulated Supply
  - Example
    - Desire 12v dc output from a typical wall wart

assume Vd = 0.7v for the diodes → need 12v + 1.4v = 13.4v for Vpk
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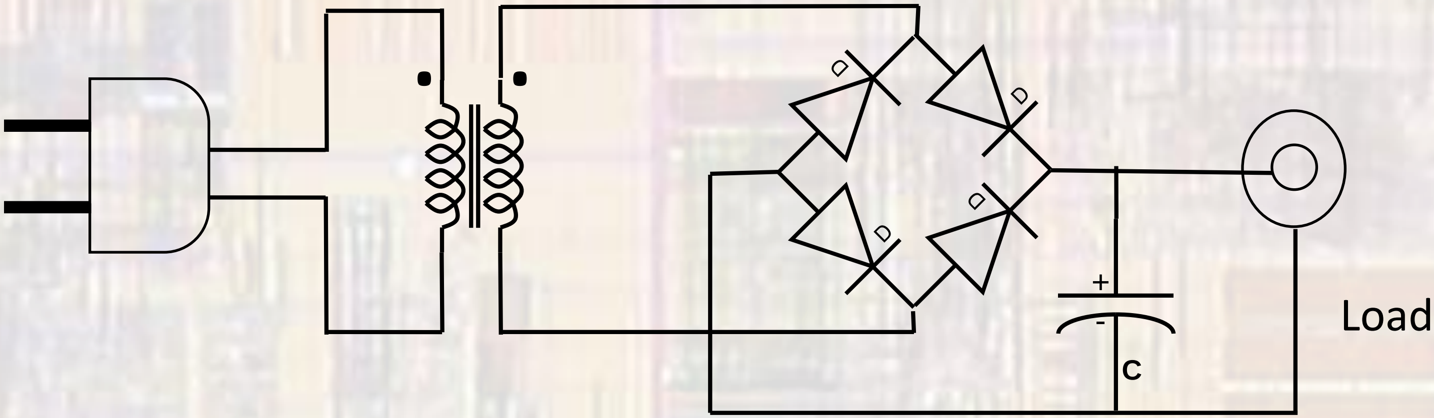
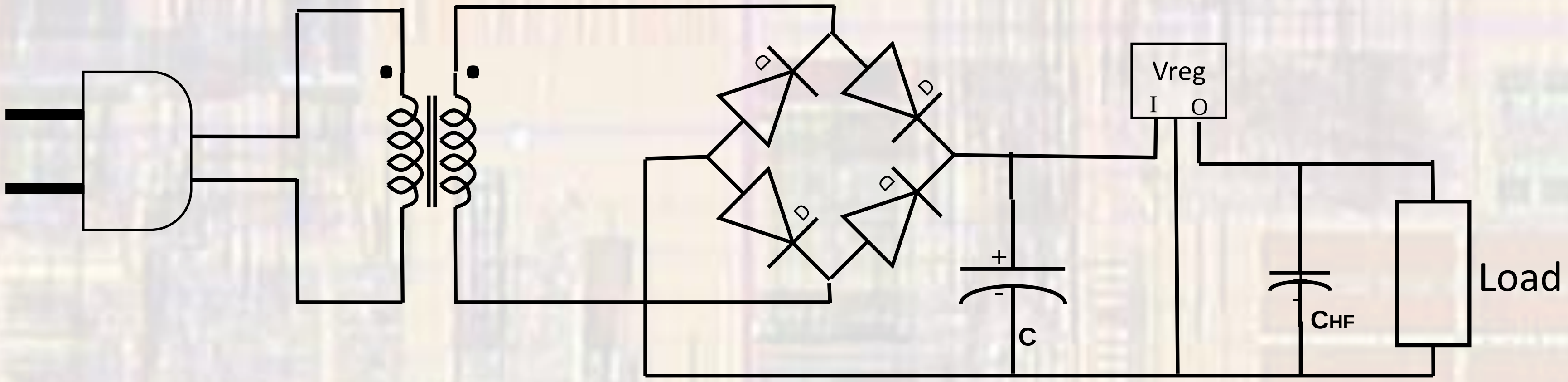


Voltage Supplies

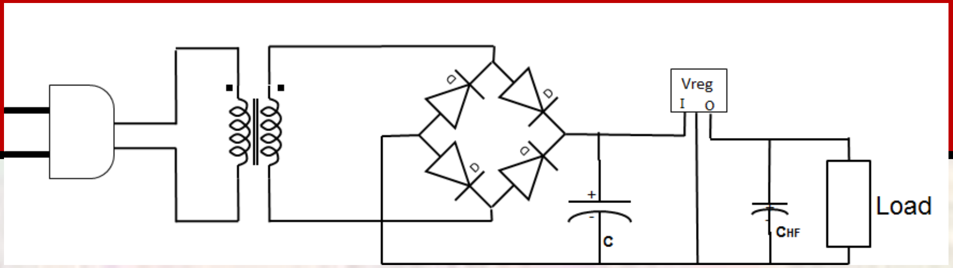
- Regulated Supply

Need something to control the output voltage over variations of temperature, input voltage and load

- Linear voltage regulator
    - uses active circuitry to maintain the output voltage
    - LDO – Low Drop Out versions require minimal overhead voltage



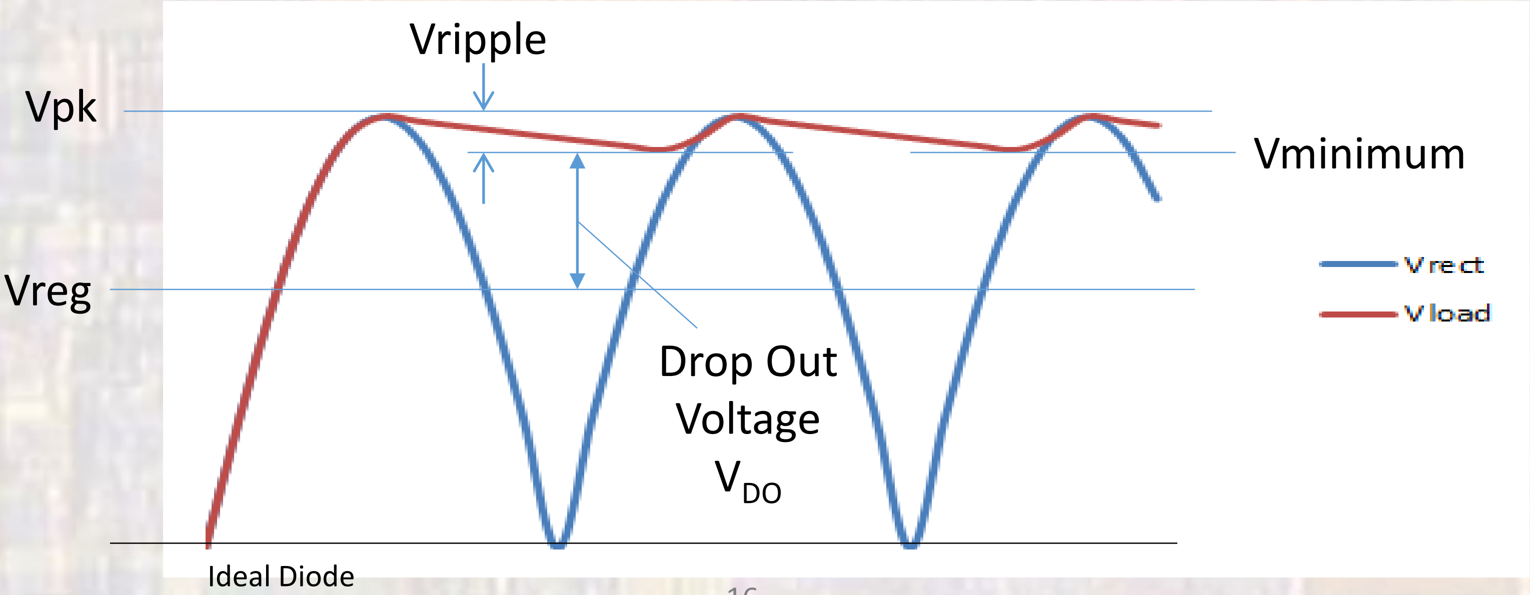
Voltage Supplies



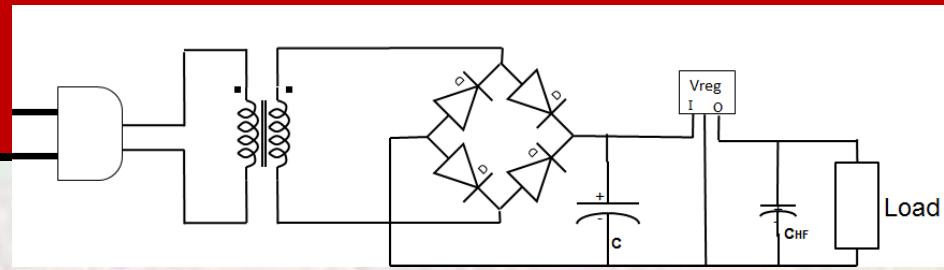
- Regulated Supply

  Need something to control the output voltage over variations of temperature, input voltage and load

  - Linear voltage regulator
    - Design the filter cap and transformer to ensure Vminimum is greater than Vreg + V_{DO}
    - The regulator will then maintain the output voltage



Voltage Supplies



- Regulated Supply

Need something to control the output voltage over variations of temperature, input voltage and load

- TI LDO Specifications

wide input voltage range

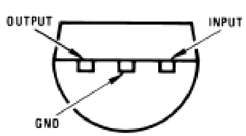
wide load current range

+/- 5% output voltage

1 - 1.5% Regulation

2V drop out voltage

Figure 1. SOIC-8 (D) (Top View, Narrow Body)



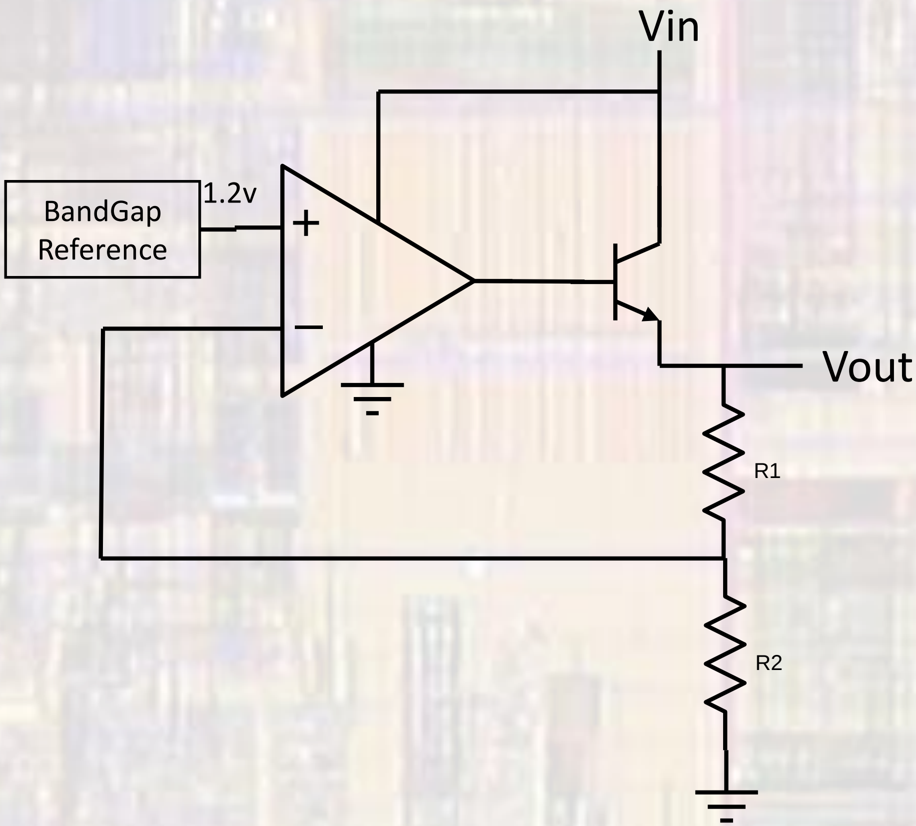
LM78LXX Electrical Characteristics LM78L05AC / LM78L05I

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		4.8	5	5.2	V
		$7V \le V_{IN} \le 20V$ $1mA \le I_O \le 40mA$ (1)	4.75		5.25	
		$1mA \le I_O \le 70mA$ (1)	4.75		5.25	
ΔV_O	Line Regulation	$7V \le V_{IN} \le 20V$		18	75	mV
		$8V \le V_{IN} \le 20V$		10	54	
ΔV_O	Load Regulation	$1mA \le I_O \le 100mA$		20	60	
		$1mA \le I_O \le 40mA$		5	30	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	$8V \le V_{IN} \le 20V$			1.0	
		$1mA \le I_O \le 40mA$			0.1	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (2)		40		μV
$\Delta V_{IN}/\Delta V_{OUT}$	Ripple Rejection	f = 120 Hz $8V \le V_{IN} \le 16V$	47	62		dB
I_{PK}	Peak Output Current			140		mA
$\Delta V_O/\Delta T$	Average Output Voltage Tempco	$I_O = 5mA$		−0.65		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			6.7	7	V
θ_{JA}	Thermal Resistance (8-Bump micro SMD)			230.9		°C/W

(2) Recommended minimum load capacitance of 0.01μF to limit high frequency noise.

Voltage Supplies

- Regulated Supply
  - Super Simple Regulator



$$\frac{R2}{R1 + R2} Vout = Vbg$$

$$Vout = Vbg \frac{R1 + R2}{R2}$$

Voltage Supplies

- Regulated Supply
  - Simple Regulator

EQUIVALENT CIRCUIT

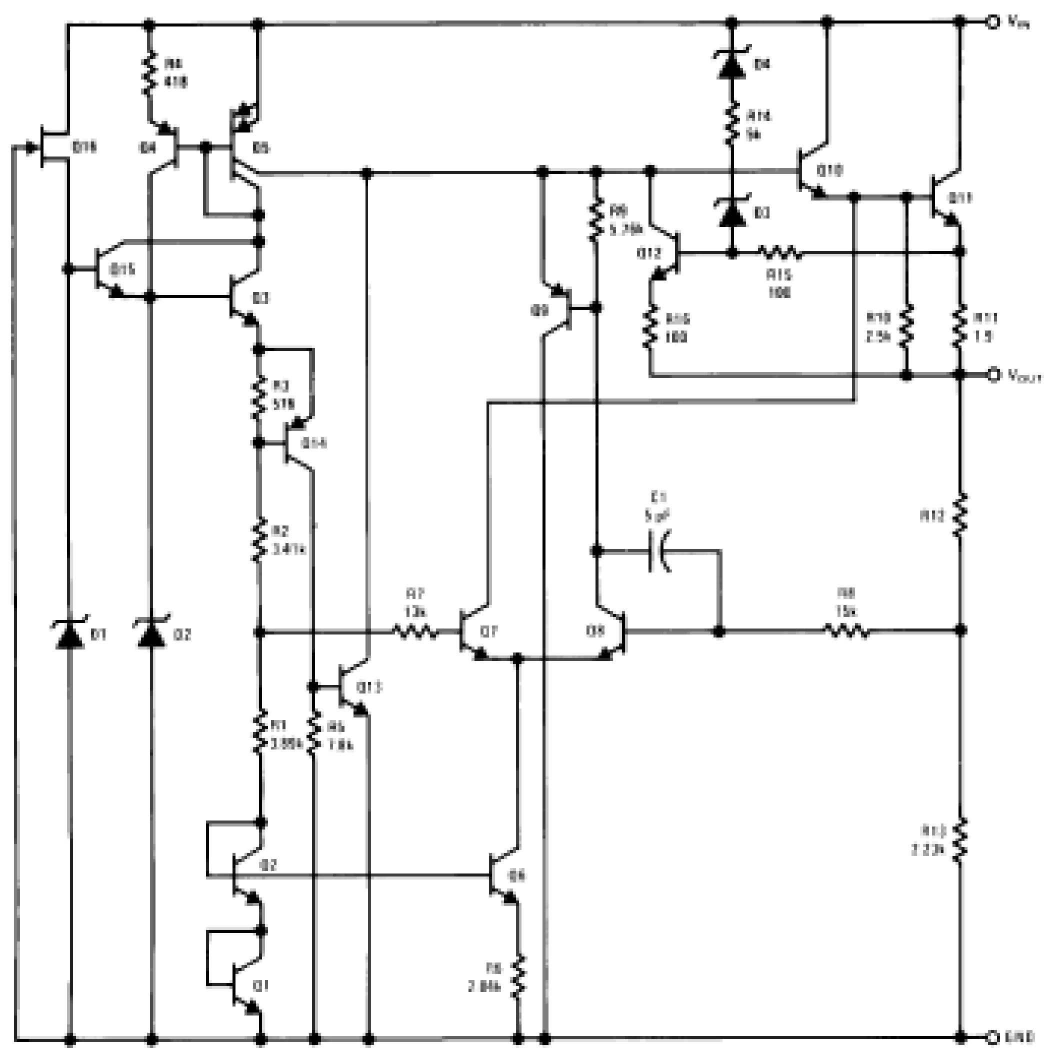
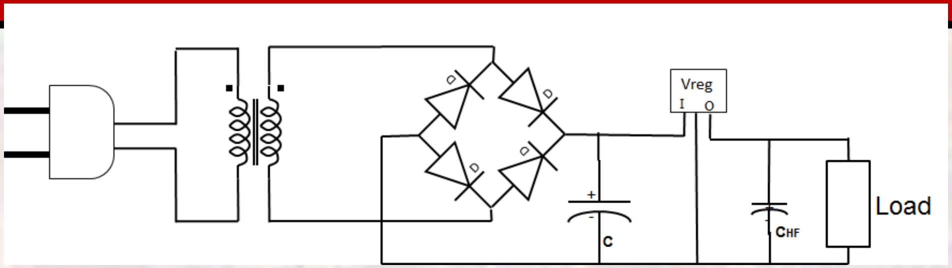


Figure 12. LM78LXX

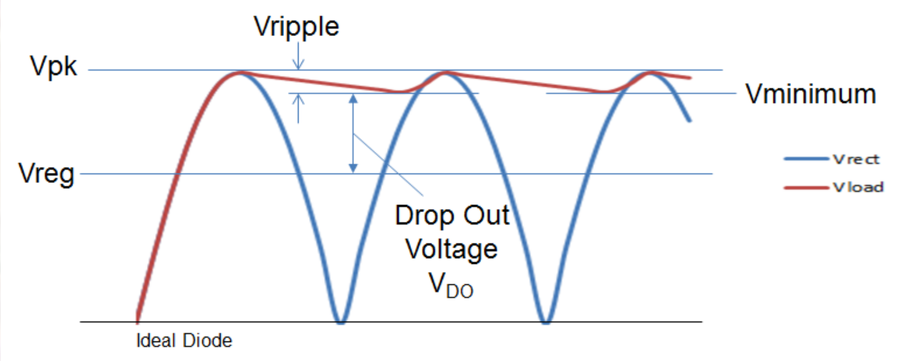
Voltage Supplies



- Regulated Supply
  - Power Considerations
    - With a 12V rectifier output and 50mA load current → Psourced = 600mW
    - In our example the load only sees 5V and 50mA → Pdissipated = 250mW
    - Where does the other power go? → dissipated in the regulator
      - Efficiency = Power provided to the load / total power dissipated

        In this case Efficiency = 42% Over half the power is lost as heat!

Design tradeoff:
More ripple → lower cost components
→ lower efficiency



Voltage Supplies

- Supply Decoupling

  - Digital circuits create current spikes on the supply pins
    - Shoot through current
    - Charging and discharging current
    - I/O switching

  - While the average supply current may be a few tens of milliamps, spikes associated with an 8 bit I/O switching can be hundreds of milliamps and a few nanoseconds wide

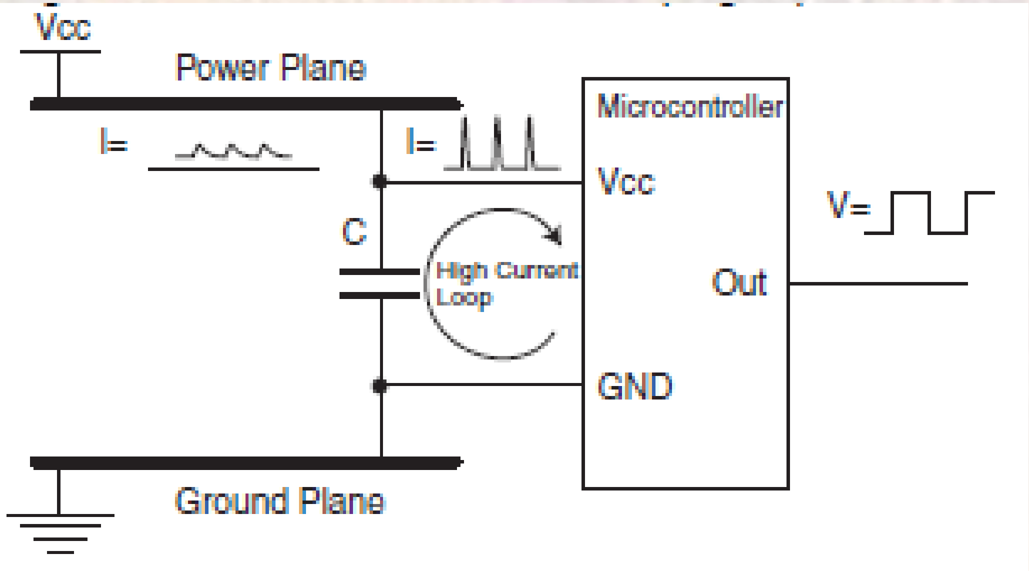
  - Power supplies and realistic circuit board traces cannot support these current spikes → noise on the supply voltage

  - Supply voltage noise can disrupt the normal operation of the processor or other circuits

Voltage Supplies

- Supply Decoupling

  - Coupling (bypass) capacitors are used to supply these spikes of current, preventing noise on the supply voltage pins

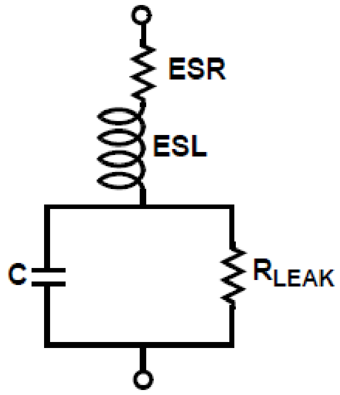


Voltage Supplies

- Supply Decoupling

  - Realistic capacitor model

ABBREVIATION	EXPLANATION	SOURCE AND DETAILS
ESR	Equivalent Series Resistance	Wire and connections to the plate Produces heat
ESL	Equivalent Series Inductance	Depends on package type Surface mount better Smaller SMD better
RLEAK	Leakage Resistance	Type of dielectric



Voltage Supplies

- Supply Decoupling

  - Realistic capacitor model

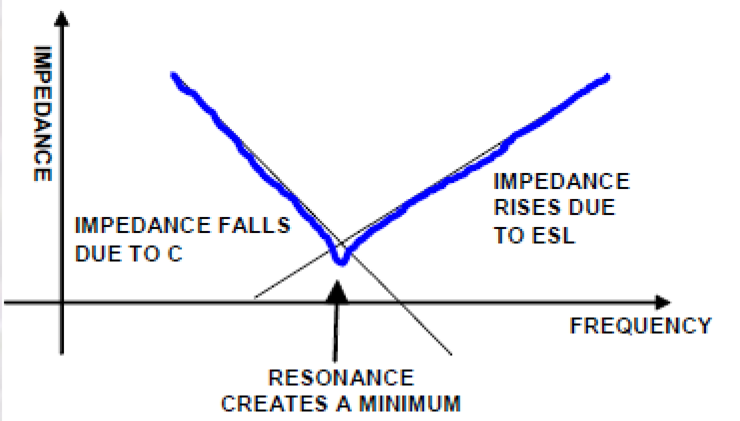


FIGURE 8. IMPEDANCE OF AN ACTUAL CAPACITOR (NON-IDEAL)

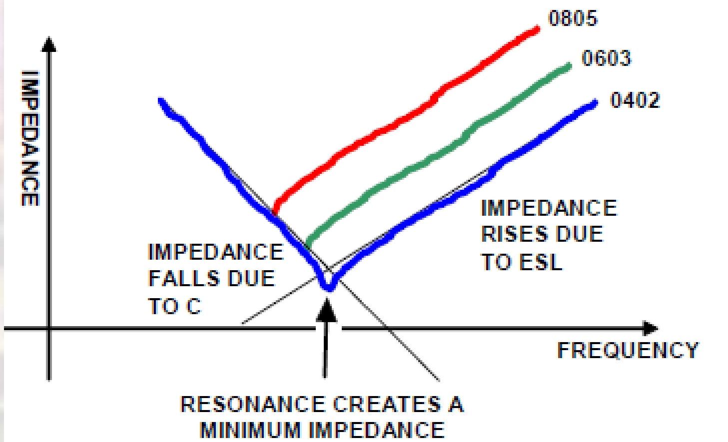


FIGURE 9. IMPEDANCE OF AN ACTUAL CAPACITOR (NON-IDEAL) IN DIFFERENT SURFACE-MOUNT PACKAGES

Voltage Supplies

- Supply Decoupling

  - Realistic capacitor model

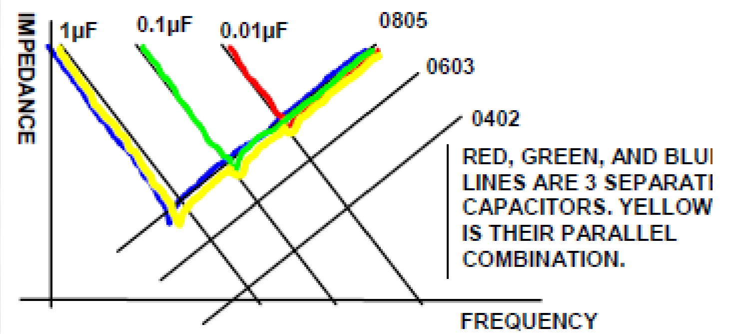


FIGURE 10. IMPEDANCE OF THREE CAPACITORS, THE SAME SURFACE-MOUNT PACKAGES

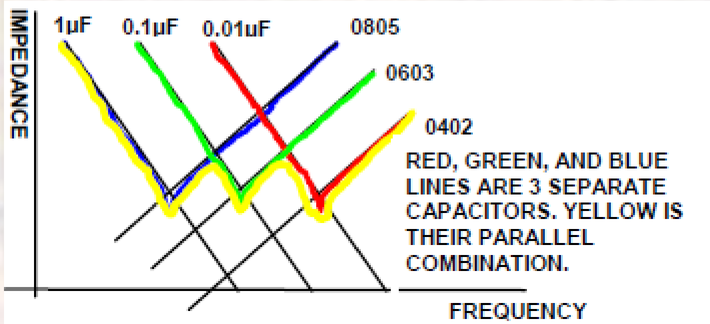


FIGURE 11. IMPEDANCE OF THREE CAPACITORS, SCALED SURFACE-MOUNT PACKAGES

Voltage Supplies

- Supply Decoupling

  - Most systems use 2 decoupling capacitors
    - 1uF - 10uF for low frequency high current spikes
    - .001uF - .01uF for high frequency spikes
  - Placed as close to the IC as possible to reduce inductance

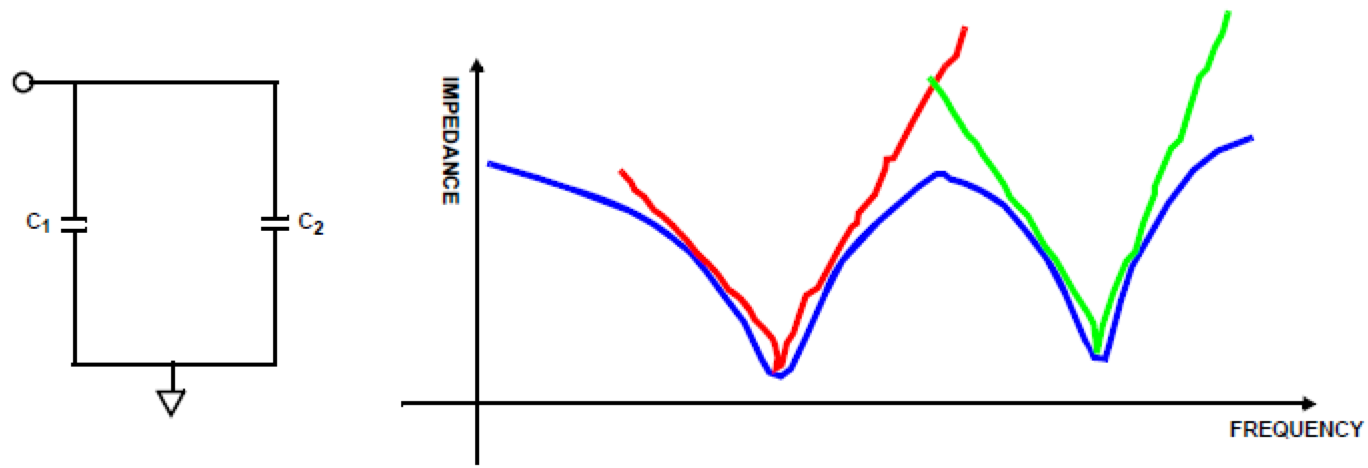


FIGURE 21. FREQUENCY RESPONSE OF TWO SCALED CAPACITORS IN PARALLEL (FOR REFERENCE)