

# FPGA Basics

Last updated 5/19/20

# FPGA MAX10

These slides review the basics of FPGA operation

Upon completion: You should be able to describe the operation of an FPGA device

# FPGA Basics

- Field Programmable Gate Array
  - Long history
    - PROM, PAL, CPLD
    - Gate Array, Standard Cells
- Why FPGAs
  - Rapid prototyping
  - In field test / modification
  - Rapidly changing technology / standard
  - Low / mid volume production
    - High volume → ASIC or ASSP

# FPGA Basics

- Advantages
  - Flexibility
  - Speed to market
  - Well characterized
- Disadvantages
  - COST
  - Maximum clock frequency
  - Power

# FPGA Basics

- Basic Concept
  - Many small fixed circuits
  - +
  - Multiple levels of interconnect
  - +
  - Programmable connections
- Enhancements
  - Fixed IP blocks
    - Memory
    - Processors
    - Interfaces

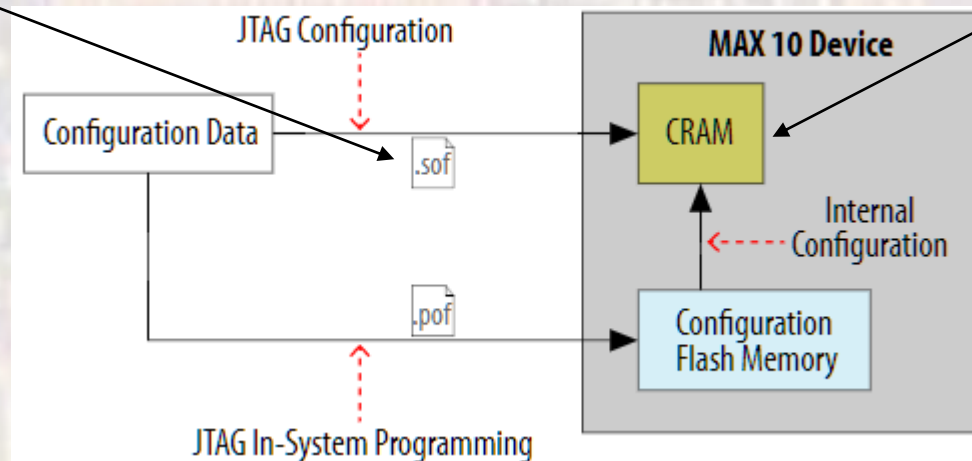
# FPGA Basics

- $FPGA$  – programmable
  - 3 primary programming methods
    - RAM
      - Volatile
      - Must be loaded on power-up
      - Most common
    - Electrically erasable (flash)
      - Non-volatile
      - Expensive
    - Fuse / Anti-fuse
      - Non-volatile

# FPGA Basics

- $FPGA$  – programmable
  - JTAG Programming Configurations
    - Load programming information (xx.sof file)
    - Directly into the Configuration RAM via the JTAG interface
  - Configuration FLASH holds the default program

xx.sof file  
SRAM Object File



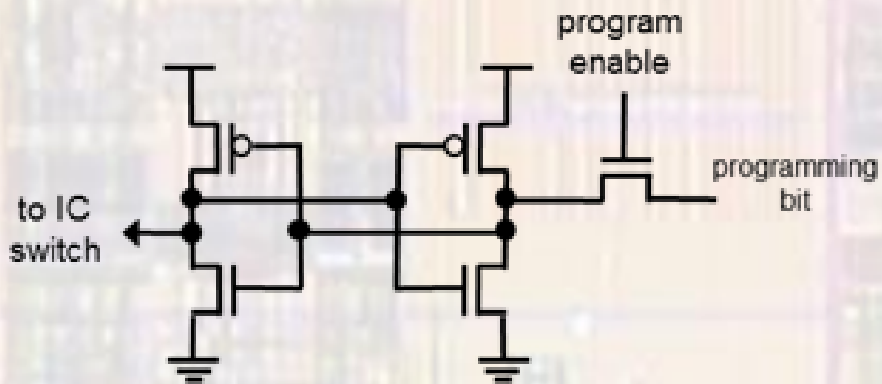
Configuration  
RAM

Src: MAX 10 FPGA Configuration Guide

# FPGA Basics

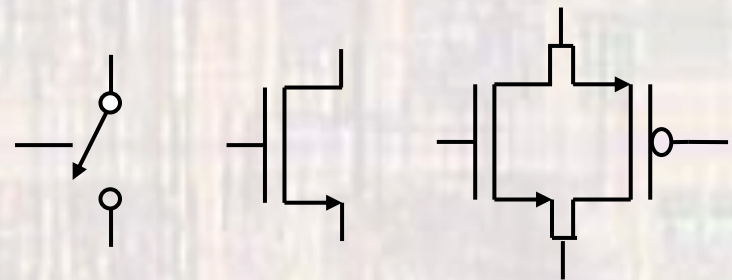
- $\text{FPGA}$  – programmable
  - SRAM based

SRAM programming cell  
(latch)



Src: Altera - PLDBasics\_FPGA\_Architecture

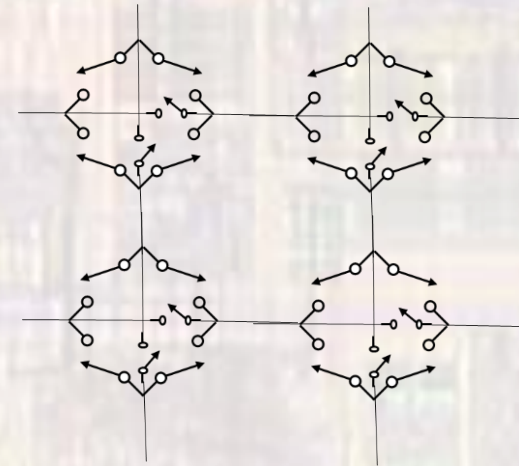
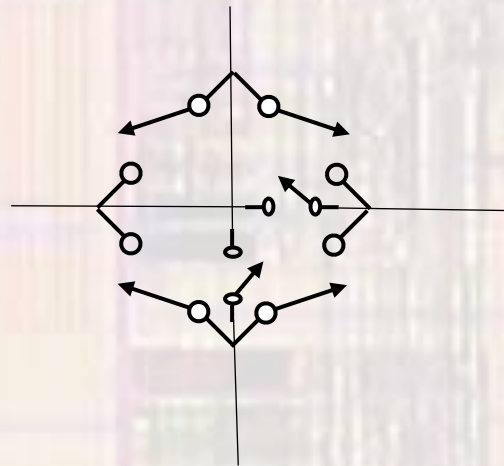
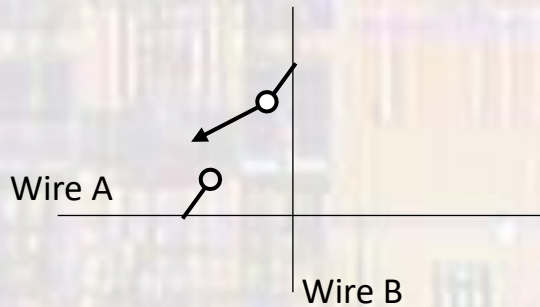
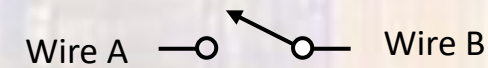
Switches





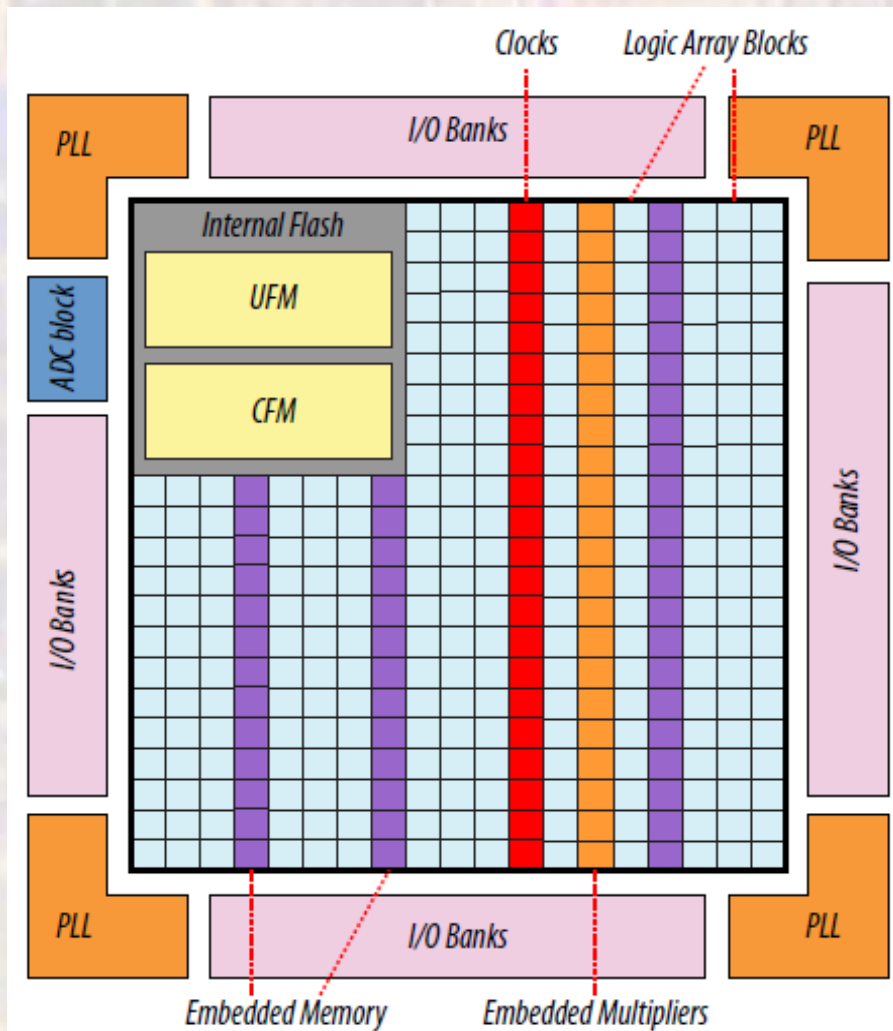
# FPGA Basics

- $FPGA$  – programmable
  - Switch configurations



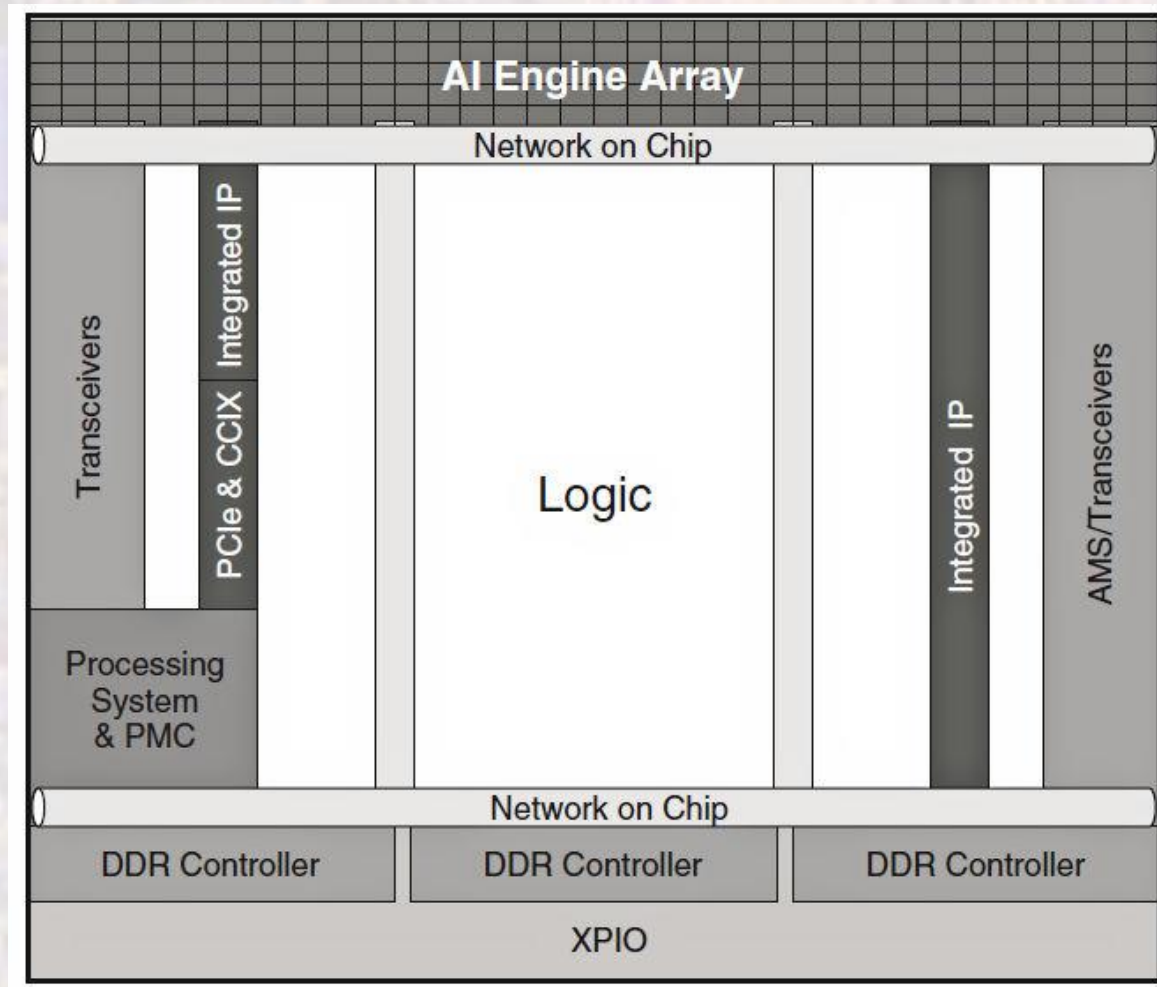
# FPGA Basics

- Intel/Altera Max 10



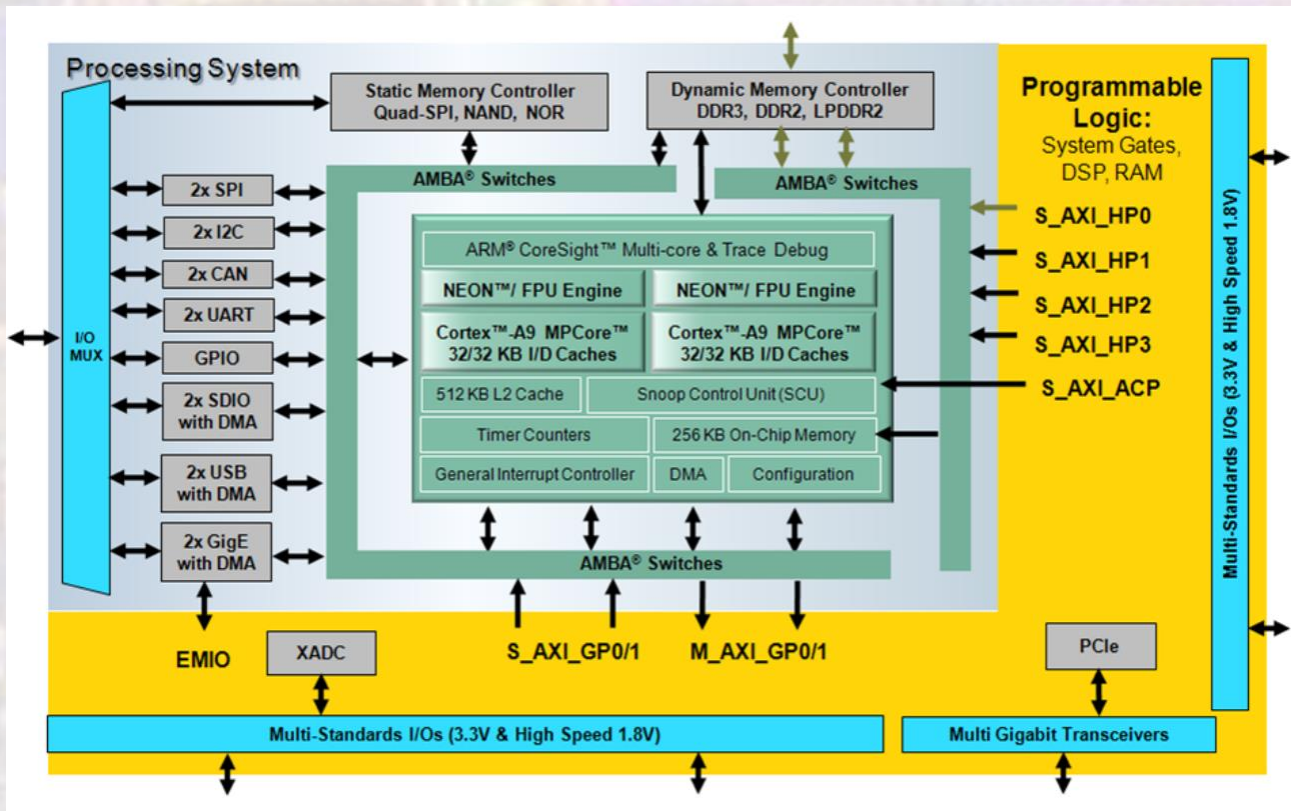
# FPGA Basics

- Xilinx Versal



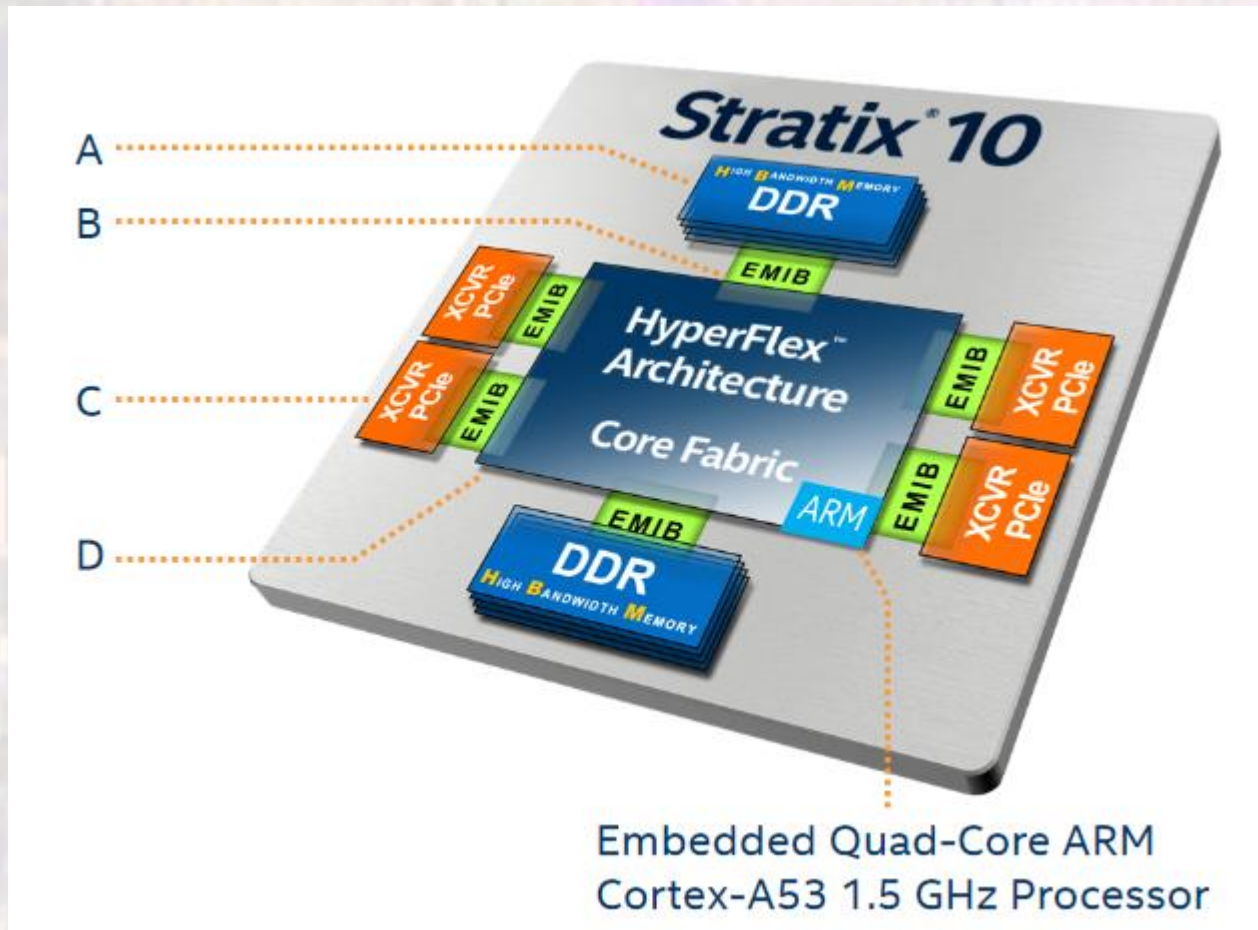
# FPGA Basics

- Xilinx Zynq



# FPGA Basics

- Intel/Altera Stratix 10



# FPGA Basics

- CRAM Configuration

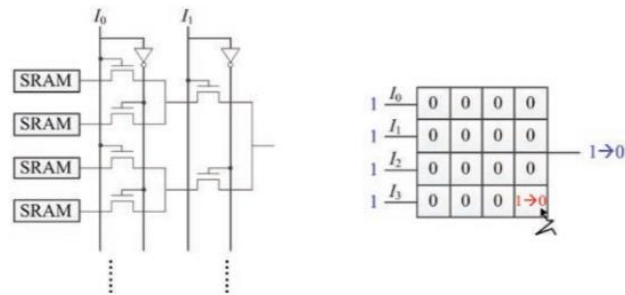


Fig. 2. SEU on an LUT.

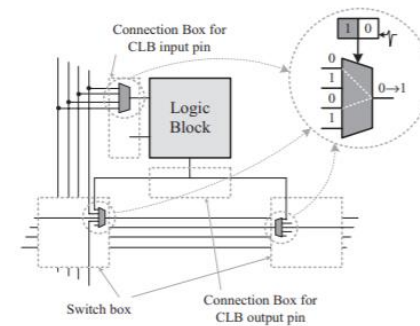


Fig. 7. An SEU on a connection box and switch box in a unidirectional routing architecture.

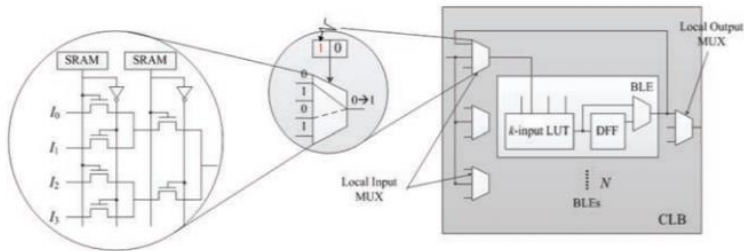


Fig. 3. SEU on an input MUX inside a logic block.

<http://eda.ee.ucla.edu/pub/J73.pdf>