EE 3921

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Homework 3

1) Given the VHDL code below, provide the expected signal values 30 pts

```
----------------------------------
--
--  control_A.vhdl
--
--  by: tj
--
--  created: 9/7/2016
--
--  version: 0.0
--
----------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity control_A is
   generic( N: positive := 8);
   port(
         i_clk:   in std_logic;
         i_rstb:  in std_logic;
         o_one:   out std_logic_vector(N-1 downto 0);
         o_five:  out std_logic_vector(N-1 downto 0)
   );
end entity;
```

```
architecture behavioral of control_A is

   signal signal_1: signed(N-1 downto 0);
   signal signal_5: unsigned(N-1 downto 0);

begin

------------------- part 1
   process (i_clk, i_rstb)
      variable i:    integer;
      variable sig:  integer range -128 to 127;
   begin
      if (i_rstb = '0') then
         sig := 32;
      else
         if (rising_edge(i_clk)) then
            i := 1;
            while (i < 5) loop
               sig := sig - 2;
               i := i + 1;
            end loop;
         end if;
      end if;
      signal_1 <= to_signed(sig, signal_1'length);
   end process;

   o_one <= std_logic_vector(signal_1);

------------------- part 5
   process (i_clk, i_rstb)
      variable i: integer;
   begin
      if (i_rstb = '0') then
         signal_5 <= (others => '0');
      else
         if (rising_edge(i_clk)) then
            i := 8;
            while (i > 2) loop
               signal_5 <= si
               i := i - 1;
            end loop;
         end if;
      end if;
   end process;

   o_five <= std_logic_vector(signal_5);

end architecture;
```

clk1: 32 – 2x4= 24
clk2: 24 – 2x4=16

clk1: 0 + 7 = 7
clk2: 7 + 7 = 14

Only last one gets updated

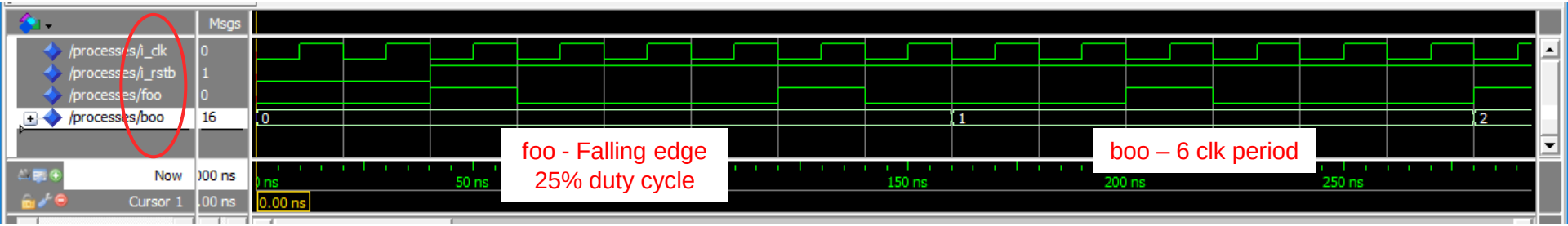
Provide the value for each signal shortly after the rising edge of the 1st and 2nd clk after reset is released. Assume rstb is released while clk is high.

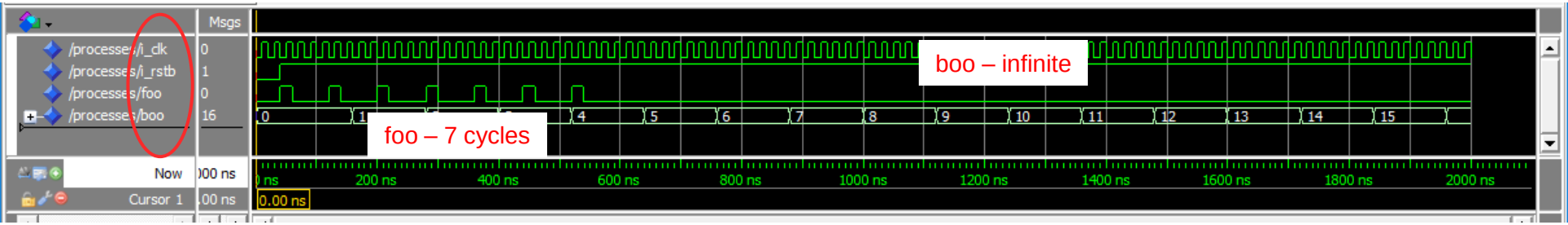
Signal	after CLK1 ↑	after CLK2 ↑
o_one	24	16
o_five	7	14

2) Provide a simulation for test processes below. Assume an existing clk process running with period PER and a resetb process that releases reset on the 2nd falling clock edge 30 pts

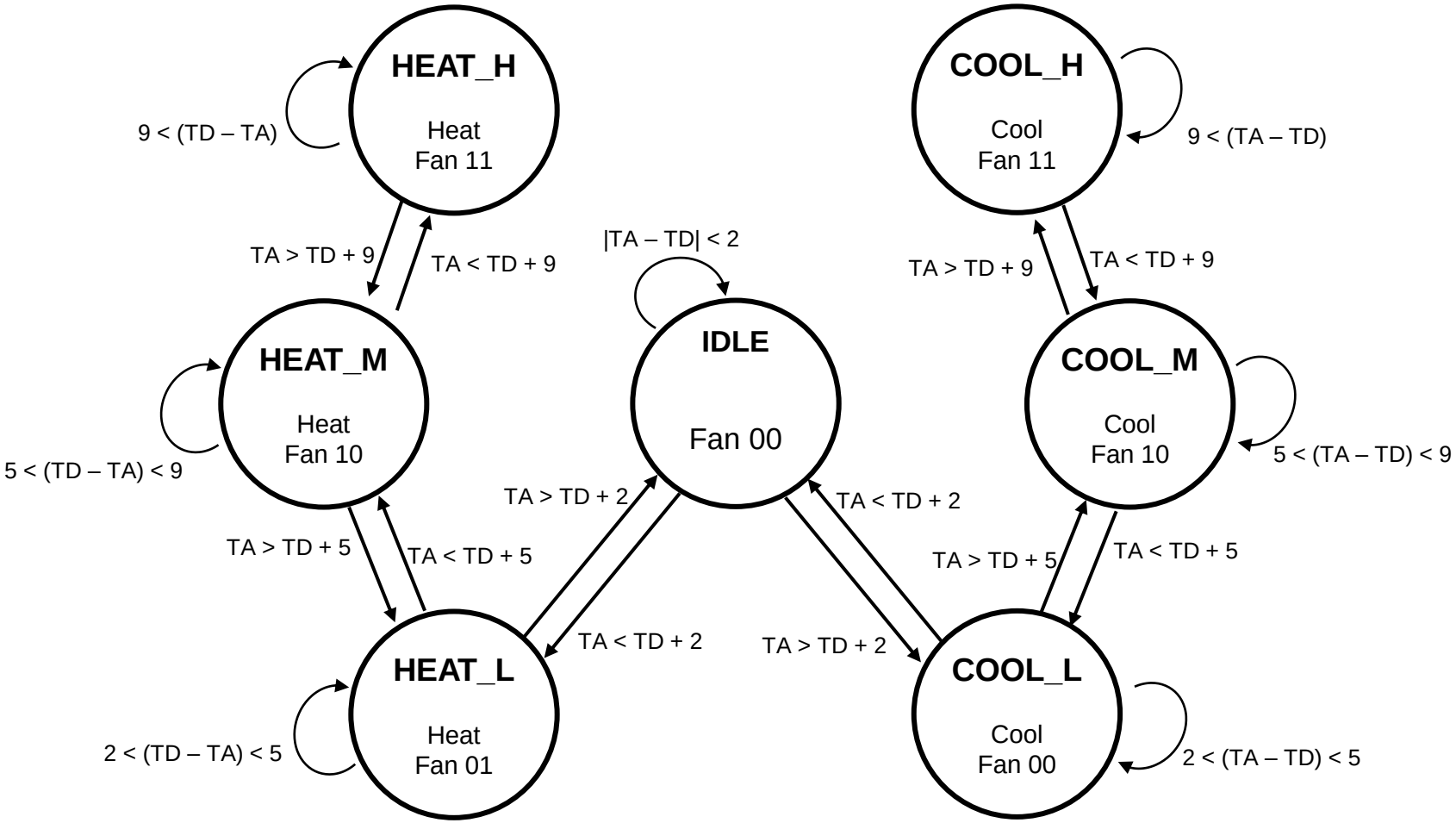
```
-- foo process
foo_proc: process
begin
   -- initialize value
   foo <= '0';

   -- wait for reset
   wait for 2*PER;

   -- already on falling clock edge

   -- create a 7 cycle loop
   for i in 1 to 7 loop
      foo <= '1';
      wait for 1*PER;
      foo <= '0';
      wait for 3*PER;
   end loop;

   -- cause it to stop
   wait;
end process;
```

```
boo_proc: process
begin
   -- initialize value
   boo <= (others => '0');

   -- wait for reset
   wait for 2*PER;

   -- no clock edge specified - use falling

   -- create infinite process
   loop
      wait for 6*PER;
      boo <= std_logic_vector(unsigned(boo) + 1);
   end loop;
end process;
```





3) Create a state transition diagram for a 3 speed heating/cooling (HVAC) system. Assume the desired temperature and actual temperatures are inputs, both heating and cooling is provided, the system is off if the two temperatures are within 2 degrees, runs at low if they are within 5 degrees, medium if they are within 9 degrees and high if they are greater than 9 degrees apart. The outputs are fan speed in binary(Off, Low, Med, High), heat and cool. 40 pts



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