EE 3921

Dr. Johnson

Homework 6

1 – FF Based memory: Modify the design from class (Max10 Memory HDL notes – page 6) to create a 128 word, 40 bit memory. Write down every line of code that must be modified. Compile your design and include the compilation report / flow summary with the number of LE's highlighted. 10pts

2A – How many onboard memory blocks would be required to support the same size memory as the previous problem? 10pts

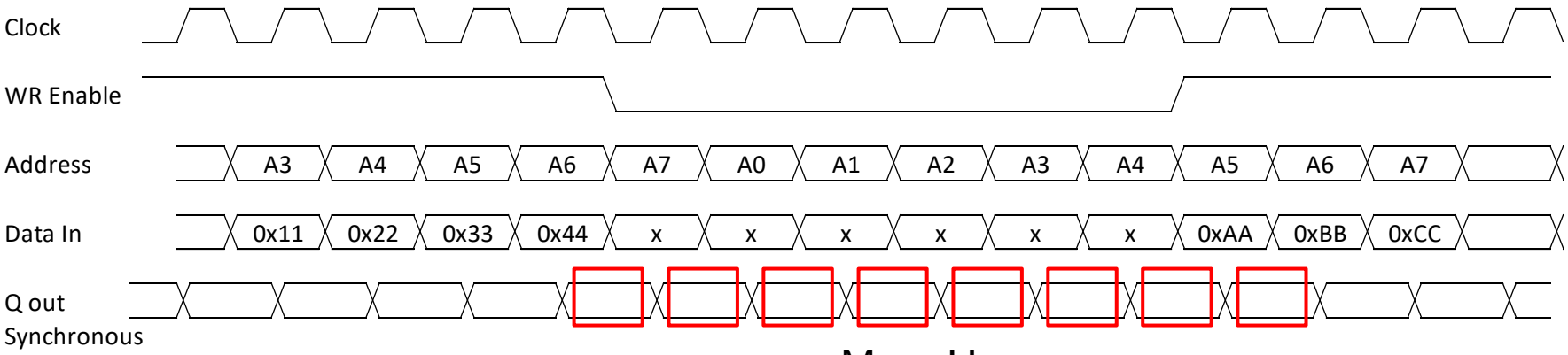
2B – What is the largest size 32bit word memory that can fit in a single on chip memory block? 10pts

3 – Implement a dual clock 8KB SRAM in by-32 configuration using the Mega Wizard 50pts

Compile your HDL and provide the code showing the address/data widths and clocks

Provide the compilation summary showing the number of memory bits used

4 – Simple single port memory: Given the timing diagram below for the simple single port memory, fill in the values for the empty boxes on the diagram and the final memory values. Assume a new data output model 20pts



	Mem Hex BEFORE	Mem Hex AFTER
A0	0x1A	
A1	0x1B	
A2	0x1C	
A3	0x1D	
A4	0x1E	
A5	0x1F	
A6	0x10	
A7	0x21	