EE 3921

Dr. Johnson

Homework 7

1 – a) Provide the generic parameters required for our VGA driver for a VESA 1600x1200 display with a 65Hz refresh rate (note: VESA in this case looks like VGA) 10pts

b) What would the required PLL output frequency be 5 pts

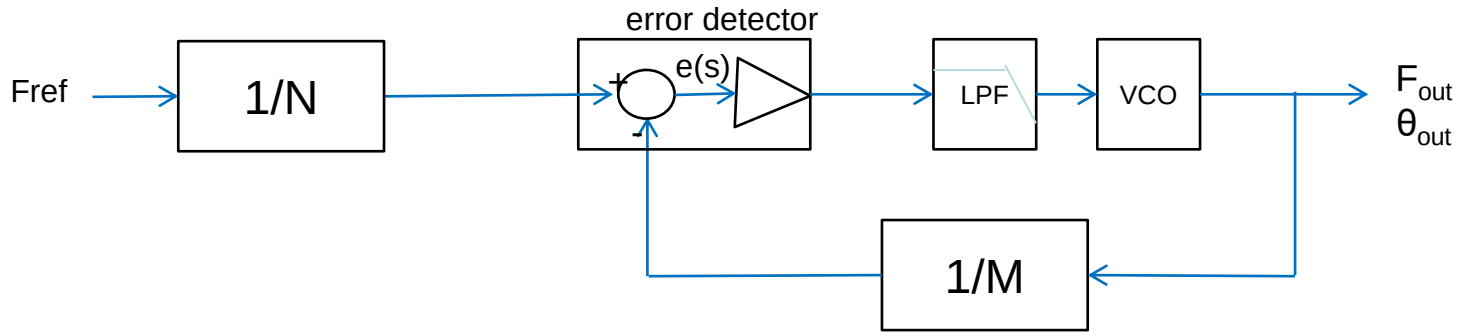
c) What would the required PLL M/N values be for this display (assume 50MHz clk) 5 pts

2 – Review the Max10 spec and provide the ranges for n and m in the PLLs. Calculate the greatest multiply possible, the greatest divide possible, and the closest frequency to the original clock that can be created (that is not the same as the original clock) Note – assume the C dividers =1 10pts

N:	
M:	

Biggest multiple	
Biggest Divide	
Closest value	

3 – Identify each block in the diagram below and provide a short description of its role in performing the PLL function 20pts



4 – Create a 7bit x 9bit multiplier using the Mega Wizard

a) Provide your module code 10 pts

b) Provide an RTL schematic 10 pts

c) Create a testbench that runs all input combinations (do not create an exhaustive list – use a loop or similar construct 20 pts

d) Provide simulation results for 4x20 and 127x259 10 pts