# MAX 10 Memory

Last updated 5/19/20

# MAX10 Memory

These slides review the implementation of memory on the MAX10 FPGA

Upon completion: You should be able to describe and evaluate the memory structures available on MAX10 FPGA


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# MAX10 Memory

- M9K Fixed Memory Blocks
  - Functional configurations
    - Single-port
    - Simple dual-port
    - True dual-port (bidirectional dual-port)
    - Shift register
    - ROM
    - FIFO buffers
    - Memory Based Multiplier


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# MAX10 Memory

- M9K Fixed Memory Blocks
  - Data width (word) configurations

| Feature | M9K Block |
|---|---|
| Configurations (depth × width) | 8192 × 1 |
| | 4096 × 2 |
| | 2048 × 4 |
| | 1024 × 8 |
| | 1024 × 9 |
| | 512 × 16 |
| | 512 × 18 |
| | 256 × 32 |
| | 256 × 36 |

Parity used as memory

  - Packed Mode
    - Single Port configuration
    - Each M9K block can be broken into 2 independent memories
    - Each memory must be less than ½ the full block size
    - 18 bit word size maximum ??
    - Each memory has only single clock support


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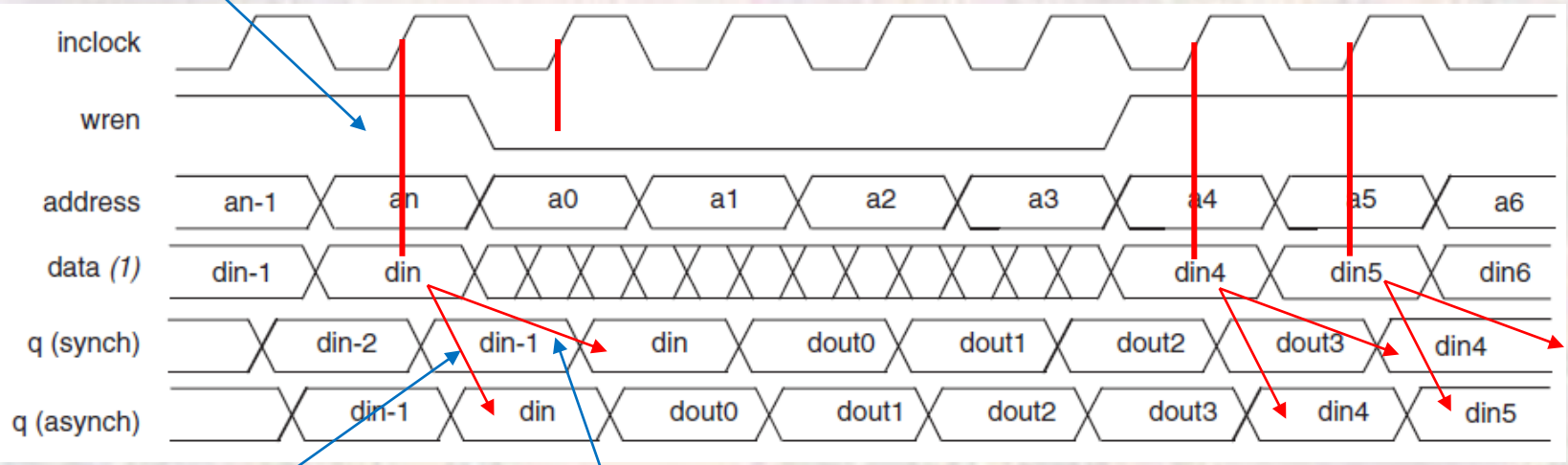
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Single Port RAM - write

Write addr captured




Src: Cyclone II Device Handbook

Async data flow through with delay

Sync data flow through with 1 clk + td delay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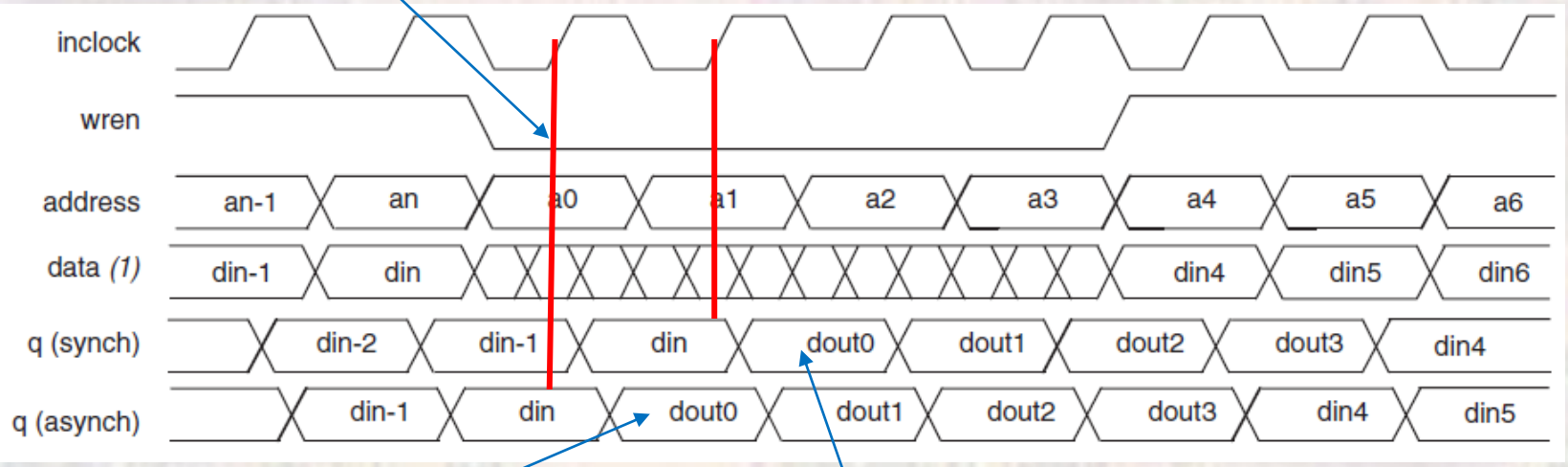
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Single Port RAM - read

Read addr captured




Src: Cyclone II Device Handbook

Async read
with delay

Sync data read
with 1 clk + td delay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# MAX10 Memory

- M9K Fixed Memory Blocks
  - Byte Enable
    - SRAM only
    - Multi-byte words can be masked

**Table 2-1: M9K Blocks Byte Enable Selections**

| byteena[3:0] | Affected Bytes. Any Combination of Byte Enables is Possible. | | | |
|---|---|---|---|---|
| | datain x 16 | datain x 18 | datain x 32 | datain x 36 |
| [0] = 1 | [7:0] | [8:0] | [7:0] | [8:0] |
| [1] = 1 | [15:8] | [17:9] | [15:8] | [17:9] |
| [2] = 1 | — | — | [23:16] | [26:18] |
| [3] = 1 | — | — | [31:24] | [35:27] |

Src: MAX 10 Device Handbook


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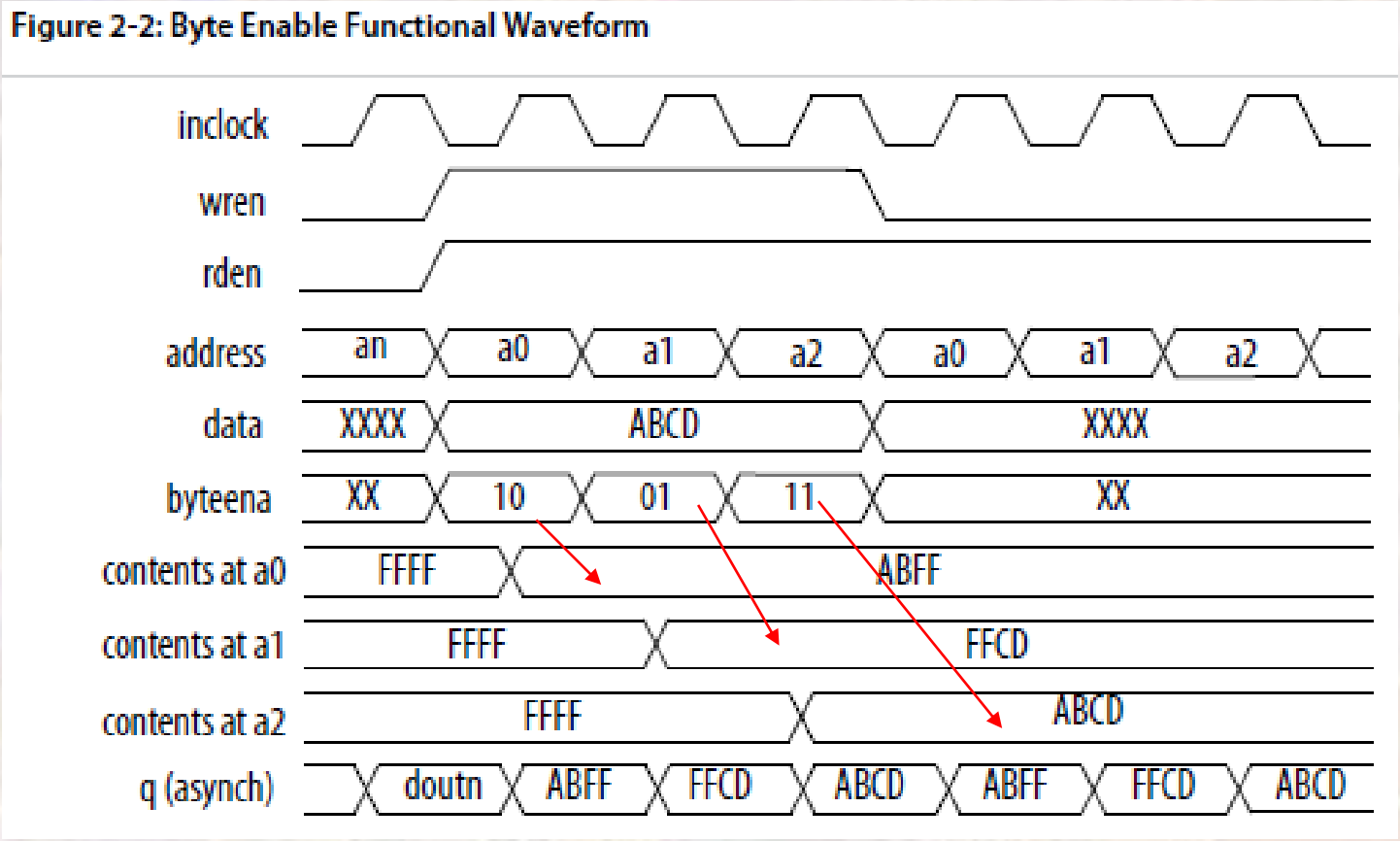
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Byte Enable – 16b example

**Figure 2-2: Byte Enable Functional Waveform**




Src: MAX 10 Device Handbook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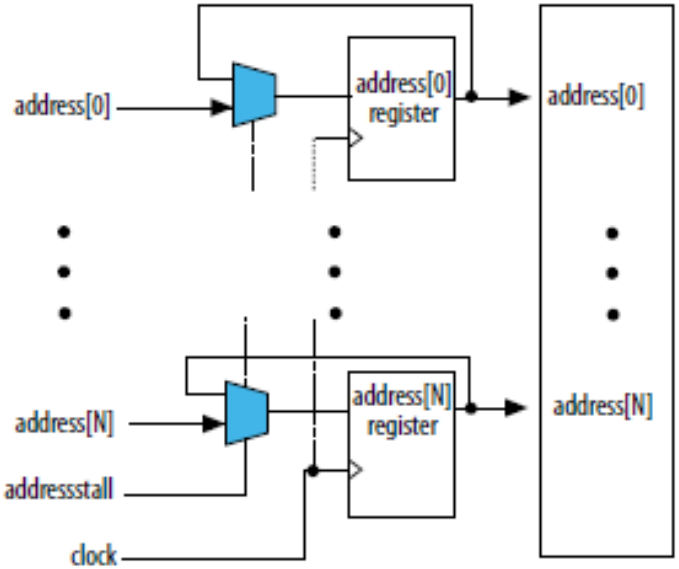
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Address Clock Enable
    - Holds the previous address input until enabled
    - Clock gate
    - Implemented as a Stall

**Figure 2-3: Address Clock Enable Block Diagram**




Src: MAX 10 Device Handbook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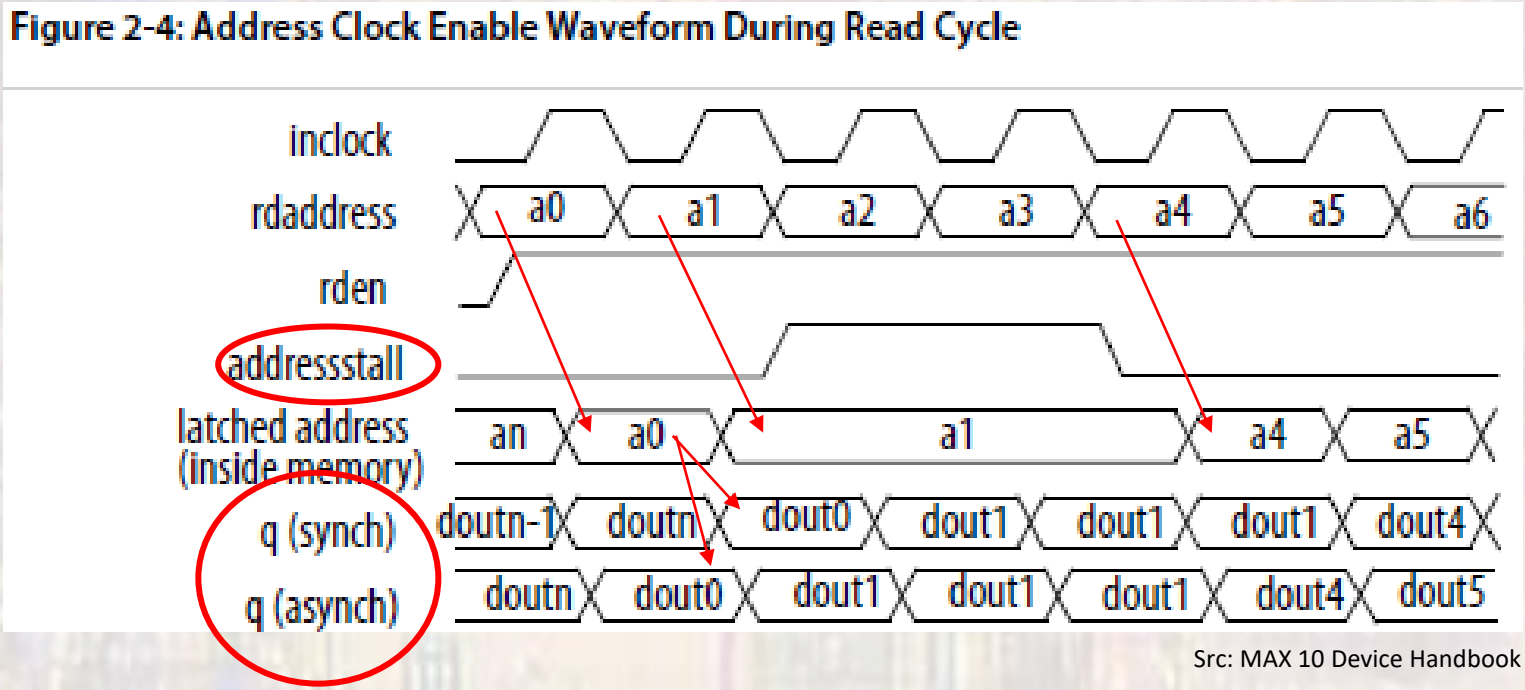
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Address Clock Enable - read

**Figure 2-4: Address Clock Enable Waveform During Read Cycle**




Src: MAX 10 Device Handbook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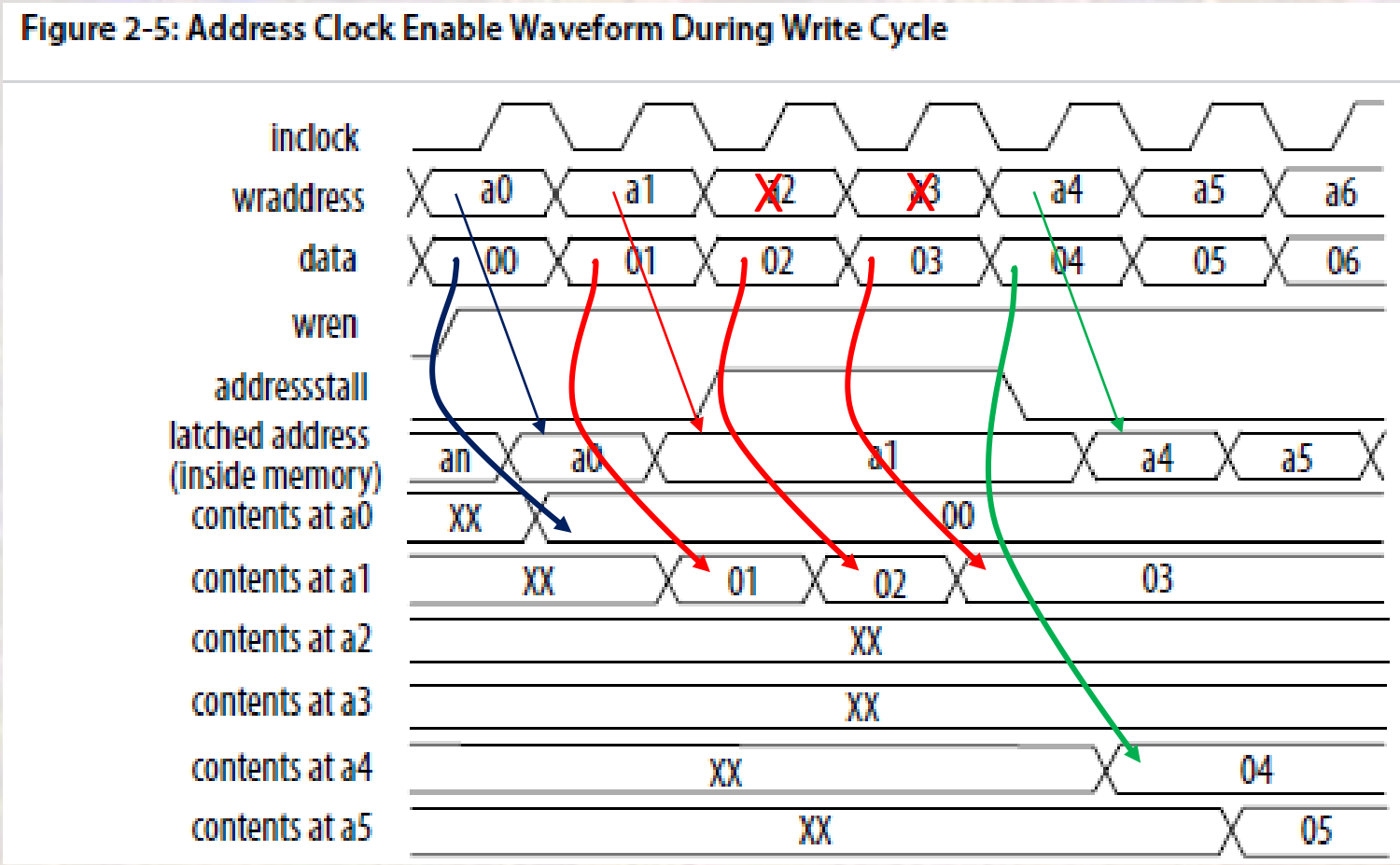
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Address Clock Enable - write

**Figure 2-5: Address Clock Enable Waveform During Write Cycle**




Src: MAX 10 Device Handbook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# MAX10 Memory

- M9K Fixed Memory Blocks
  - Clock Modes

| Clock Mode | Description | Modes | | | | |
|---|---|---|---|---|---|---|
| | | True Dual-Port | Simple Dual-Port | Single-Port | ROM | FIFO |
| Independent Clock Mode | A separate clock is available for the following ports:<br>• Port A—Clock A controls all registers on the port A side.<br>• Port B—Clock B controls all registers on the port B side. | Yes | — | — | Yes | — |
| Input/Output Clock Mode | • M9K memory blocks can implement input or output clock mode for single-port, true dual-port, and simple dual-port memory modes.<br>• An input clock controls all input registers to the memory block, including `data`, `address`, `byteena`, `wren`, and `rden` registers.<br>• An output clock controls the data-output registers. | Yes | Yes | Yes | Yes | — |
| Read or Write Clock Mode | • M9K memory blocks support independent clock enables for both the read and write clocks.<br>• A read clock controls the data outputs, read address, and read enable registers.<br>• A write clock controls the data inputs, write address, and write enable registers. | — | Yes | — | — | Yes |
| Single-Clock Mode | A single clock, together with a clock enable, controls all registers of the memory block. | Yes | Yes | Yes | Yes | Yes |

Src: MAX 10 Device Handbook


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# MAX10 Memory

- M9K Fixed Memory Blocks
  - Additional Control Signals
    - Clock Enable
      - Enables the clock
      - If no clock is enabled – no memory activity
    - Asynchronous Clear
      - Clears the output data register if present
      - No clear for the input data register
    - Read/Write
      - Several variations depending on mode


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# MAX10 Memory

- M9K Fixed Memory Blocks
  - Data flow-through model
    - All inputs are registered
    - Outputs can be synchronous or asynchronous
    - 2 flow through options
  - Read-during-write – new data
    - Single port, true Dual Port
    - Write data flows through to the output
  - Read-during-write – old data
    - Single port, true Dual Port
    - Old data is provided to the output


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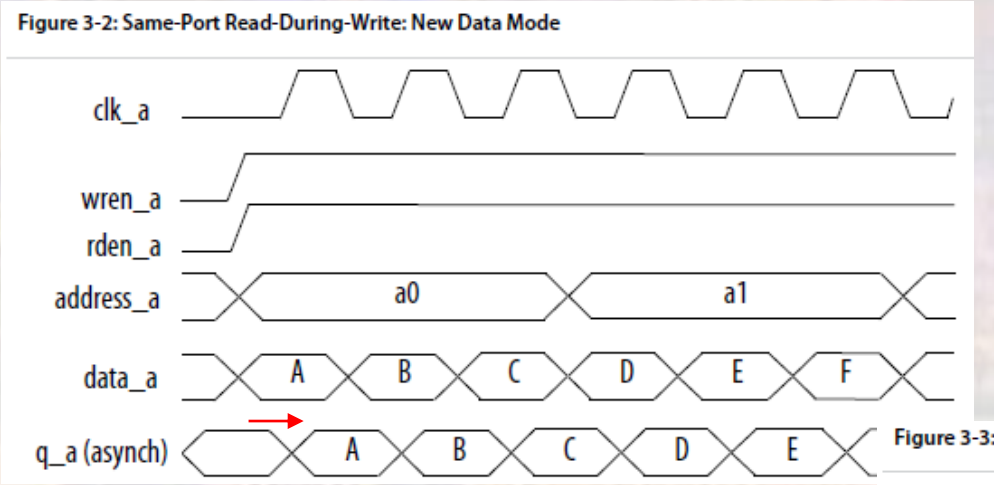
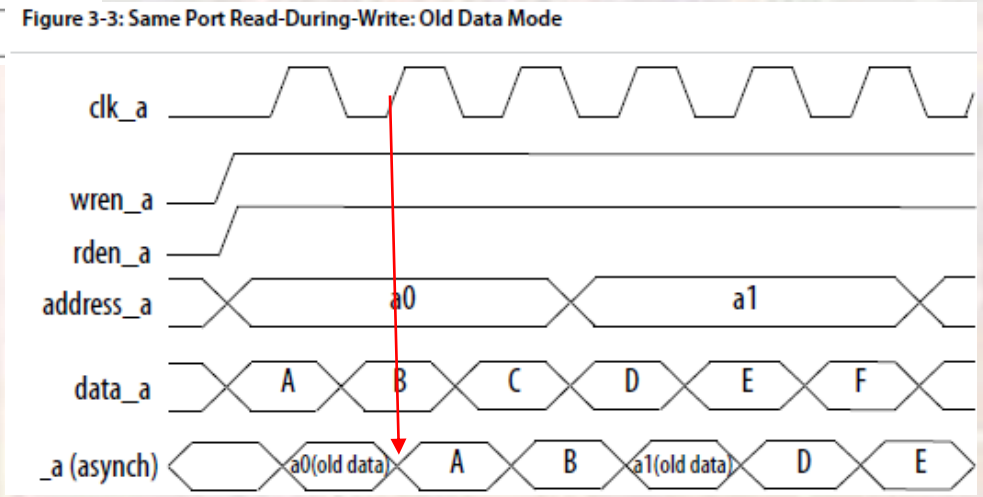
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Read during Write




Write complete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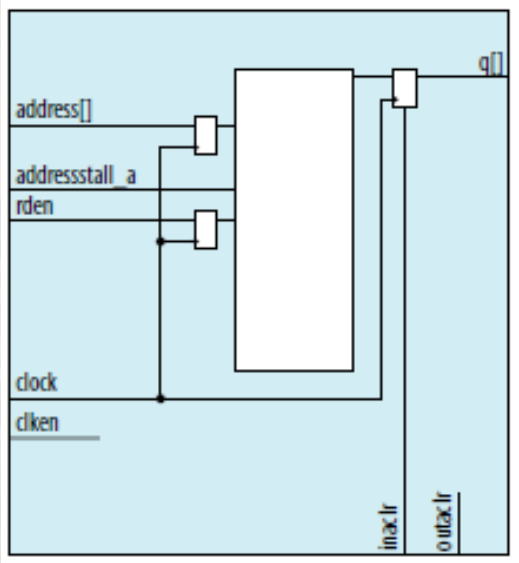
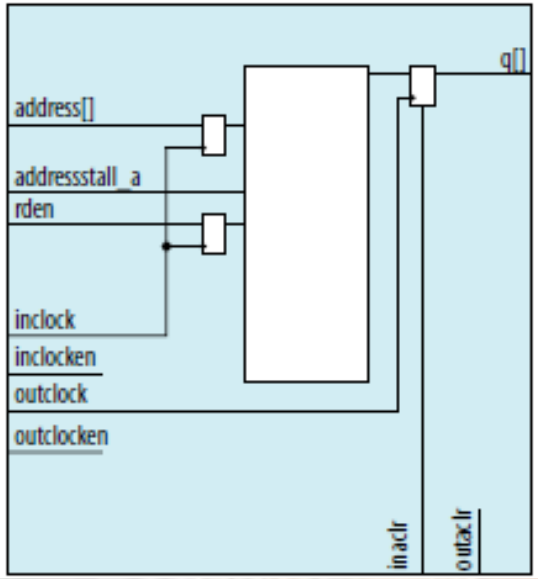
# MAX10 Memory

- M9K Fixed Memory Blocks
  - ROM – Single Port
    - SRAM with memory pre-loaded from a MIF file
    - Single Port
    - Read only

Single Clock




In/Out Clock

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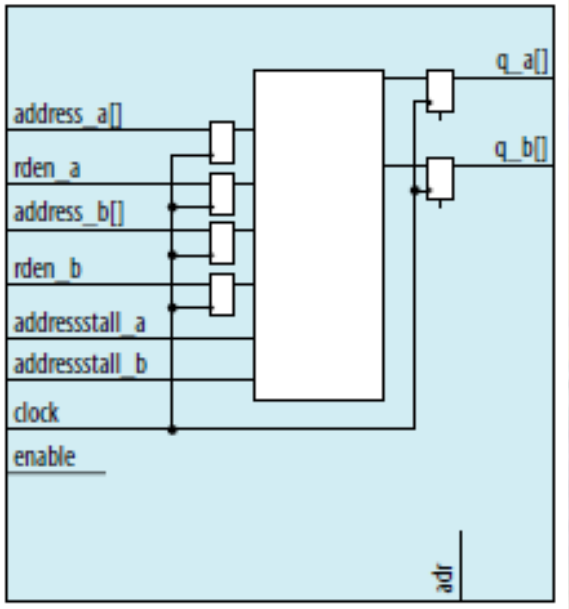
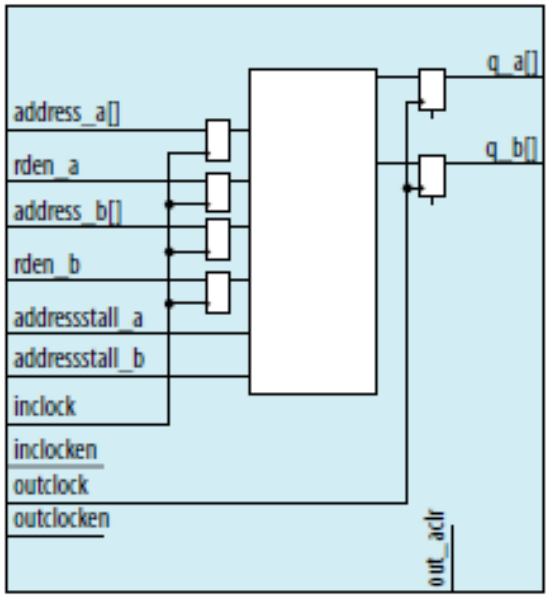
# MAX10 Memory

- M9K Fixed Memory Blocks
  - ROM – Dual Port
    - SRAM with memory pre-loaded from a MIF file
    - Dual Port
    - Read only

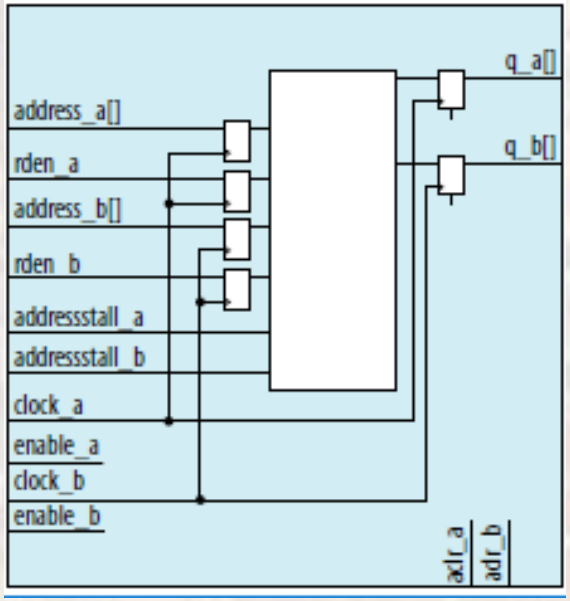
Single Clock




In/Out Clock




A/B Clock





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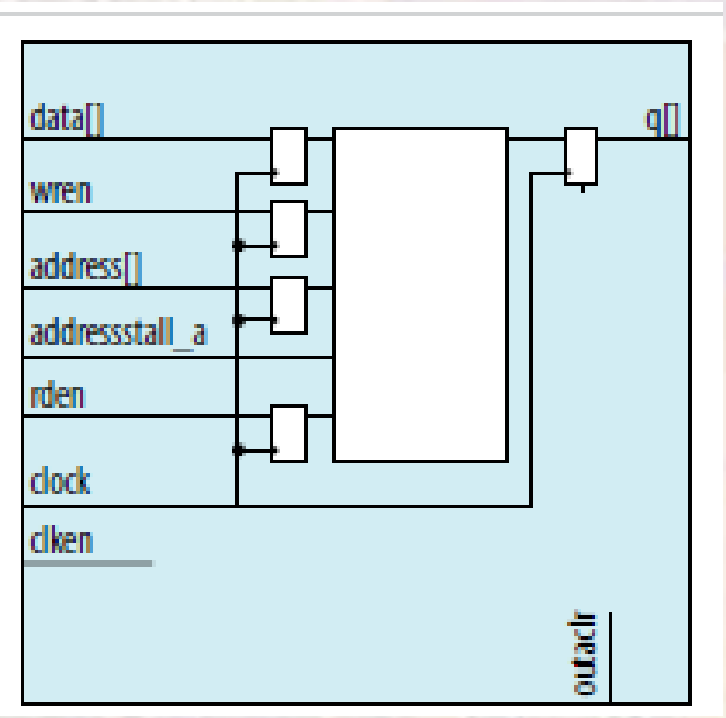
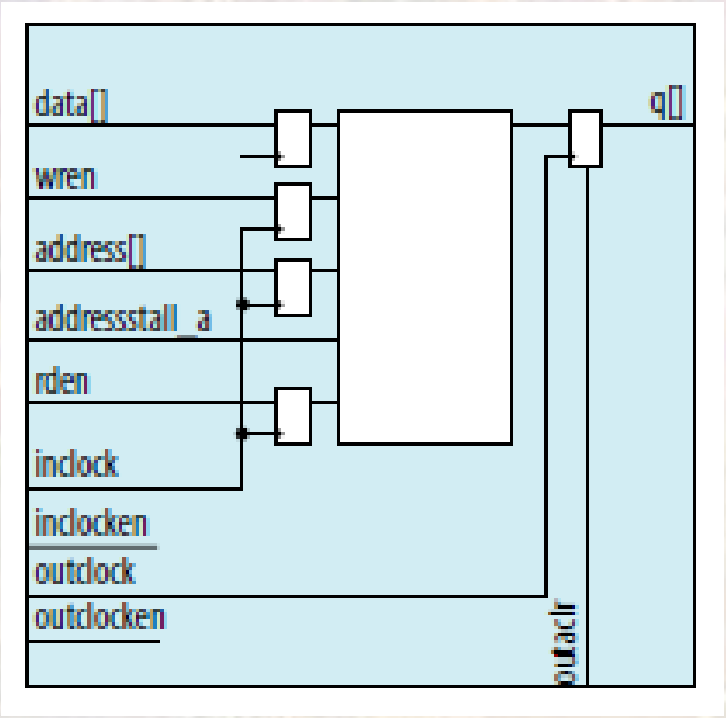
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Single Port RAM

Single Clock




Dual Clock




Src: MAX 10 Device Handbook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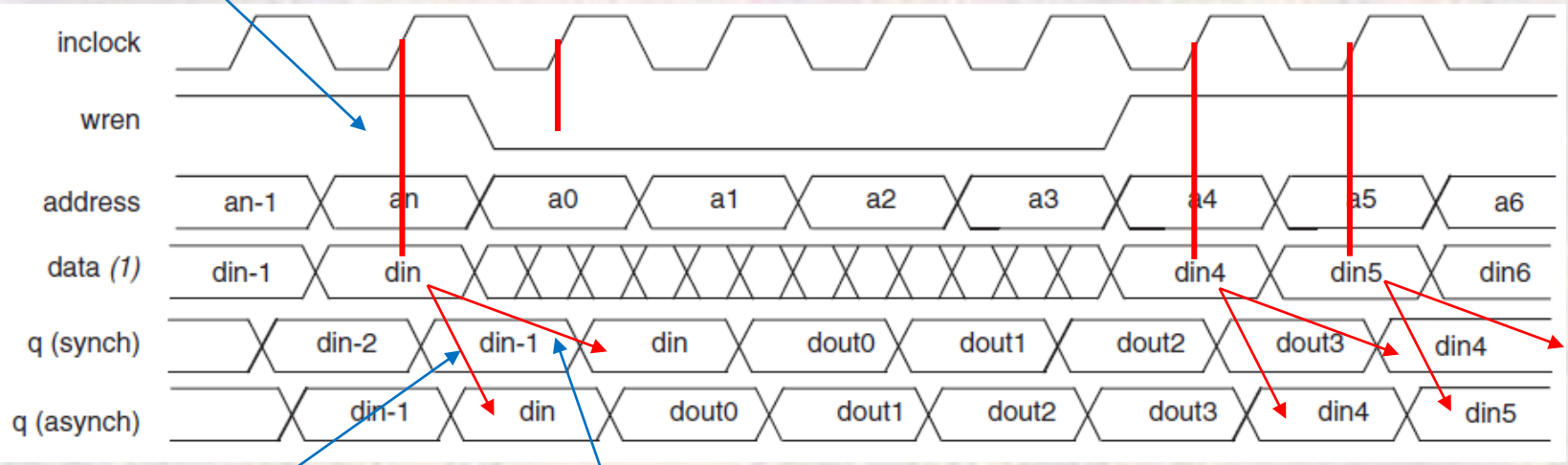
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Single Port RAM - write

Write addr captured




Src: Cyclone II Device Handbook

Async data flow through with delay

Sync data flow through with 1 clk + td delay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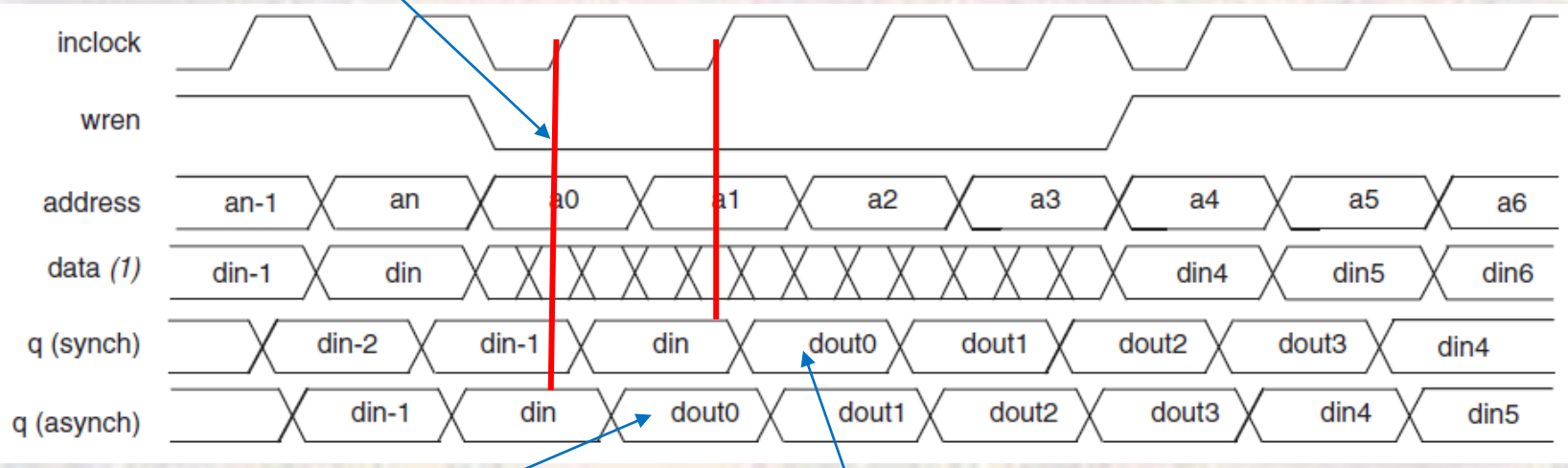
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Single Port RAM - read

Read addr captured




Src: Cyclone II Device Handbook

Async read
with delay

Sync data read
with 1 clk + td delay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# MAX10 Memory

- M9K Fixed Memory Blocks
  - Simple Dual Port RAM
    - Separate read and write addresses
    - Simultaneous read and write
    - Data in and out ports do not have to have matching widths


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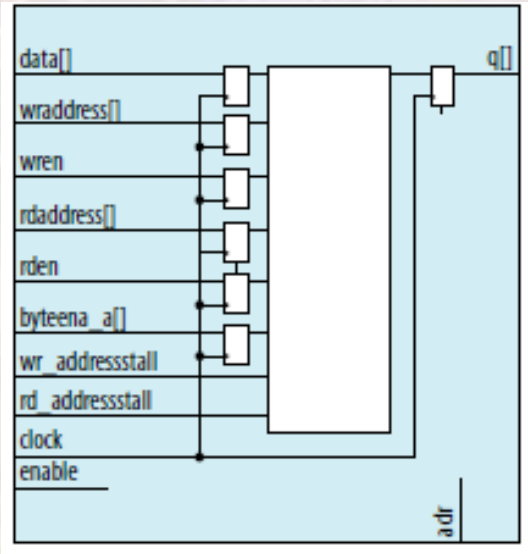
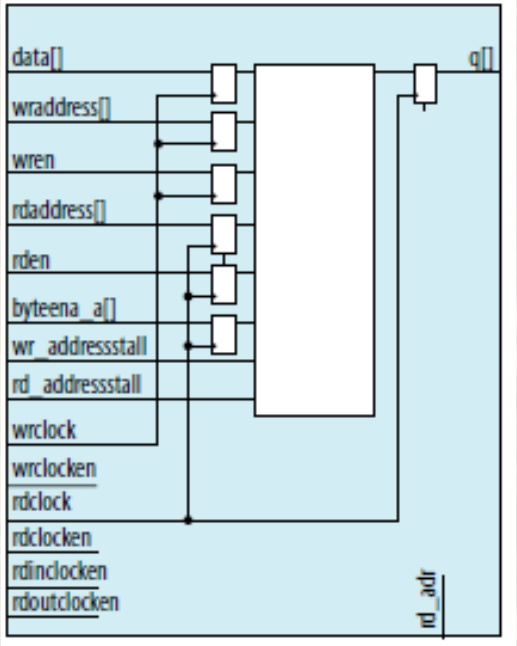
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Simple Dual Port RAM

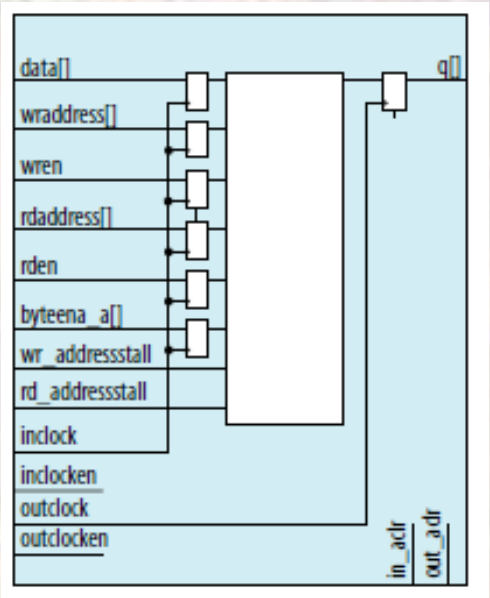
Single Clock




R/W Clock




In/Out Clock

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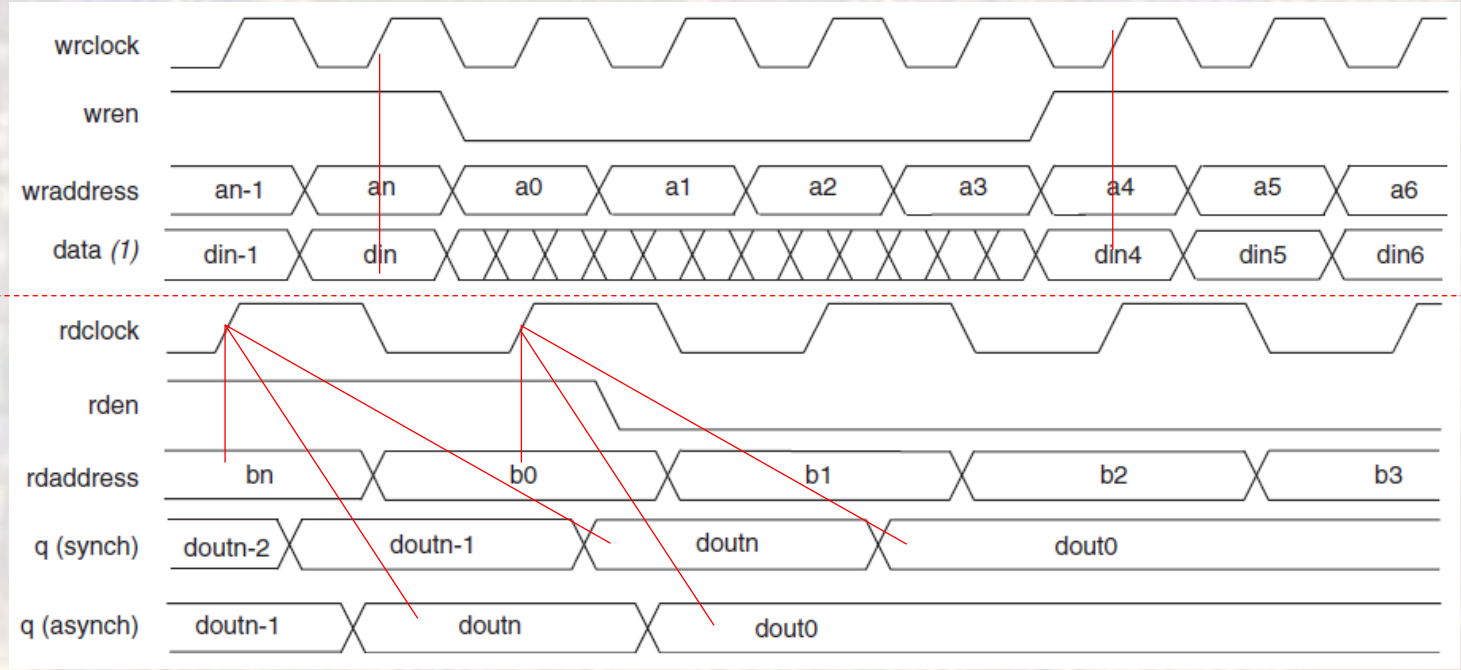
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Simple Dual Port RAM




Src: Cyclone II Device Handbook

# MAX10 Memory

- M9K Fixed Memory Blocks
  - True Dual Port RAM
    - Supports 2 reads, 2 writes, Read/Write
    - Multiple clock options
    - Data in and out ports do not have to have matching widths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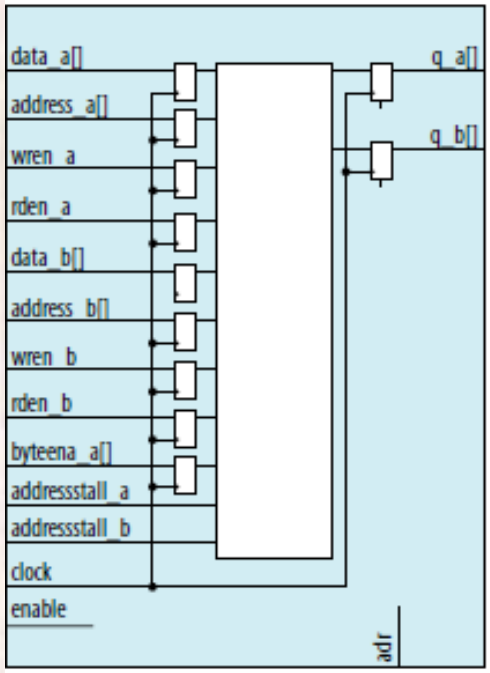
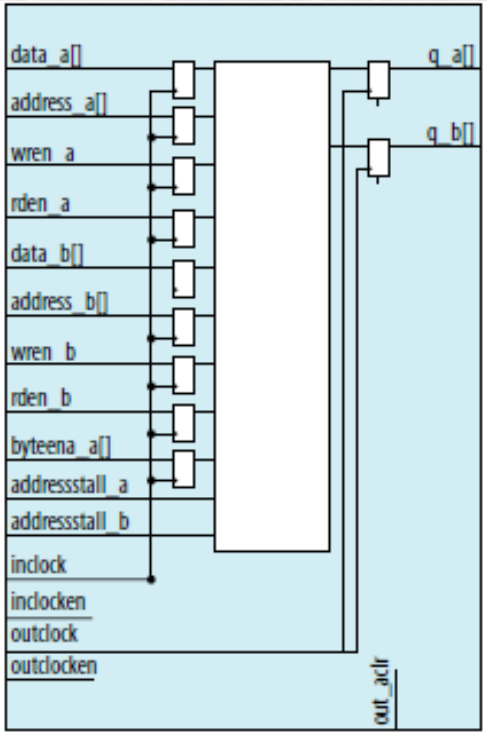
# MAX10 Memory

- M9K Fixed Memory Blocks
  - True Dual Port RAM
  - Multiple R/W Ports

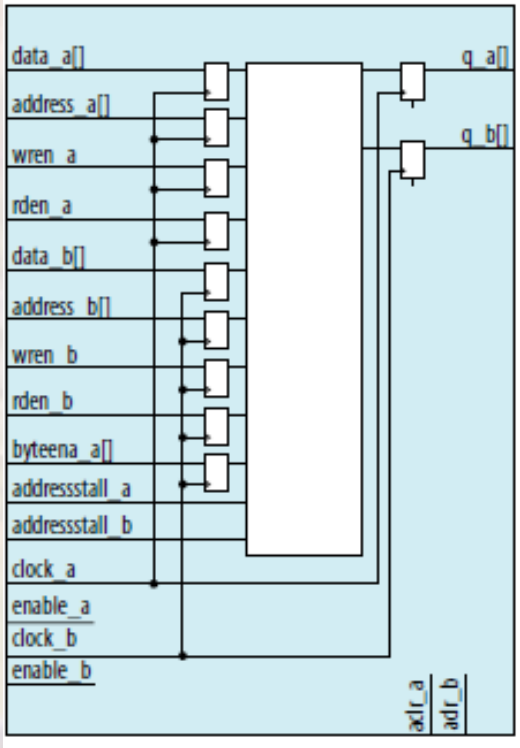
Single Clock




R/W Clock




A/B Clock





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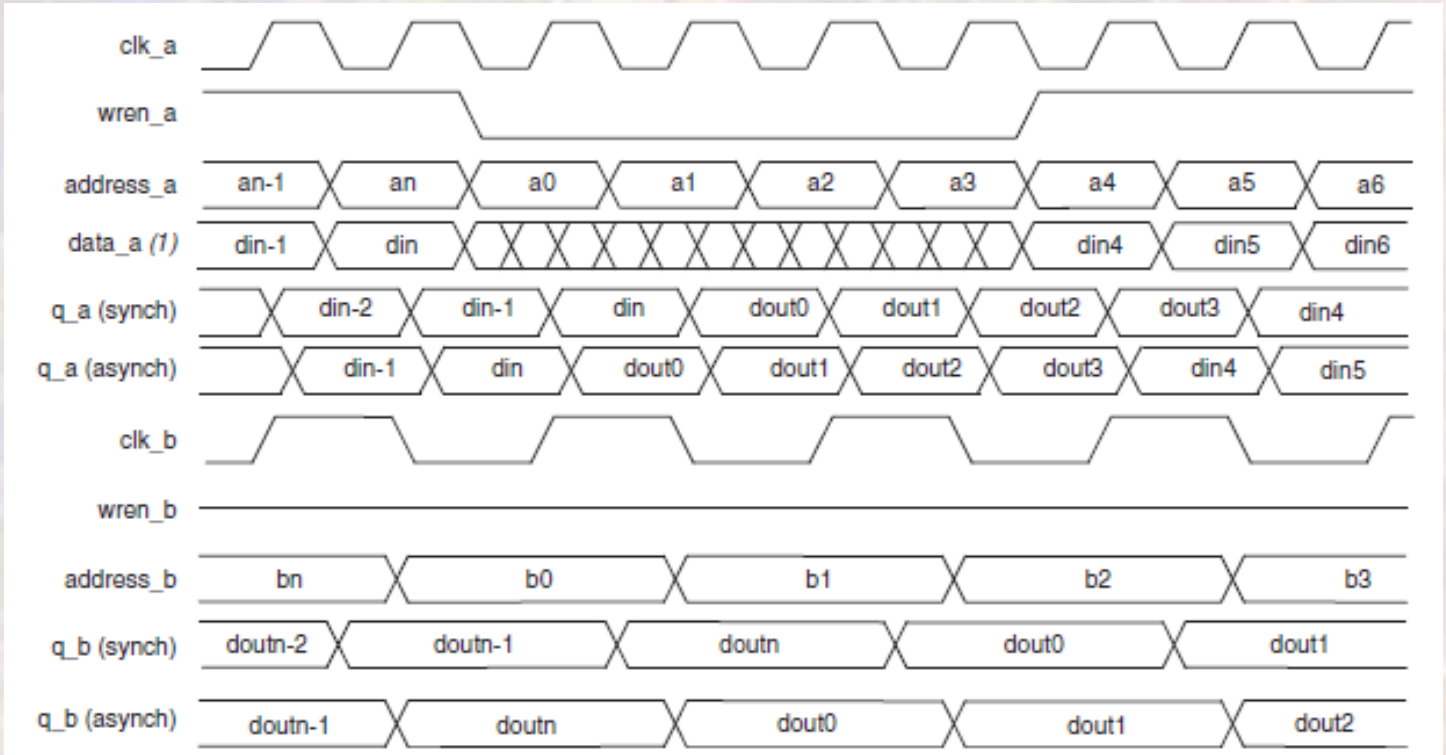
# MAX10 Memory

- M9K Fixed Memory Blocks
  - True Dual Port RAM




Src: Cyclone II Device Handbook

# MAX10 Memory

- M9K Fixed Memory Blocks
  - Mixed Port Configurations

**M9K Block Mixed-Width Configurations (Simple Dual-Port RAM)**

| Read Port | Write Port | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 8192 × 1 | 4096 × 2 | 2048 × 4 | 1024 × 8 | 512 × 16 | 256 × 32 | 1024 × 9 | 512 × 18 | 256 × 36 |
| 8192 × 1 | Yes | Yes | Yes | Yes | Yes | Yes | — | — | — |
| 4096 × 2 | Yes | Yes | Yes | Yes | Yes | Yes | — | — | — |
| 2048 × 4 | Yes | Yes | Yes | Yes | Yes | Yes | — | — | — |
| 1024 × 8 | Yes | Yes | Yes | Yes | Yes | Yes | — | — | — |
| 512 × 16 | Yes | Yes | Yes | Yes | Yes | Yes | — | — | — |
| 256 × 32 | Yes | Yes | Yes | Yes | Yes | Yes | — | — | — |
| 1024 × 9 | — | — | — | — | — | — | Yes | Yes | Yes |
| 512 × 18 | — | — | — | — | — | — | Yes | Yes | Yes |
| 256 × 36 | — | — | — | — | — | — | Yes | Yes | Yes |

**M9K Block Mixed-Width Configurations (True Dual-Port RAM Mode)**

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 8192 × 1 | 4096 × 2 | 2048 × 4 | 1024 × 8 | 512 × 16 | 1024 × 9 | 512 × 18 |
| 8192 × 1 | Yes | Yes | Yes | Yes | Yes | — | — |
| 4096 × 2 | Yes | Yes | Yes | Yes | Yes | — | — |
| 2048 × 4 | Yes | Yes | Yes | Yes | Yes | — | — |
| 1024 × 8 | Yes | Yes | Yes | Yes | Yes | — | — |
| 512 × 16 | Yes | Yes | Yes | Yes | Yes | — | — |
| 1024 × 9 | — | — | — | — | — | Yes | Yes |
| 512 × 18 | — | — | — | — | — | Yes | Yes |


Src: MAX 10 Device Handbook
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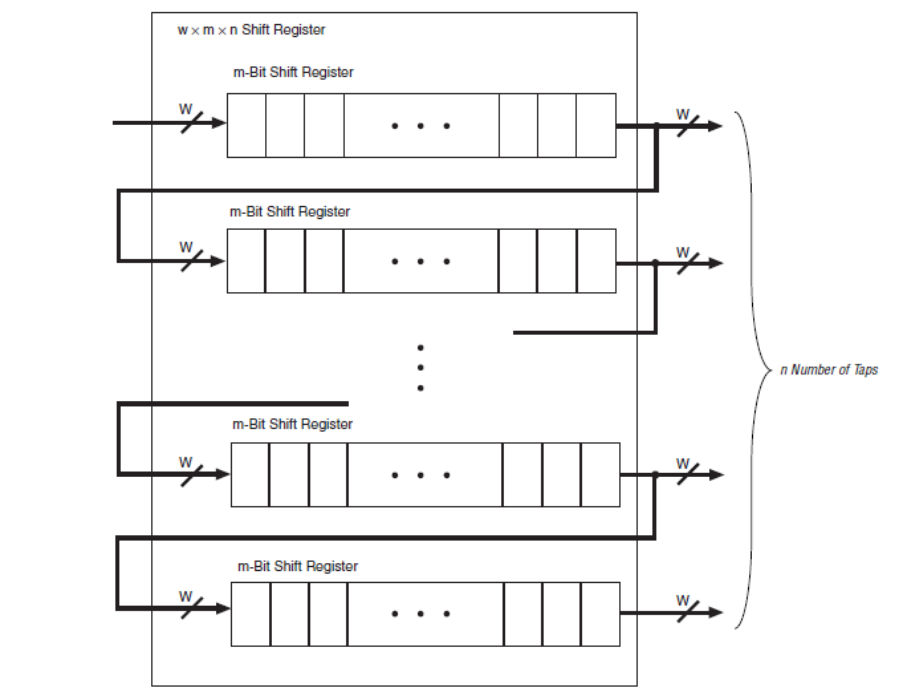
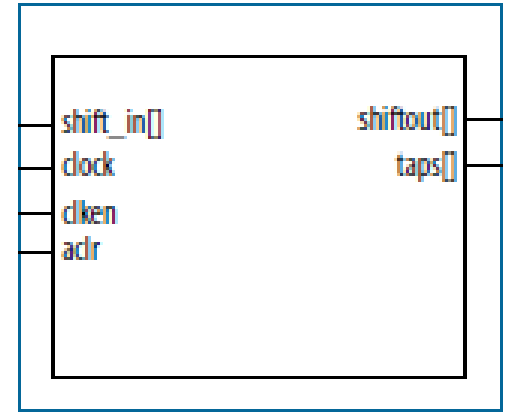
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Multi-tap Shift RAM
    - Multiple M9K blocks can be cascaded

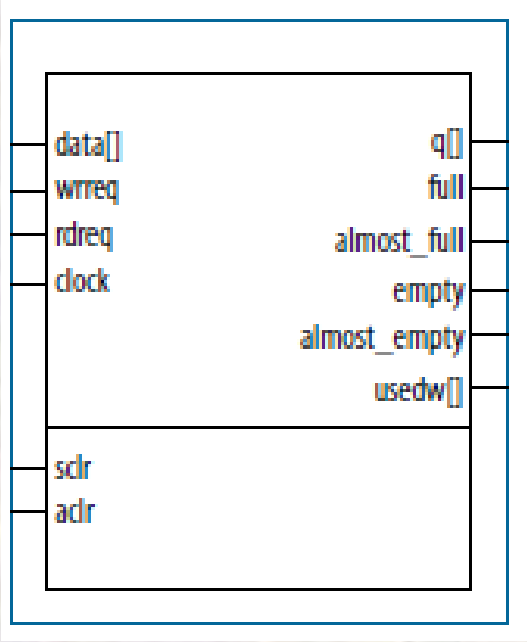


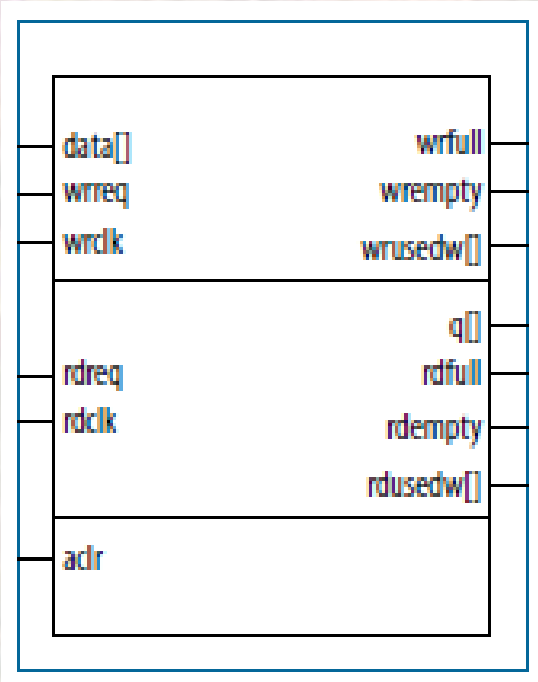




Src: Cyclone II Device Handbook

# MAX10 Memory

- M9K Fixed Memory Blocks
  - FIFO
    - Separate read and write clocks available
    - Separate read and write data widths available
    - Empty and Full signals

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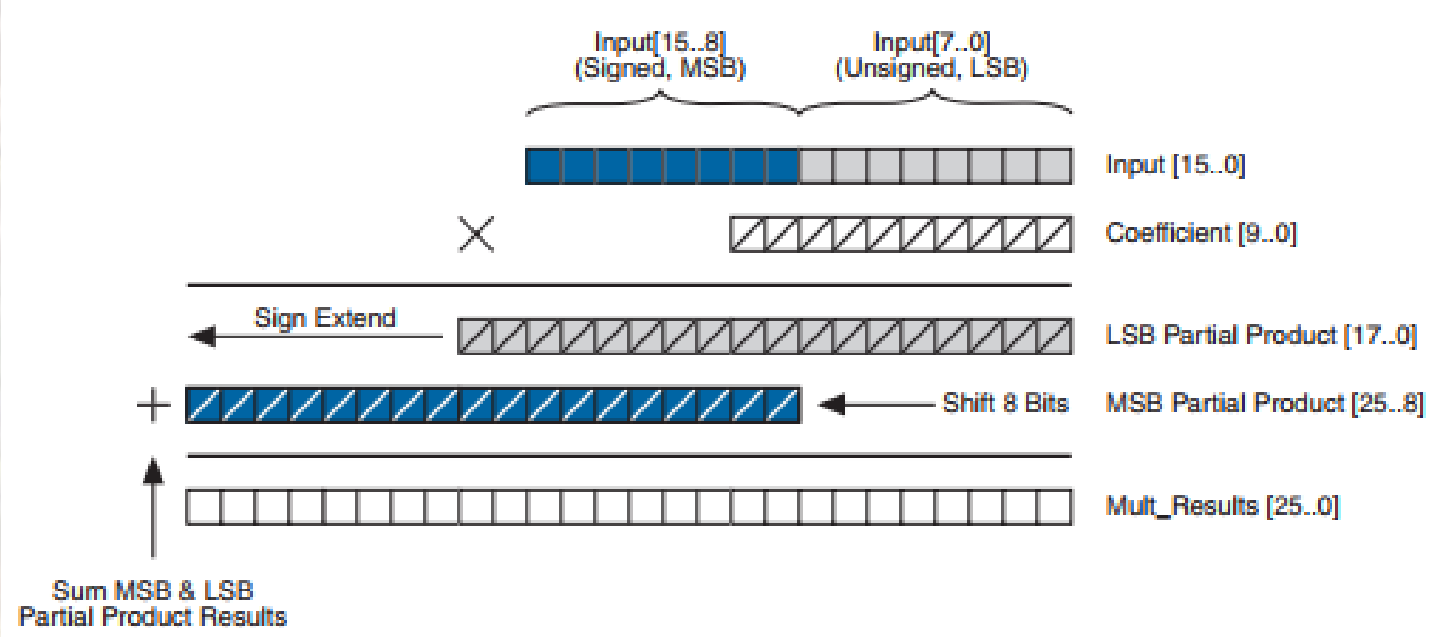
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Memory Based Multiplier

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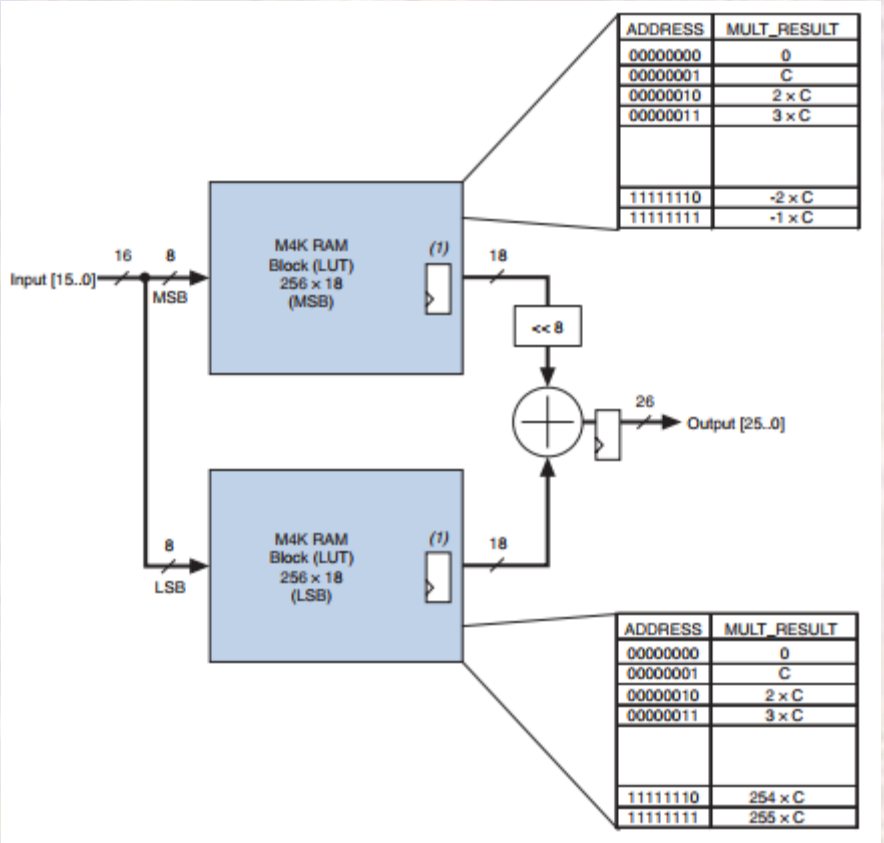
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Memory Based Multiplier

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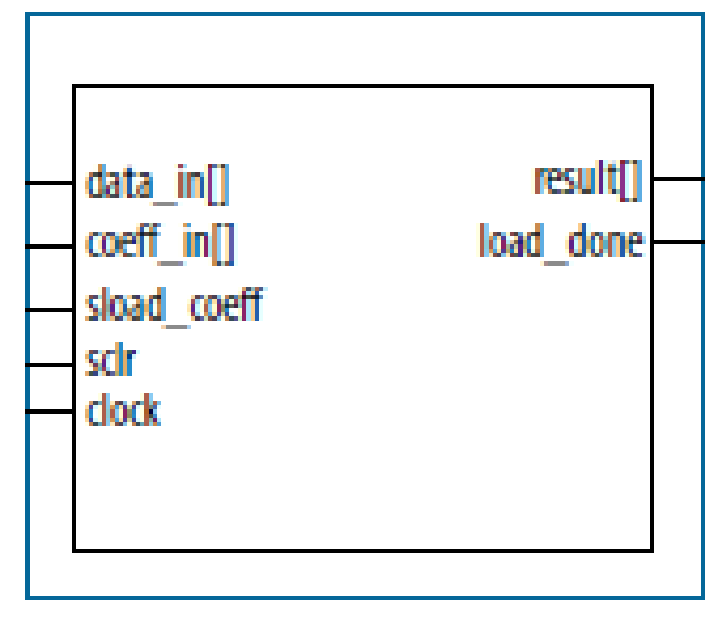
# MAX10 Memory

- M9K Fixed Memory Blocks
  - Memory Based Multiplier

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# MAX10 Memory

- User Flash Memory
  - Nonvolatile

| Features | Capacity |
|---|---|
| Endurance | Read and write counts up to 10,000 cycles |
| Data retention | • 20 years at 85 °C<br>• 10 years at 100 °C |
| Maximum operating frequency | • Serial interface: 7.25 MHz<br>• Parallel interface: 116 MHz |
| Data length | Stores data of up to 32-bit length |

| Device | Pages per Sector | | | | | Page Size (Kb) | Total User Flash Memory Size (Kb) | Total Configuration Memory Size (Kb) |
|---|---|---|---|---|---|---|---|---|
| | UFM1 | UFM0 | CFM2 | CFM1 | CFM0 | | | |
| 10M50 | 4 | 4 | 48 | 36 | 84 | 64 | 5888 | 10752 |

available for User Flash in some configurations


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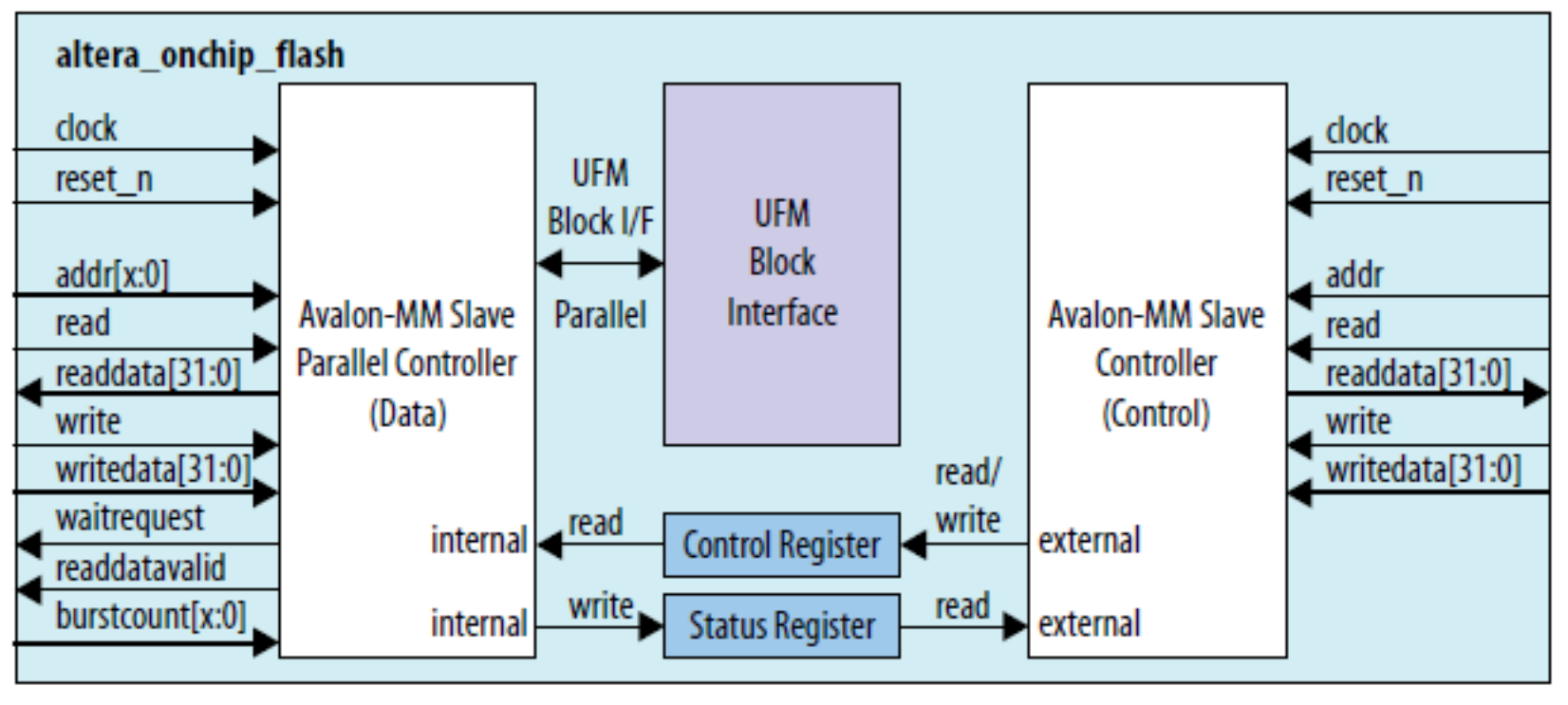
# MAX10 Memory

- User Flash Memory
  - Parallel Mode Operation

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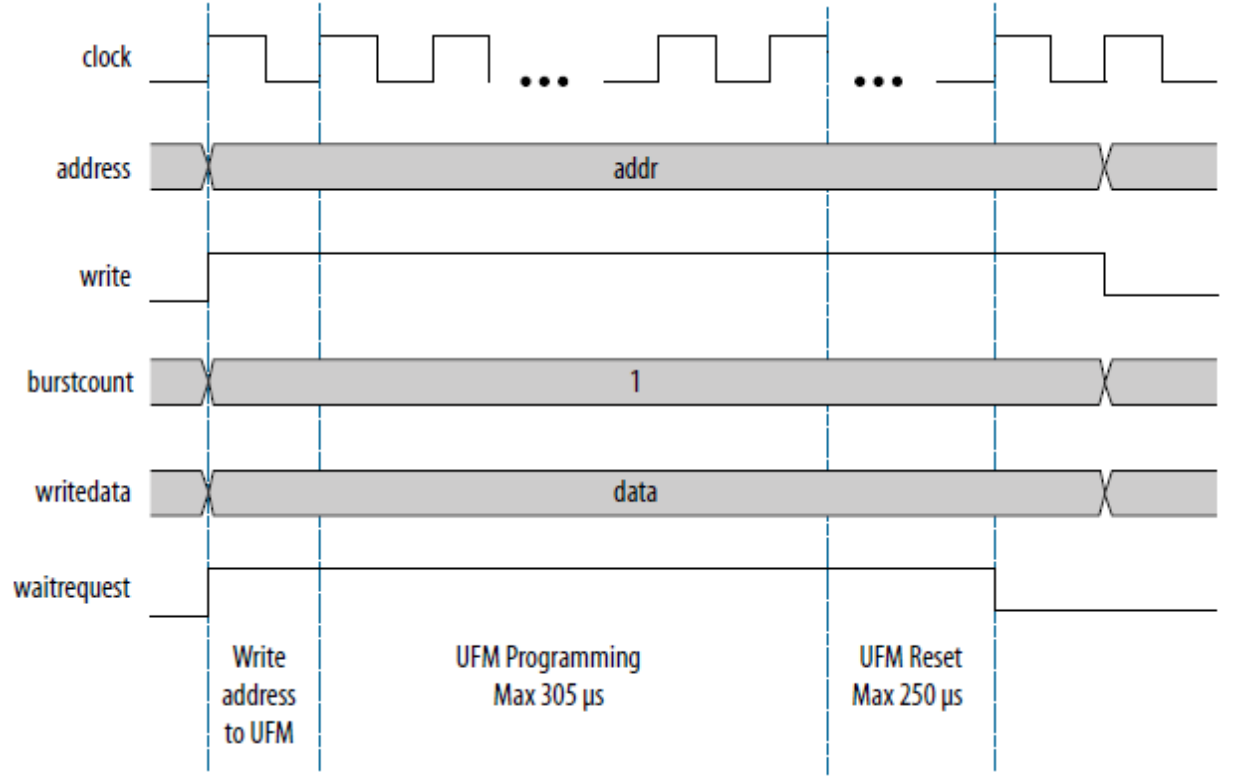
# MAX10 Memory

- User Flash Memory
  - Parallel Mode Operation - WRITE

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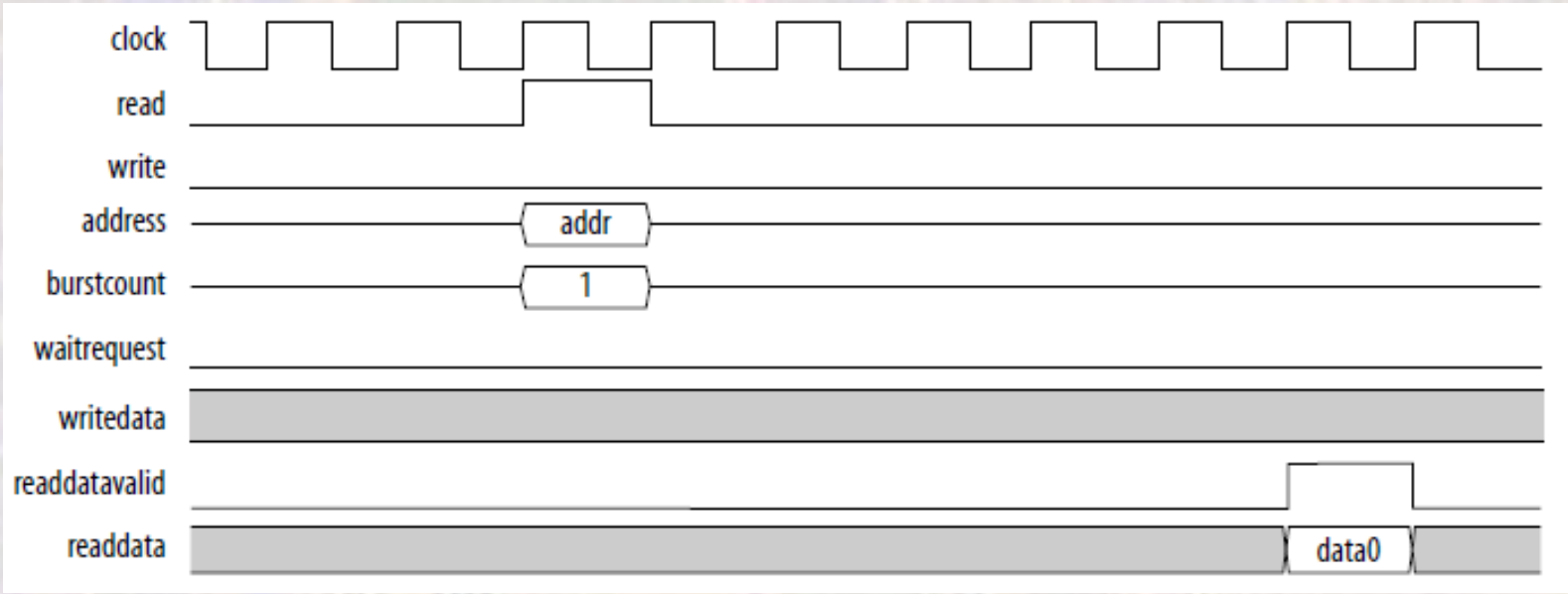
# MAX10 Memory

- User Flash Memory
  - Parallel Mode Operation - READ

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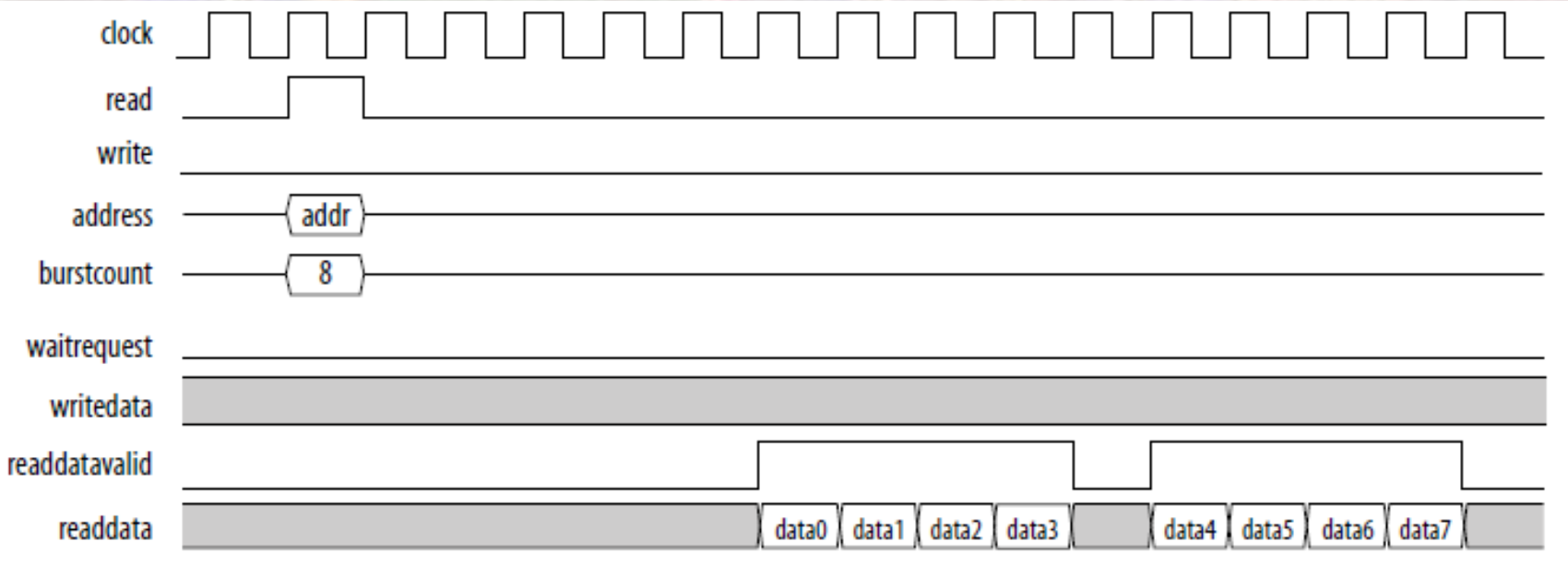
# MAX10 Memory

- User Flash Memory
  - Parallel Mode Operation – BURST READ

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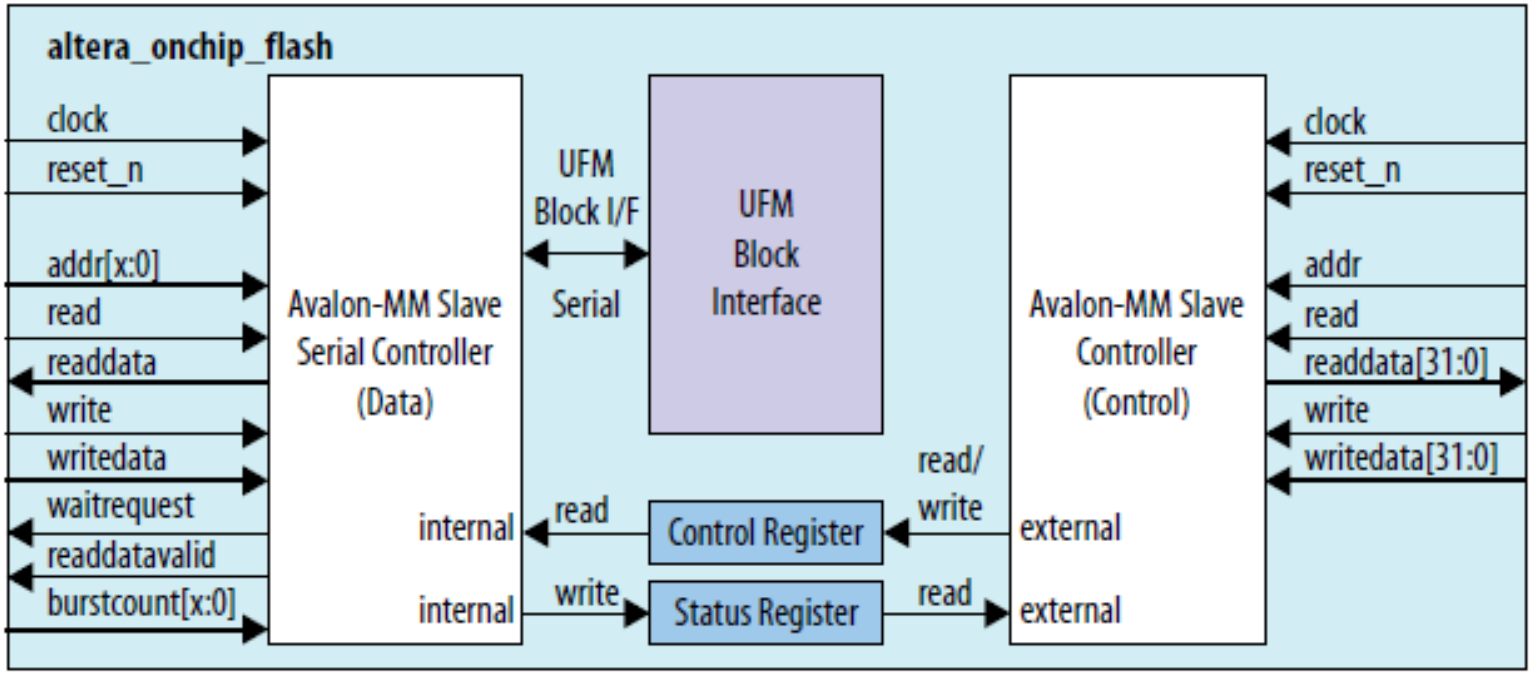
# MAX10 Memory

- User Flash Memory
  - Serial Mode Operation

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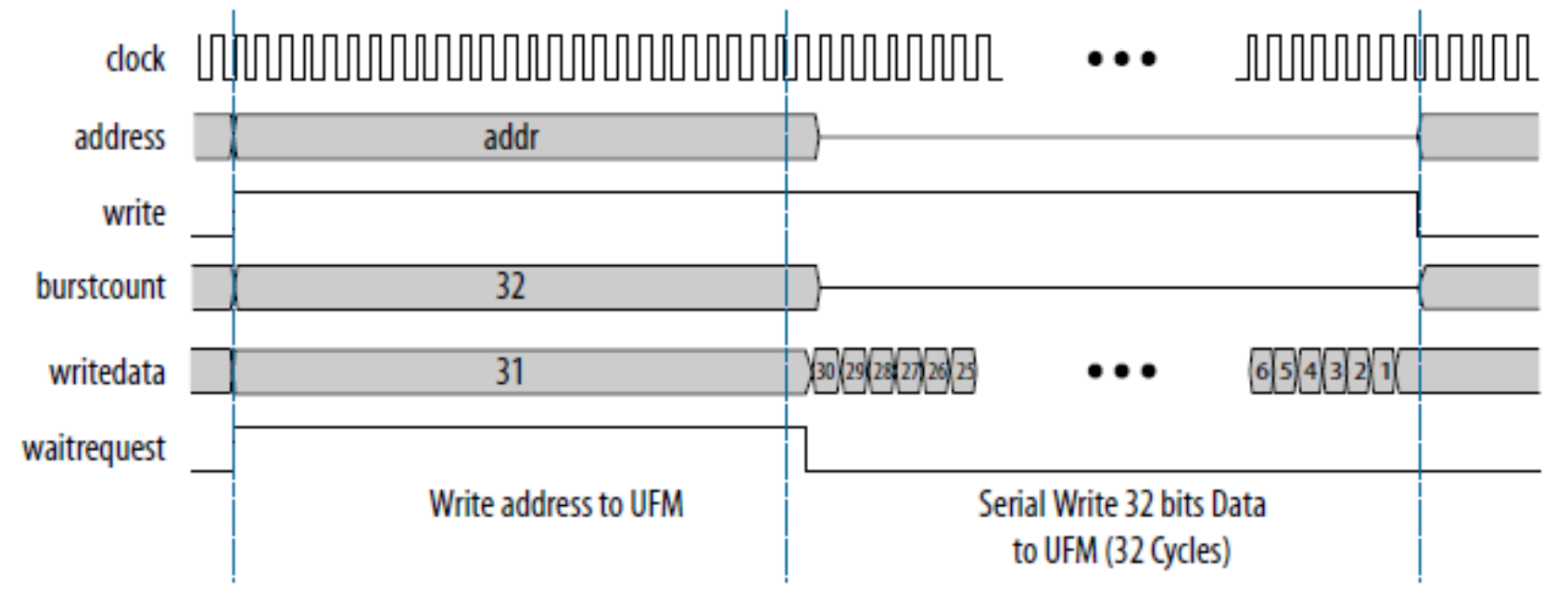
# MAX10 Memory

- User Flash Memory
  - Serial Mode Operation - WRITE

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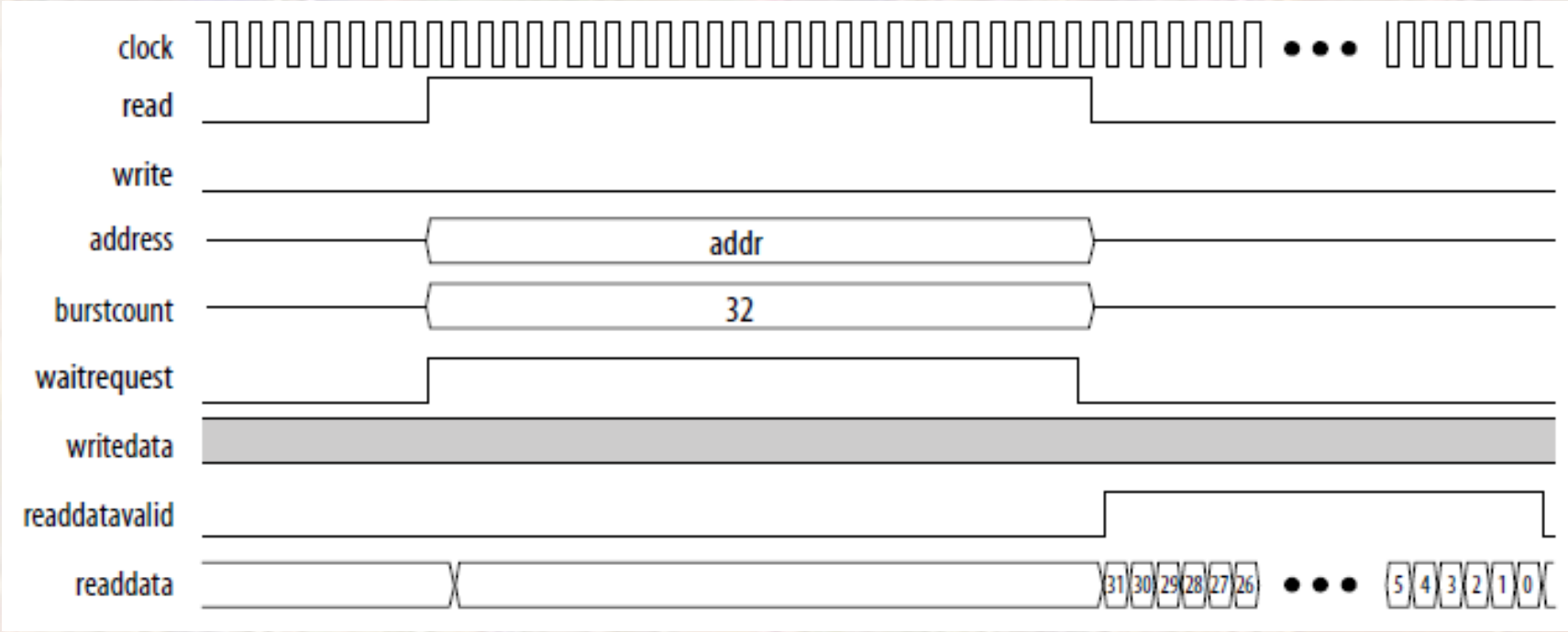
# MAX10 Memory

- User Flash Memory
  - Serial Mode Operation - READ





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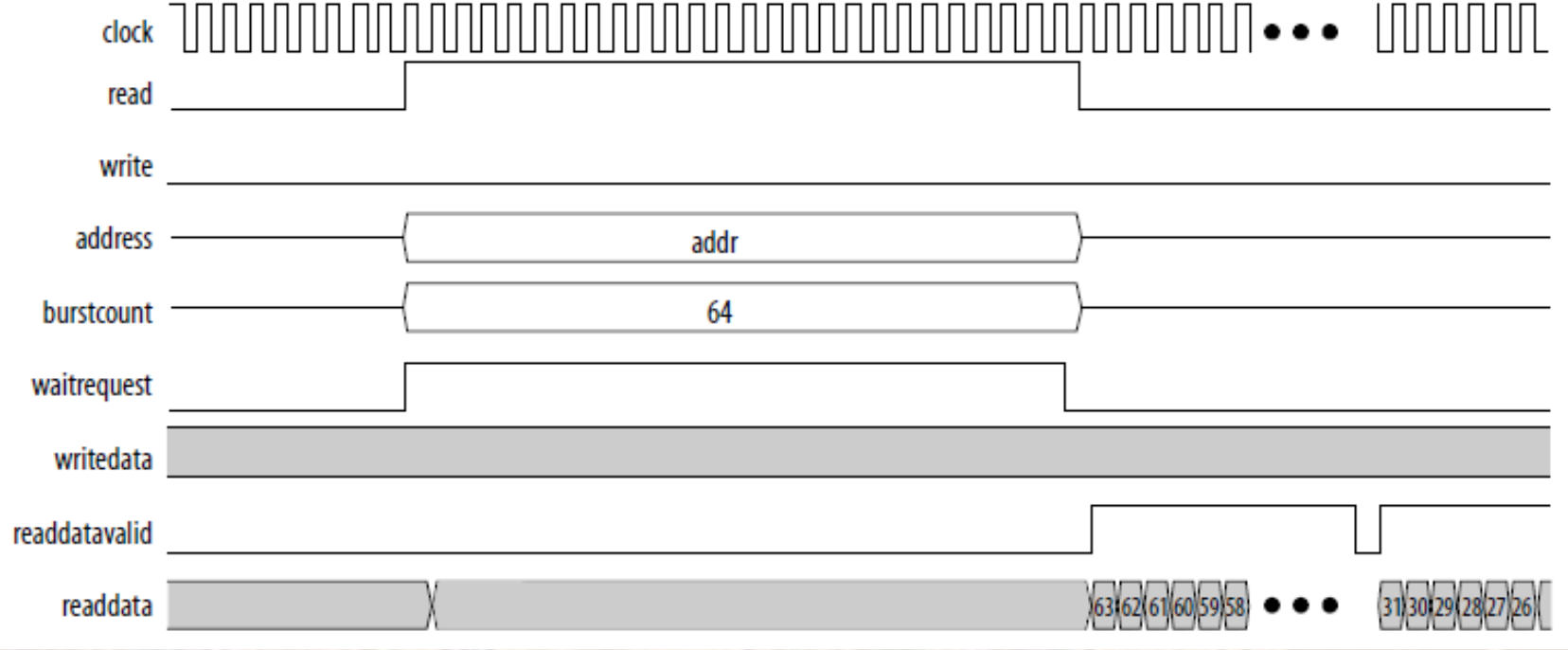
# MAX10 Memory

- User Flash Memory
  - Serial Mode Operation – BURST READ

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