# Last updated 8/10/20

#### These slides describe the operation of the MAX10 Multiplier block

#### Upon completion: You should be able implement a multiplier on the MAX10 FPGA

- Multiplier
  - 144 18 x 18 multipliers
  - Can be configured as 2 9 x 9 multipliers



- Additional Fixed Blocks Multiplier
  - Configured as 2 9 x 9 multipliers



- Multipliers
  - Embedded
    - Signals
      - signa A is signed
      - signb B is signed

Data A		Data B		Docult	
signa Value	Logic Level	signb Value	Logic Level	nesuit	
Unsigned	Low	Unsigned	Low	Unsigned	
Unsigned	Low	Signed	High	Signed	
Signed	High	Unsigned	Low	Signed	
Signed	High	Signed	High	Signed	

Src: MAX 10 Device Handbook

- Multipliers
  - Embedded
    - IP Catalog
      - lpm\_mult standard multiplier
      - altmult\_add uses LEs to implement the adders in multiply/add function
      - altmult\_accum –uses LEs to implement the accumulator in a multiply/accumulate function
      - altmult\_complex complex multiplier
      - altmemmult memory based multiplier

- Multipliers LPM\_MULT
  - Note no signa or signb in this implementation

just an option for signed or unsigned multiplcation

✓ Basic Functions
✓ Arithmetic
ALTERA_CORDIC
ALTERA_FP_ACC_CUSTC
ALTERA_FP_FUNCTIONS
ALTMEMMULT
F ALTMULT_ACCUM (MAC)
ALTMULT_ADD
ALTMULT_COMPLEX
ALTSQRT
LPM_COMPARE
LPM_COUNTER
LPM_DIVIDE
LPM_MULT
PARALLEL_ADD
> Bridges and Adaptors

🕥 Save IP Variation	×
IP variation file name: 9_Q1_EE3921/Projects/Multiplier_Example/mult_18x18	OK
IP variation file type <ul> <li>VHDL</li> </ul>	Cancer
○ Verilog	.:

• Multipliers

🔏 MegaWizard Plug-In Manager [pa	ige 1 of 5]		?	×
LPM_MULT		About	<u>D</u> ocumen	tation
1 Parameter Settings	ary			
General / General2 / Pipel	ining >			
mult_18x18 dataa[170] datab[170]	Currently selected device family:	MAX 10	project/defa	
multiplication	Multiplier configuration			
	Multiply 'dataa' input by 'datab' input			
	O Multiply 'dataa' input by itself (squaring operation)	)		
	How wide should the 'dataa' input ite? 18 How wide should the 'datab' input bo? 18 How should the width of the 'result' output be determine Automatically calculate the width Restrict the width to 36 v bits	bits bits ned?		
Resource Usage 2 dsp_9bit	Cancel < Ba	dk Next	t> Eir	nish

Multipliers

🛪 MegaWizard Plug-In Manag	ger [page 2 of 5] ?	×
DPM_MUL	T <u>A</u> bout <u>D</u> ocum	entation
Parameter Settings     2 EDA     3       General     General2	Summary Pipelining	
mult_18x18 dataa[170] result[350 datab[170]	Datab Input Does the 'datab' input bus have a constant value?   No  Yes, the value is  Multiplication Type Which type of multiplication do you want?  Unsigned Signed	
	Implementation Which multiplier implementation should be used? Use the default implementation Use the dedicated multiplier circuitry (Not available for all families) Use logic elements	
Resource Usage 2 dsp_9bit	Cancel < Back	<u>Fi</u> nish

Multipliers

MegaWizard Plug-In Manager I	nage 3 of 51	7 X
***	Page 2 01 21	· ^
LPM_MULT		About Documentation
1 Parameter 2 EDA 3 Sur Settings	nmary	
General > General2 > Pi	pelining	
	Dissista	
mult_18x18		
dataa[170]	Do you want to pipeline the function?	
datab[170]		
	Yes, I want output latency of 0	clock cycles
	Create an ' <u>a</u> dr' asynchronous dear port	
	Create a 'dken' dock enable dock	
	Optimization	
	What type of optimization do you want?	
	Oefault	
	○ Speed	
	🔿 Area	
Resource Usage		
2 dsp_9bit	Cancel	< Back Next > Finish
	Cancer	

• Multipliers

* MegaWizard Plug-In Manager [page 5 of 5]				
🔄 LPM_MULT		[	About Documentation	
1 Parameter 2 EDA 3 Sumr Settings	nary			
mult_18x18 dataa[170] datab[170] unsigned multiplication	Turn on the files you wish to automatically generated, ar to generate the selected fil MegaWizard Plug-In Manag The MegaWizard Plug-In Ma D:\GDrive\MSOE\19_Q1_EE	o generate. A gray checkmark ind nd a green checkmark indicates a es. The state of each checkbox i er sessions. anager creates the selected files 3921/Projects/Multiplier_Exampl	dicates a file that is in optional file. Click Finish s maintained in subsequent in the following directory: e\	
	File	Description		
	mult_18x18.vhd	Variation file		
	mult_18x18.inc	AHDL Include file		
	mult_18x18.cmp	VHDL component declaration file	2	
	mult_18x18.bsf	Quartus Prime symbol file		
	mult_18x18_inst.vhd	Instantiation template file		
Resource IIsage				
2 dsp 9bit		Cancel Cancel	Next > Finish	

Multipliers

🕽 Quartus Prime IP Files

When you create an Intel IP variation, a Quartus Prime IP File is generated. Quartus Prime IP Files are used to represent the Intel IP in your design. Do you want to add the Quartus Prime IP File to the project?

 $\times$ 

D:\GDrive\MSOE\20\_Q1\_EE3921\Projects\Multiplie...

Automatically add Quartus Prime IP Files to all projects

(Note: Turning on this option permanently suppresses this dialog box. You can change this setting in the Options dialog box)

Multipliers

```
---
    multiplier_example.vhdl
---
    by: johnsontimoj
___
    created: 8/17/2018
_ _
    version: 0.0
_ _
    Multiplier example
_ _
    inputs: multiplier, multiplicand
_ _
    outputs: product
_ _ _ .
library ieee;
use ieee std_logic_1164 all:
use ieee.numeric_std.all;
entity multiplier_example is
   port ( i_multiplicand:
                                in std_logic_vector(17 downto 0);
             i_multiplier:
                                in std_logic_vector(17 downto 0);
            o_product:
                                out std_logic_vector(35 downto 0)
         ):
end entity:
```

```
architecture behavioral of multiplier_example is
   component mult_18x18
   PORT
   (
               : IN STD_LOGIC_VECTOR (17 DOWNTO 0);
      dataa
      datab
              : IN STD_LOGIC_VECTOR (17 DOWNTO 0);
      result
              : OUT STD_LOGIC_VECTOR (35 DOWNTO 0)
   );
   end component;
begin
  mult_18x18_inst : mult_18x18 PORT MAP (
              => i_multiplicand,
      dataa
              => i_multiplier,
      datab
      result => o_product
   );
end architecture;
```



- Multipliers
  - Soft Multipliers
    - RAM based Look Up Table
      - All possible solutions stored
      - Used for constant coefficient multiplication
      - ALTMEMMULT
    - Logic based