MAX 10 PLLs MegaWizard

Last updated 9/28/22

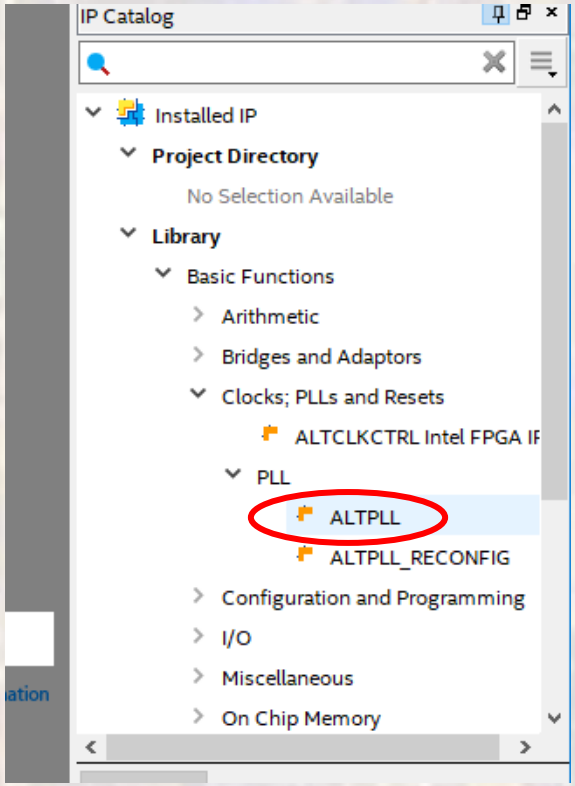
PLL Basics

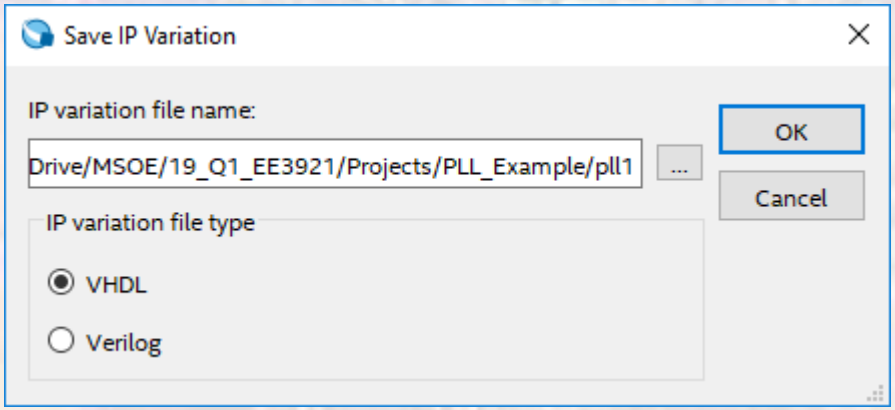
These slides describe the use of the MAX10 PLL MegaWizard tool

Upon completion: You should be able create your own PLLs using the MegaWizard

MAX10 PLL MegaWizard

- MegaFunction AltPll





MAX10 PLL MegaWizard

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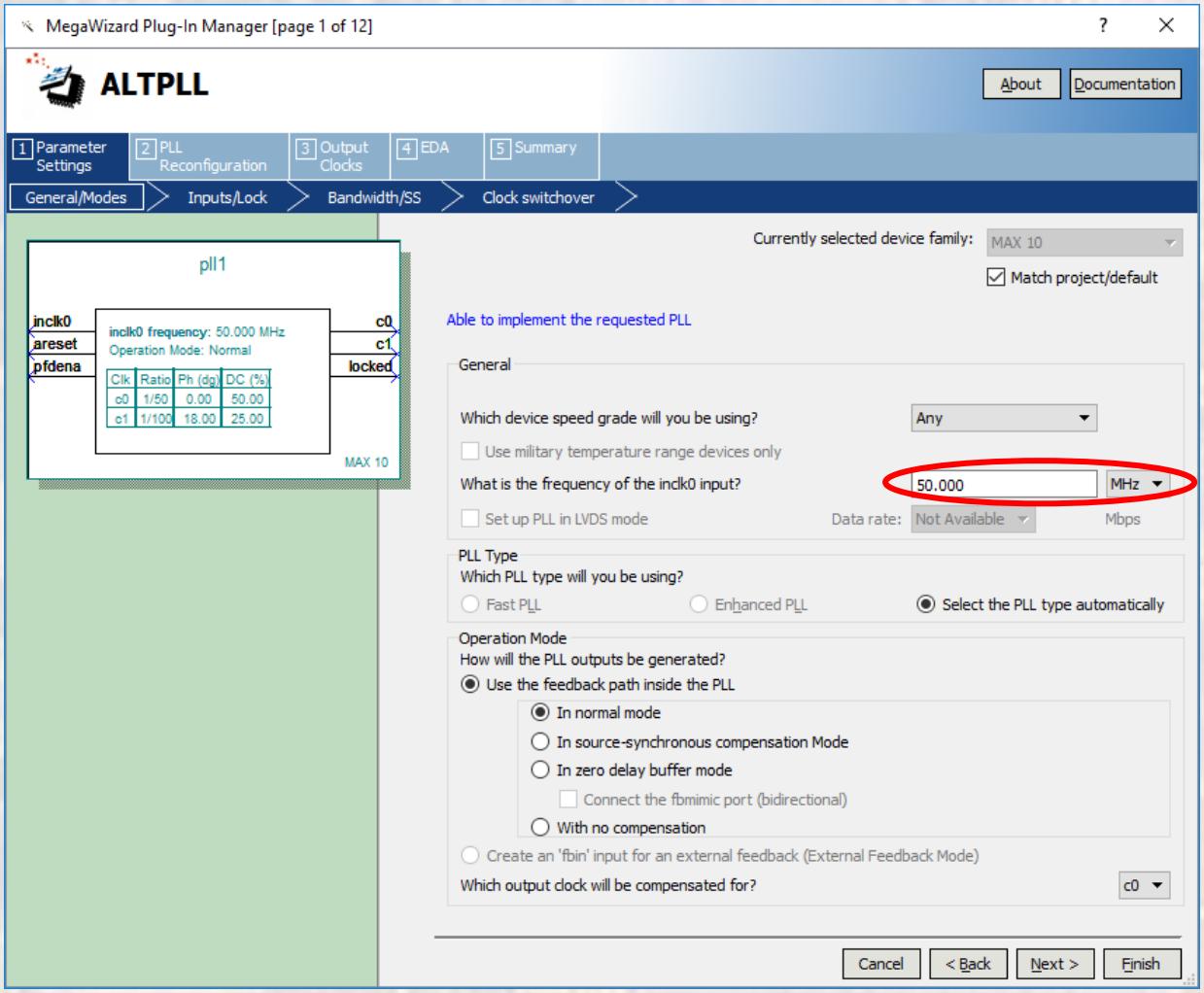

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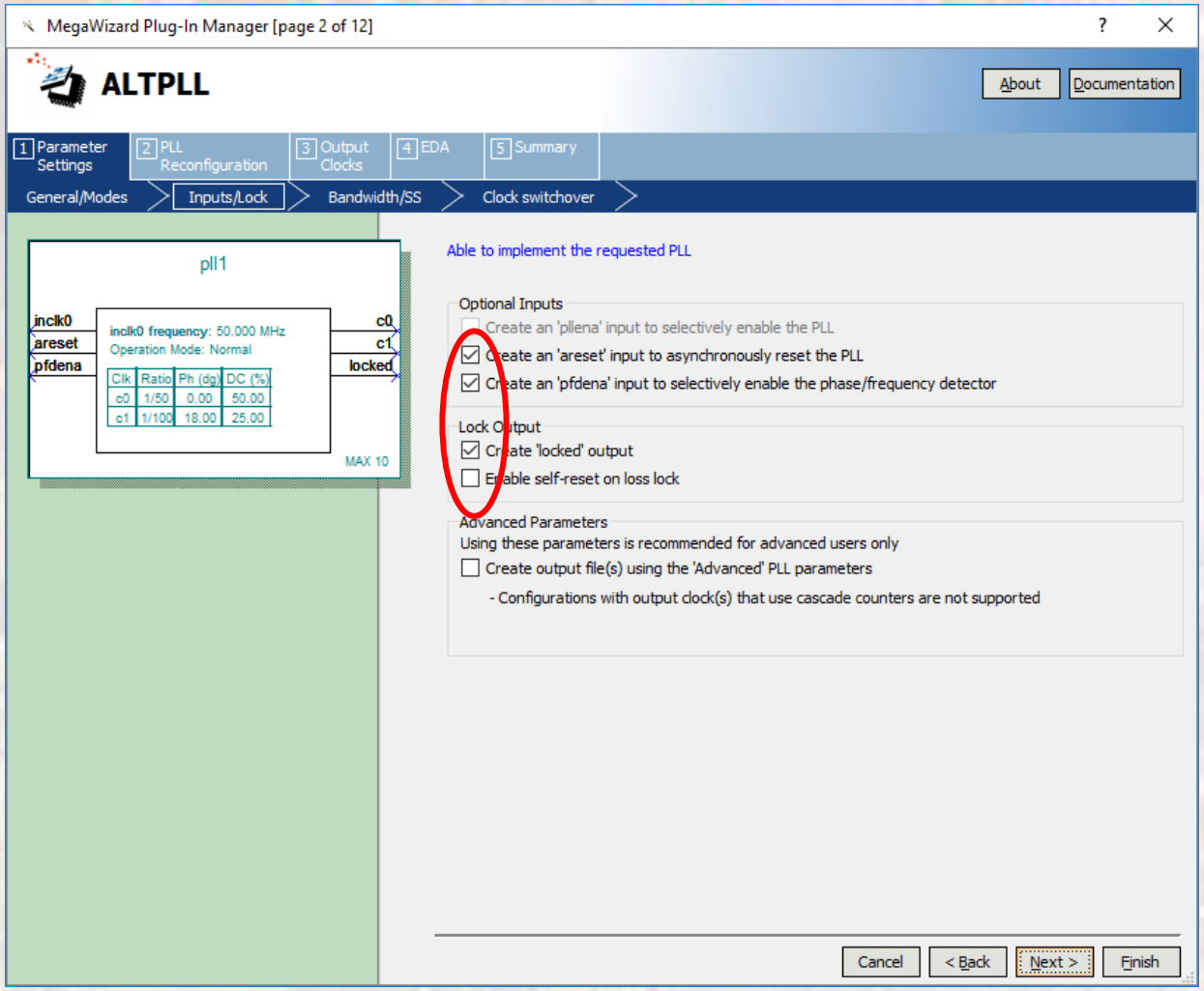

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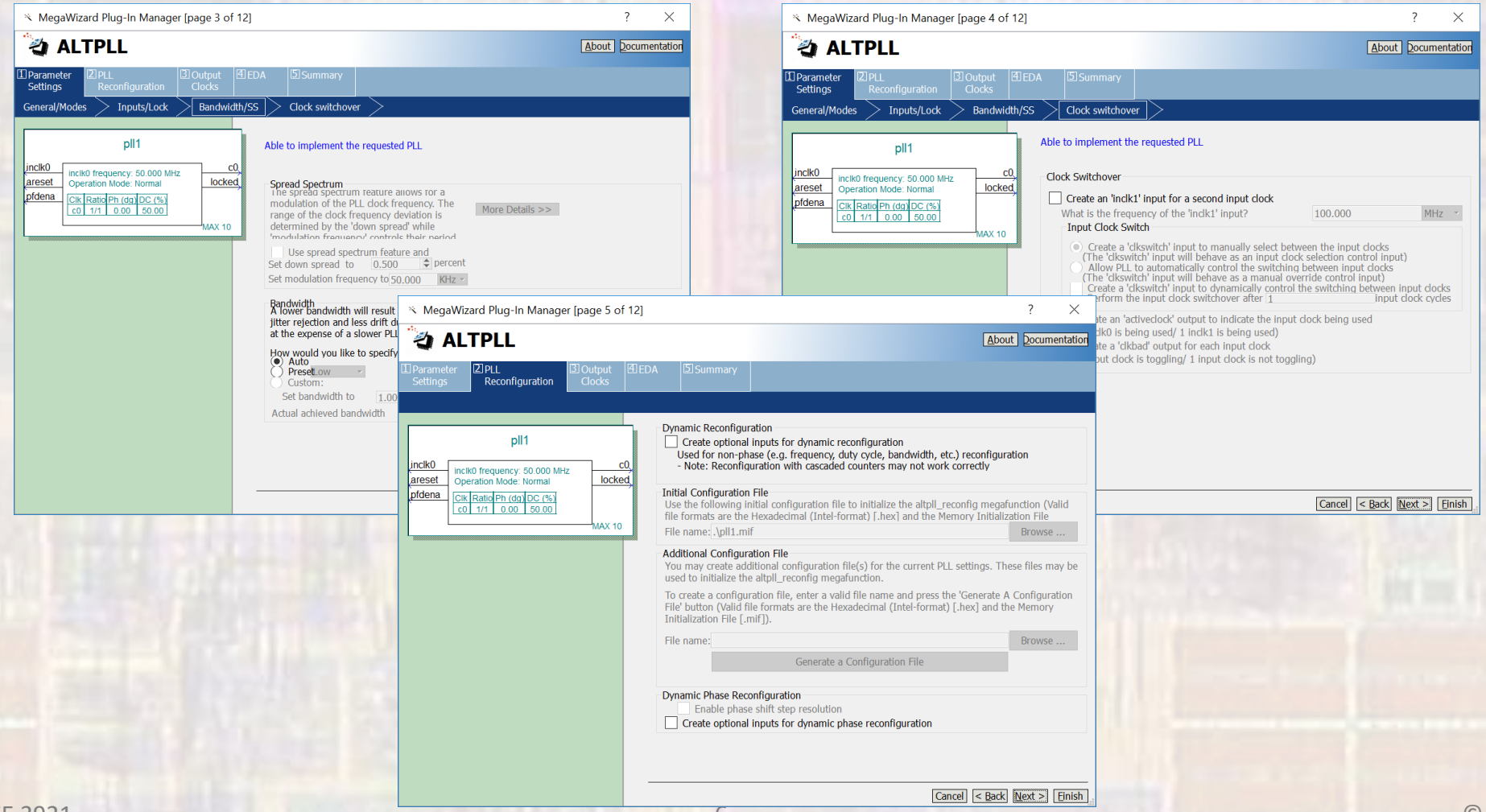

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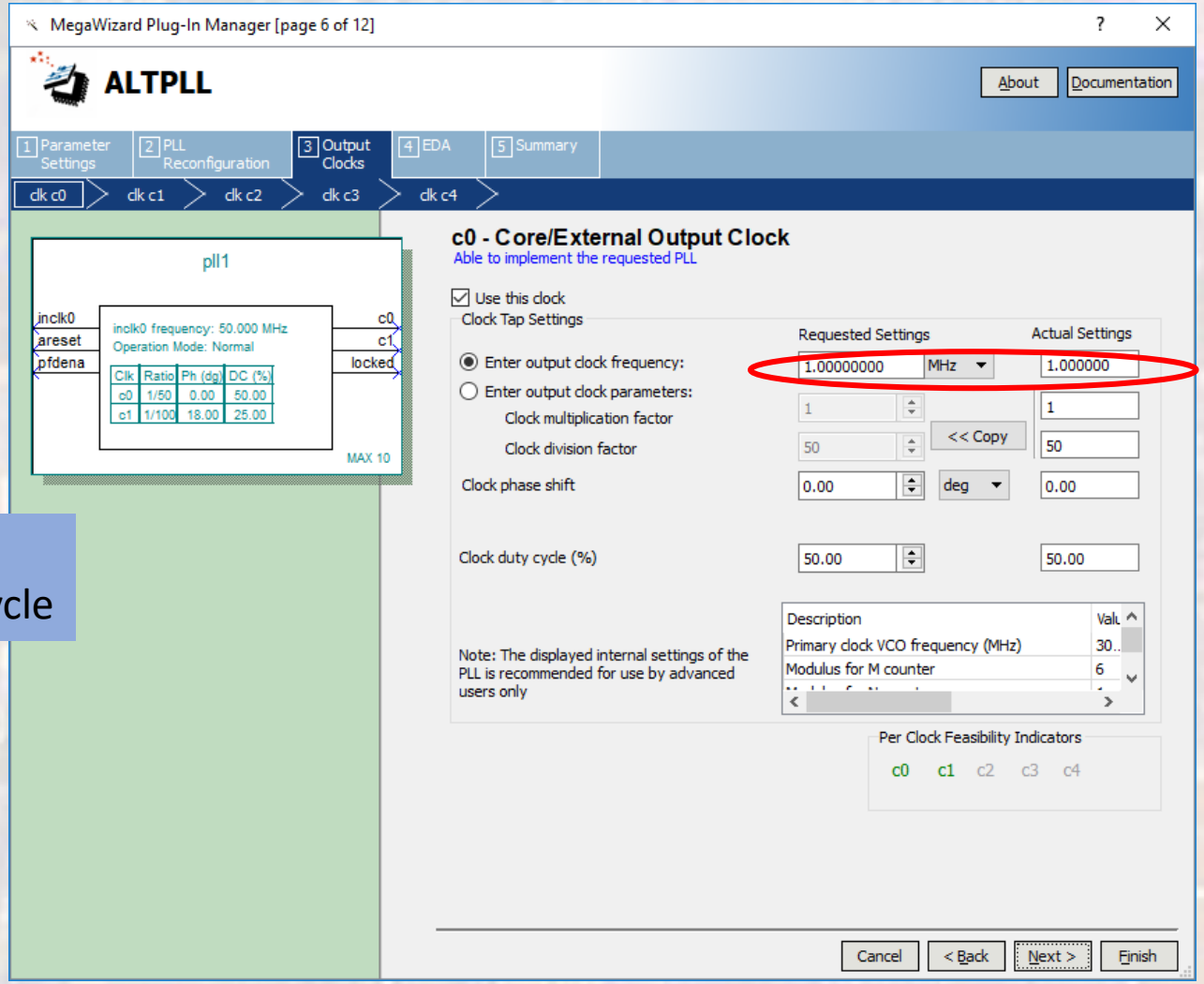

1MHz clk
50% duty cycle

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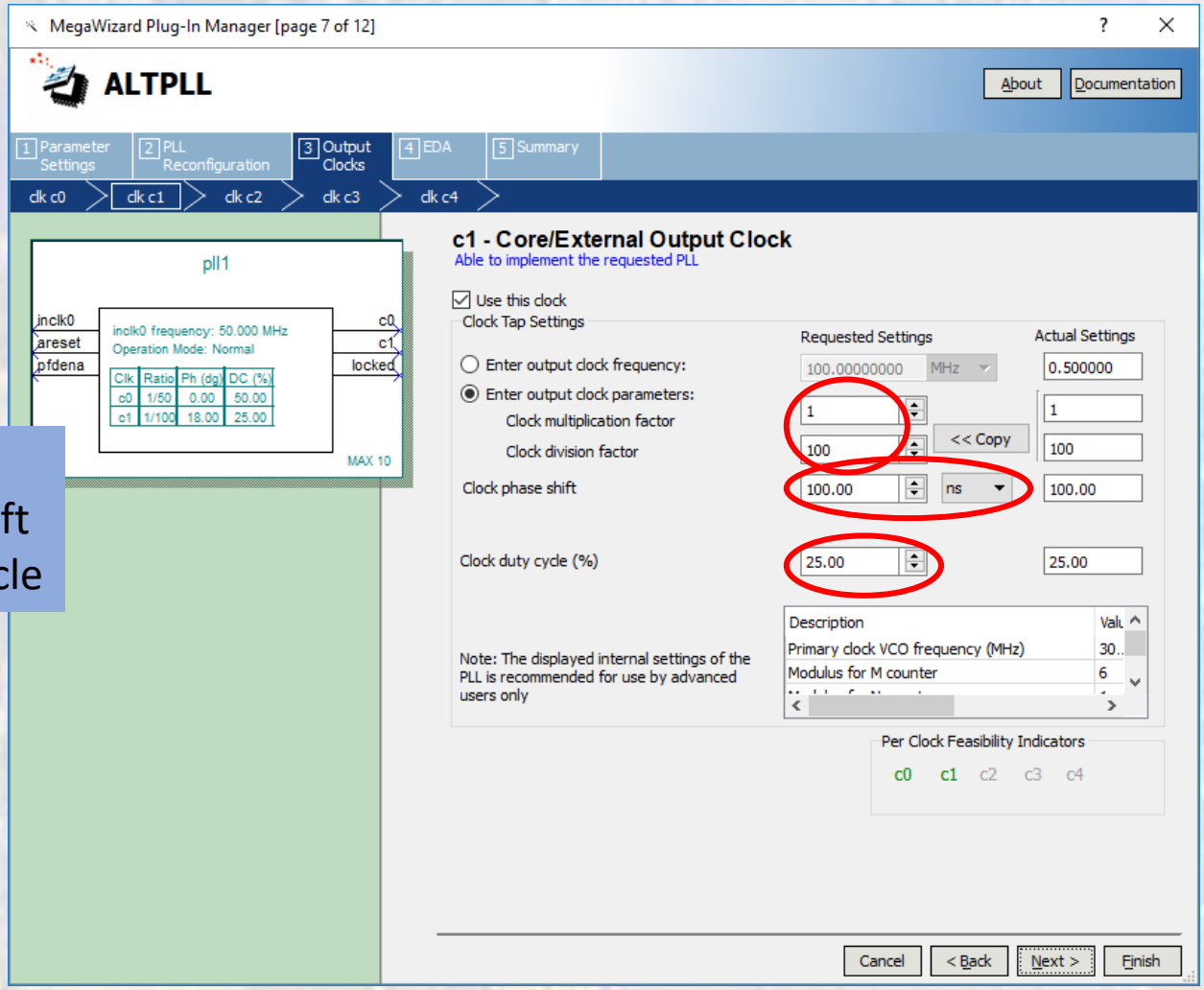
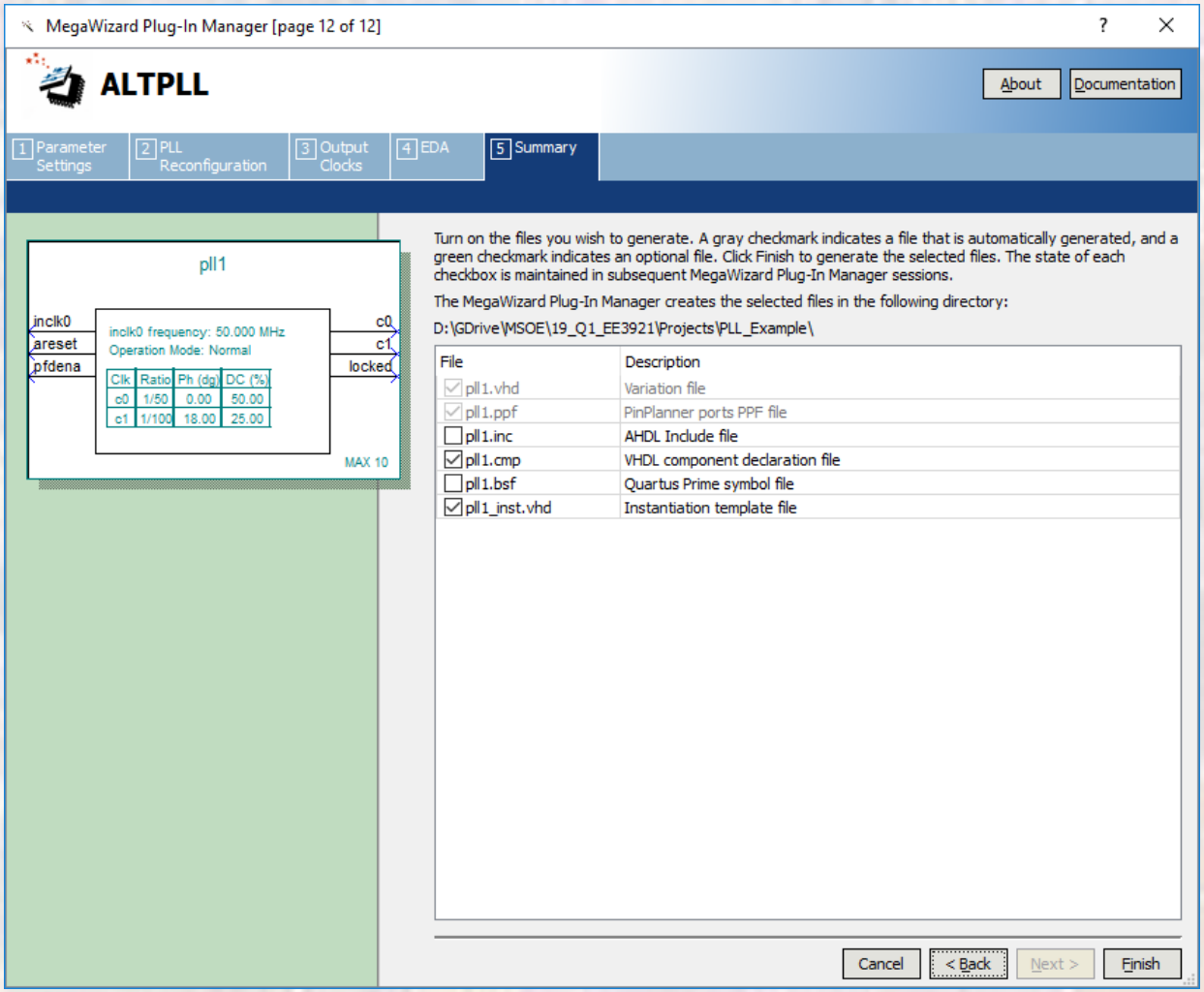
- MegaFunction AltPll



500KHz clk
100ns ph shift
25% duty cycle

MAX10 PLL MegaWizard

- MegaFunction AltPll



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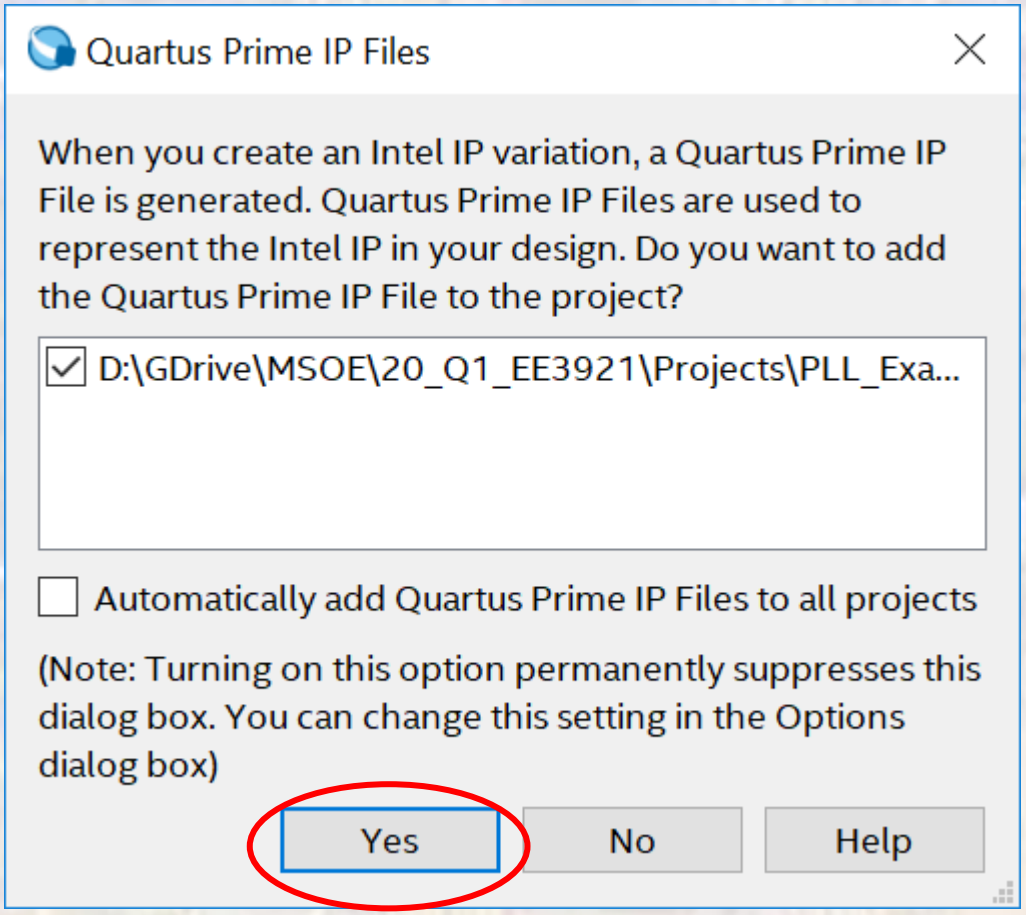

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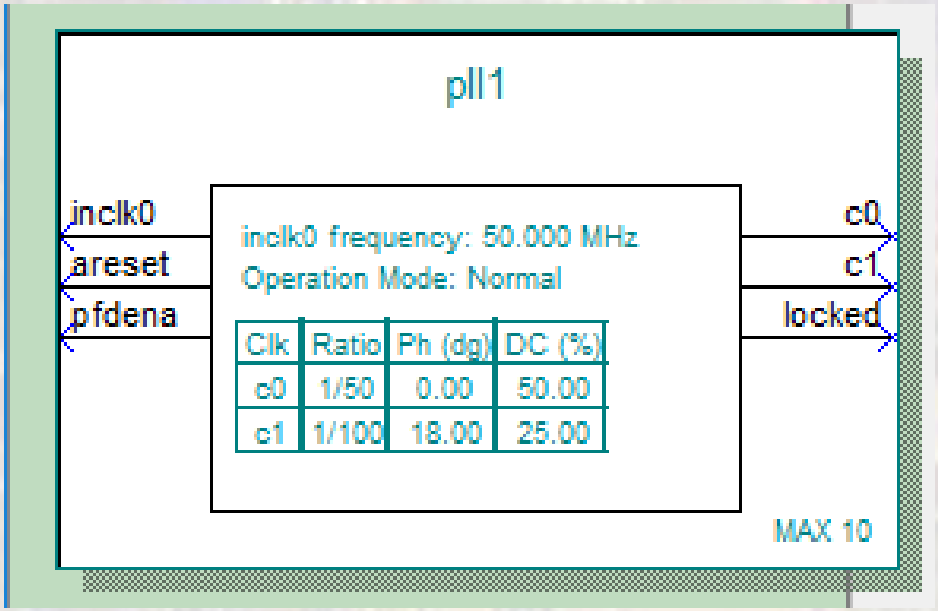
- MegaFunction AltPll

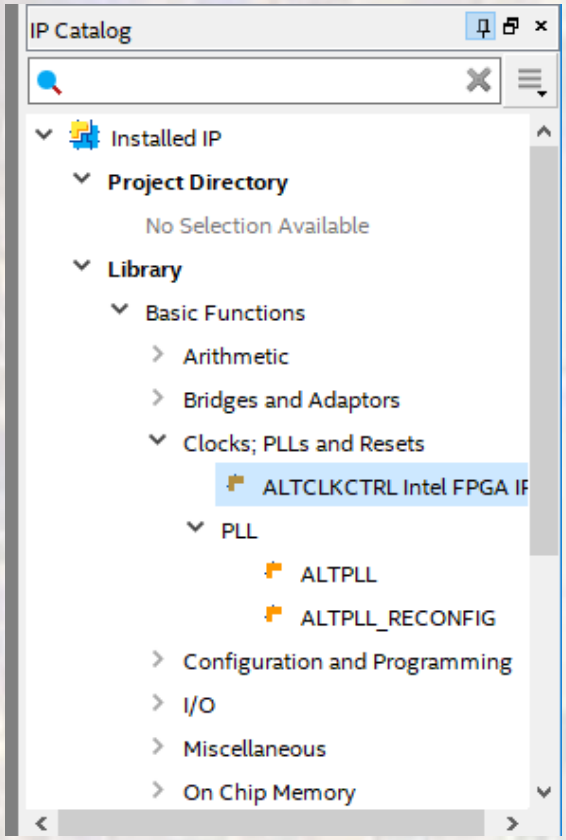



```
component pll1
    PORT
    (
        areset      : IN STD_LOGIC  := '0';
        inclk0      : IN STD_LOGIC  := '0';
        pfdena      : IN STD_LOGIC  := '1';
        c0          : OUT STD_LOGIC ;
        c1          : OUT STD_LOGIC ;
        locked      : OUT STD_LOGIC
    );
end component;
```

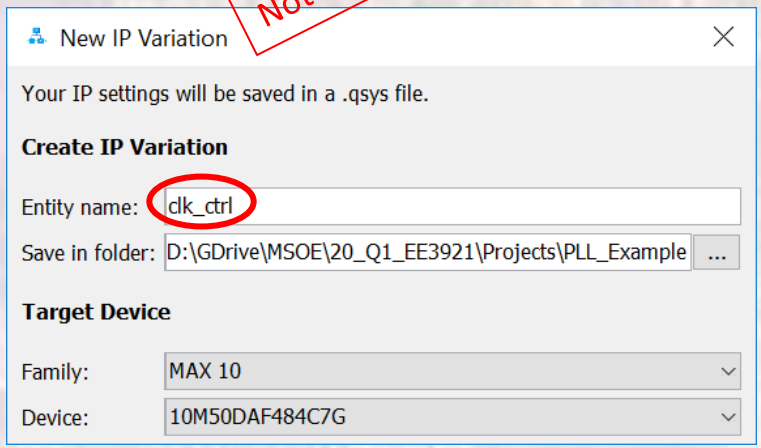
```
pll1_inst : pll1 PORT MAP (
        areset  => areset_sig,
        inclk0  => inclk0_sig,
        pfdena      => pfdena_sig,
        c0   => c0_sig,
        c1   => c1_sig,
        locked => locked_sig
    );
```

MAX10 PLL MegaWizard

- MegaFunction AltClkCtrl
  - Required to get CLOCK_50 to the PLL input



Only required when the PLL is the only block
Not required for any of our designs



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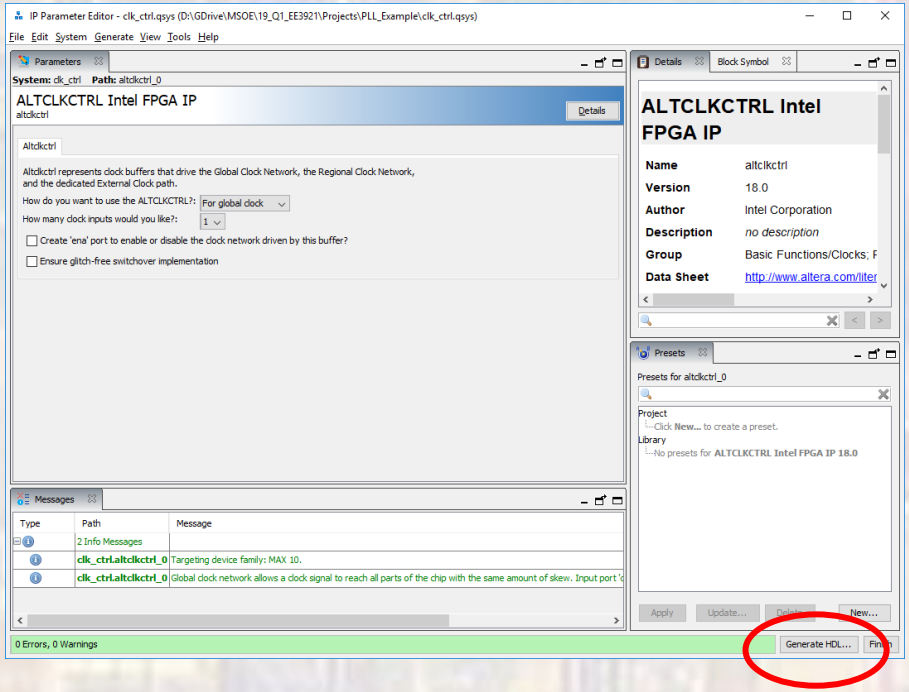

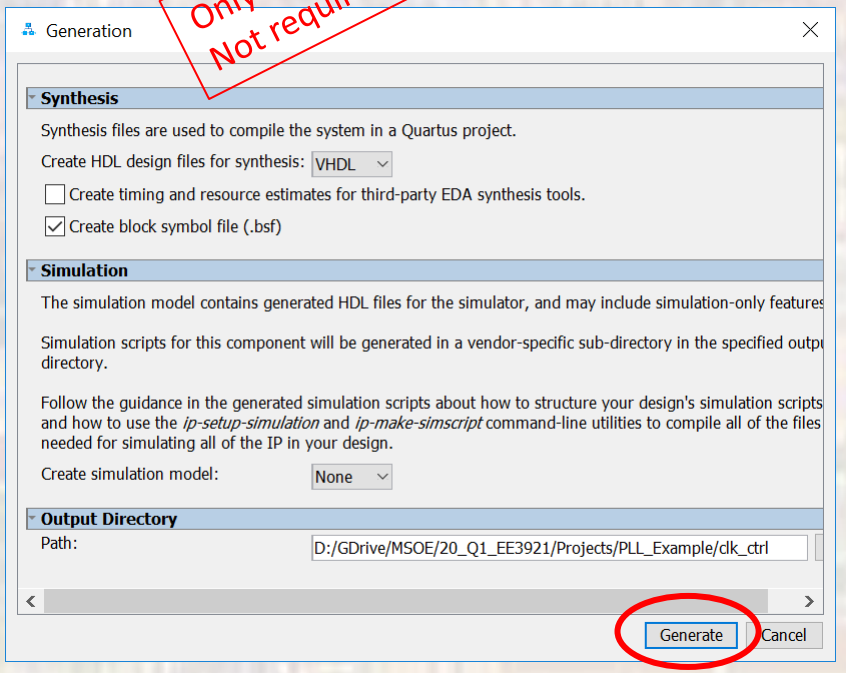

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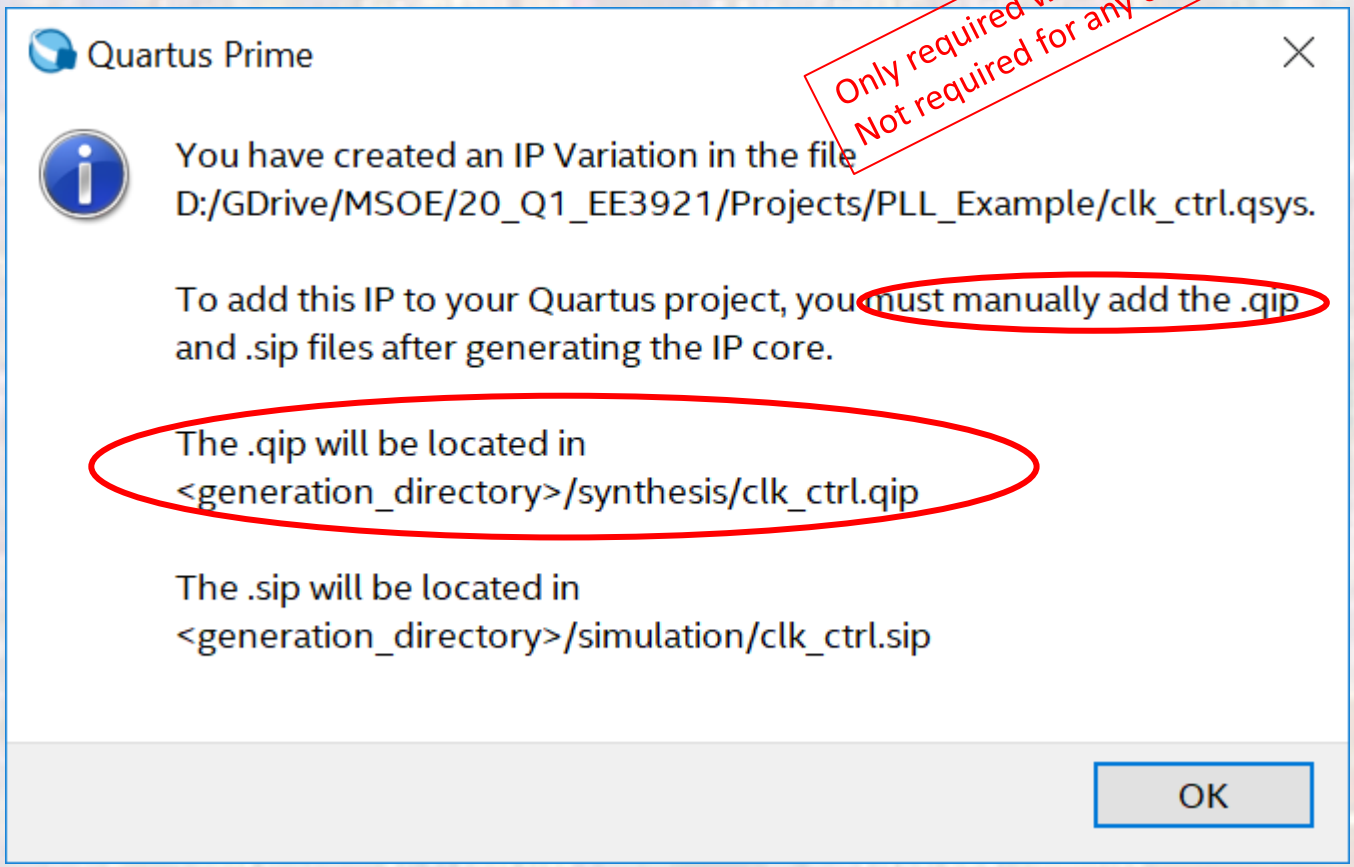
- MegaFunction AltClkCtrl
  - Required to get CLOCK_50 to the PLL input



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MAX10 PLL MegaWizard

- MegaFunction AltPll

```
--
--  pll_example_de10.vhdl
--
--  by: johnsontimoj
--
--  created: 8/12/2018
--
--  version: 0.0
--
----------------------------------
----------------------------------
--
--  PLL example - de10 implementation
--
--  inputs: CLK, enable, reset
--
--  outputs: 3 clocks - different frequencies and phases, locked
--
--  Use System Console - ADC Toolkit for validation
--
----------------------------------

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity pll_example_de10 is
   port  (  CLOCK_50:            in std_logic;
            SW:                  in std_logic_vector(9 downto 0);
            ARDUINO_IO:          inout std_logic_vector(4 downto 0)
         );
end entity;
```

```
architecture hardware of pll_example_de10 is

   signal clk_50_intermediate:   std_logic;

   component pll1
      PORT
      (
         areset      : IN STD_LOGIC  := '0';
         inclk0      : IN STD_LOGIC  := '0';
         pfdena      : IN STD_LOGIC  := '1';
         c0          : OUT STD_LOGIC ;
         c1          : OUT STD_LOGIC ;
         locked      : OUT STD_LOGIC
      );
   end component;

   component clk_ctrl is
      port (
         inclk  : in  std_logic := 'X'; -- inclk
         outclk : out std_logic         -- outclk
      );
   end component clk_ctrl;

begin

   pll1_inst : pll1 PORT MAP (
                              areset      => SW(0),
                              inclk0      => clk_50_intermediate,
                              pfdena      => ARDUINO_IO(0),
                              c0          => ARDUINO_IO(1),
                              c1          => ARDUINO_IO(2),
                              locked      => ARDUINO_IO(3)
      );

   clk1 :  clk_ctrl
      port map (
               inclk  => CLOCK_50,
               outclk => clk_50_intermediate
      );

end architecture;
```

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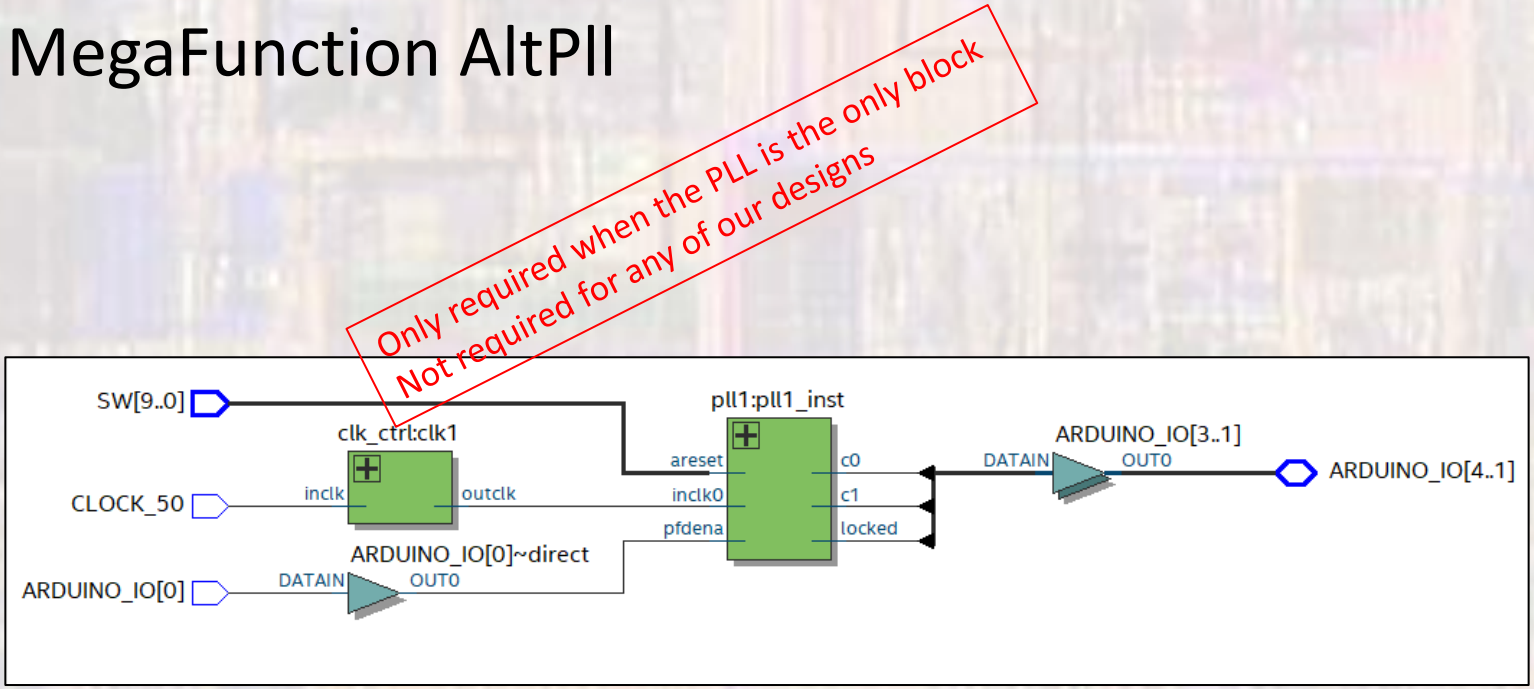
- MegaFunction AltPll



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- MegaFunction AltPll

1MHz clk
50% duty cycle

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500KHz clk
100ns ph shift
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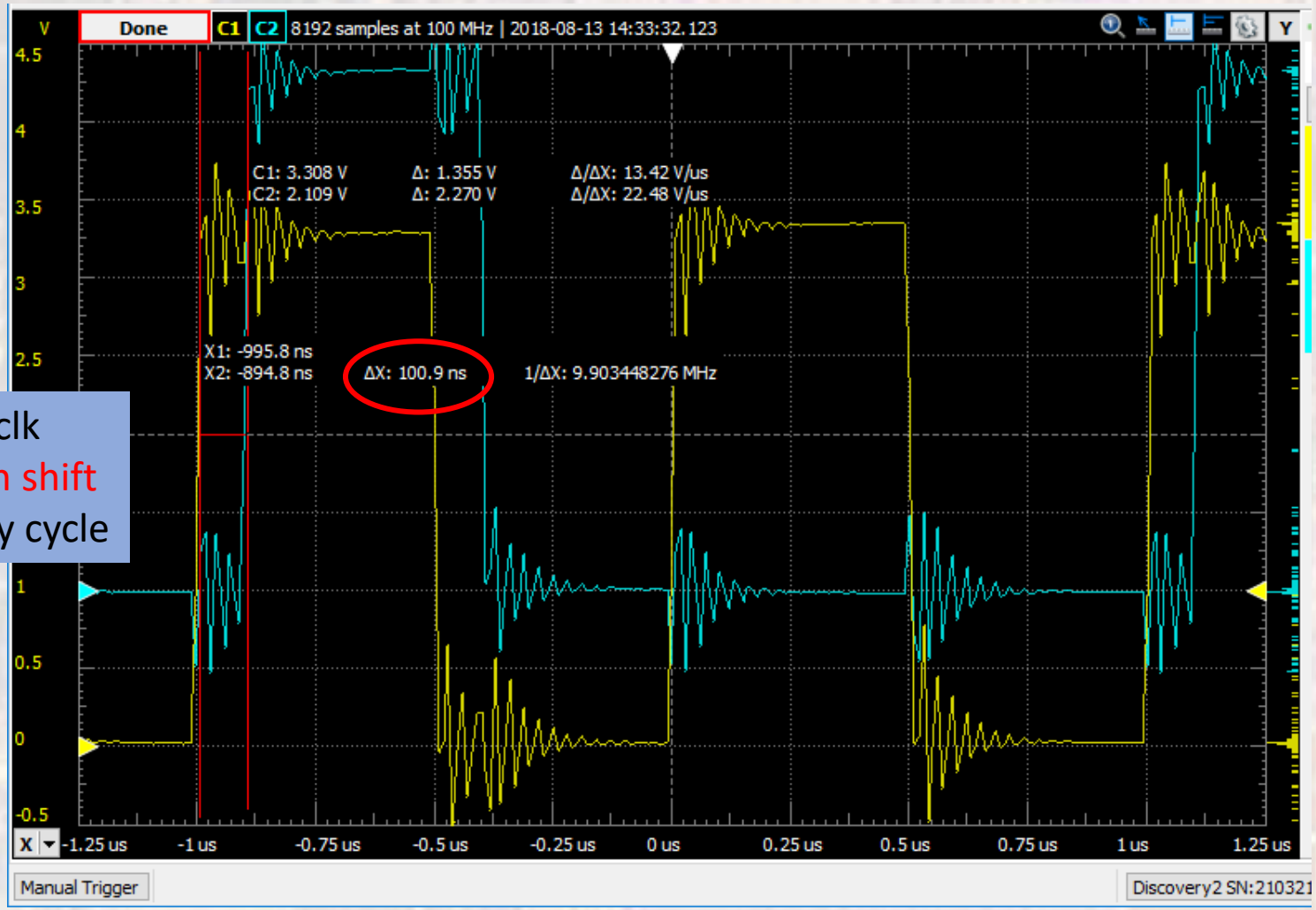

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