NIOS Pixel Display - Intro

Last updated 10/12/20

NIOS II Pixel Display - Intro

These slides describe the Pixel Display IP

Upon completion: You should be able to describe and use the Pixel Display IP

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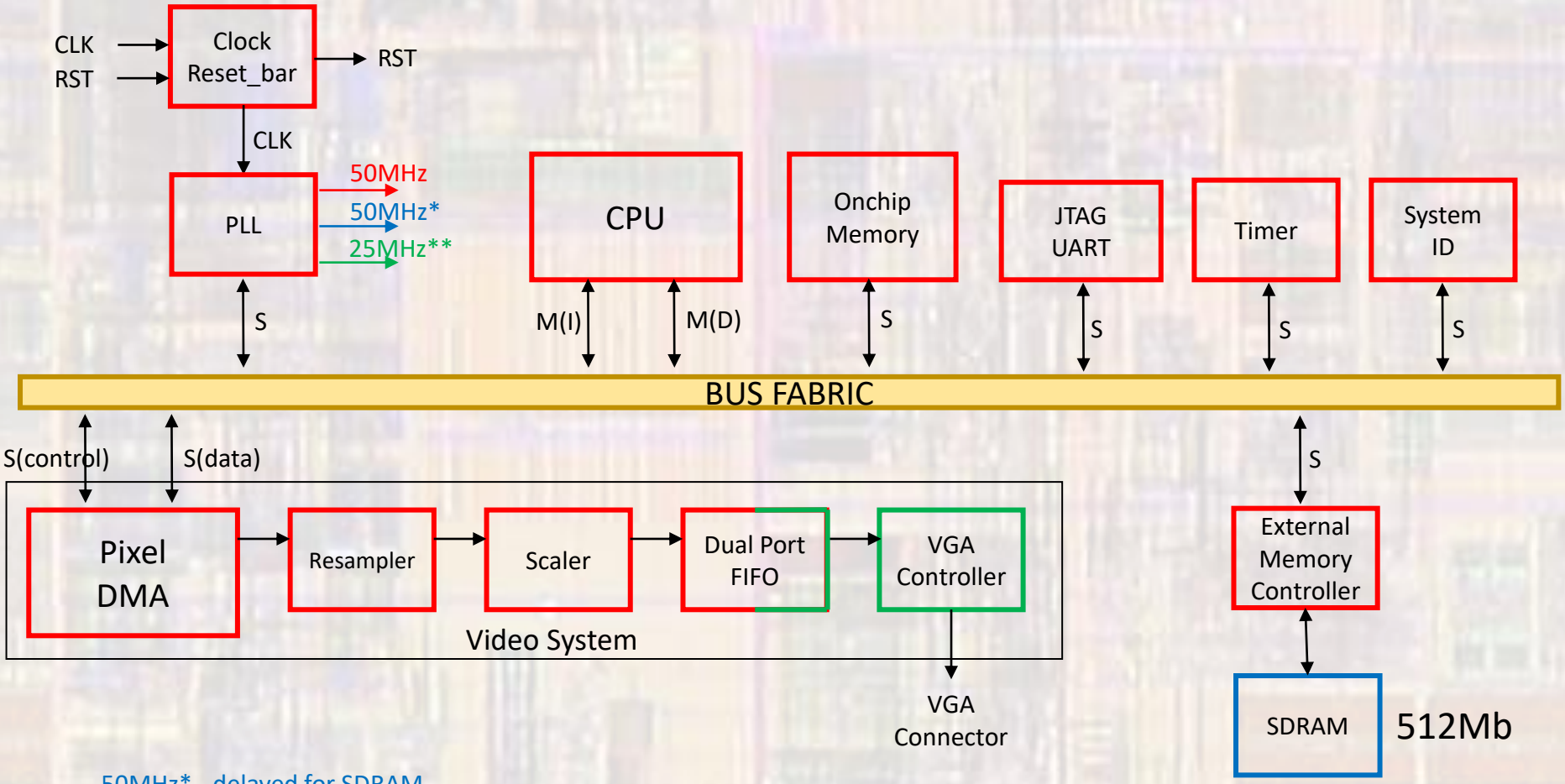

50MHz* - delayed for SDRAM

25MHz** - VGA clk

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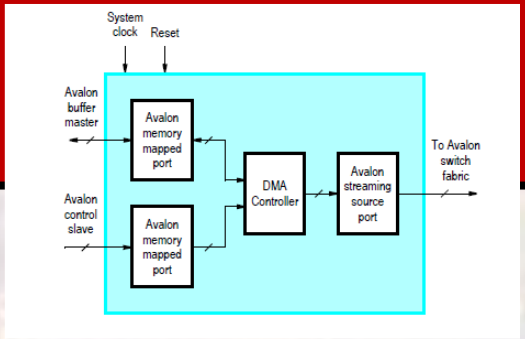
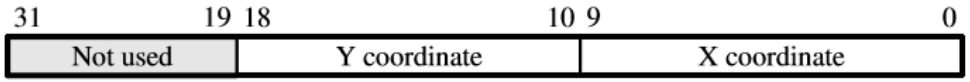


- Pixel Buffer DMA Controller
  - Reads frames from external memory and inserts them into the video data stream
  - DMA based – provide starting address and # of transfers
    - Start address and size of display
  - Supports 2 starting addresses (buffer and back buffer)
  - Separate control and data interfaces
  - Selectable color space format
  - Support for consecutive or X-Y addressing modes
    - Consecutive – location (1,2) for a 640x480 display would be located at memory offset 640(1) + 2 = 642
    - X-Y- location is built into the address offset



b) X-Y address format for the 640 × 480 resolution

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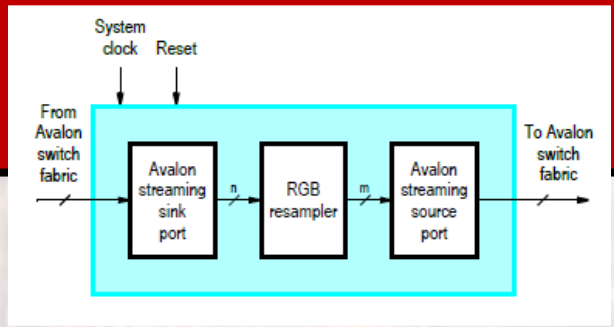

- RGB Resampler
  - Converts video data streams between color formats
    - Lots of color formats supported
    - Can support the addition of an Alpha value if required
      - Alpha is a measure of transparency (0 = fully transparent, 1 = opaque)
    - E.g. 16bit RGB → 30bit RGB

- 16-Bit RGB — This format uses 5 bits for red, and 6 bits for green and 5 bits for blue as shown in Figure 9. This mode is defined as 16 bits per symbol and one symbol per beat.

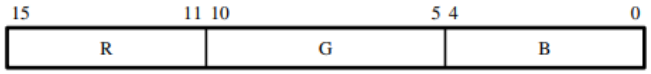

Figure 9. 16-bit RGB Color Space.

- 30-bit RGB — This format uses 10 bits for each color as shown in Figure 11. This mode is defined as 10 bits per symbol and three symbols per beat.

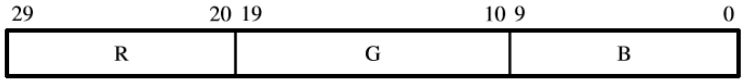

Figure 11. 30-bit RGB Color Space.

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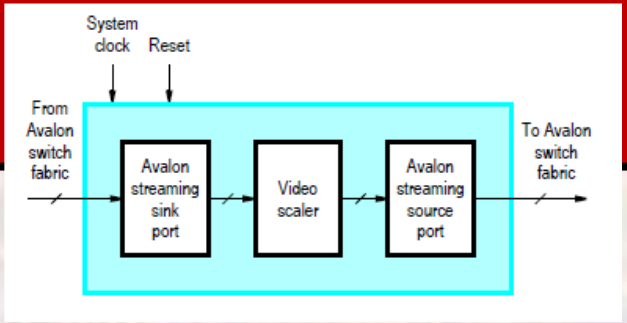

- Scaler
  - Modifies the resolution of a video data stream
    - Adds or removes entire rows and columns
  - When adding rows or columns the data is replicated
  - When removing rows and columns, the first row/column is sent through and any removed rows/columns are dropped
    - No interpolation or averaging
  - Supports scaling factors: 0.25, 0.5, 0.75, 1, 2, 4, 8

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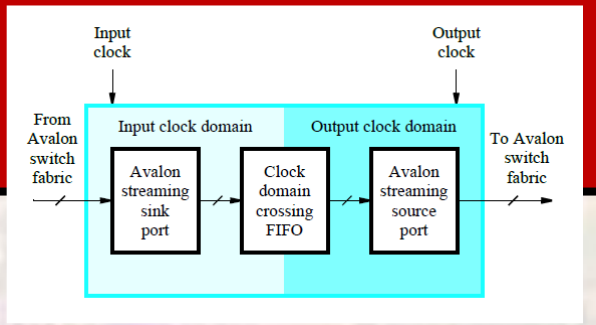

- Dual Clock FIFO
  - Transfers data across two different clock domains
  - Output clock is set by the output resolution
    - VGA 640x480 clock is 25MHz
  - Input clock is determined by system design requirements
    - We will typically use 50MHz
  - Data format is programmable
    - Symbol: a complete piece of data
    - Beat: a unit of transmission – one complete set of data
    - The VGA driver requires:

      10bits/color 3 colors per pixel location

      →

      10bit symbols 3 symbols / beat

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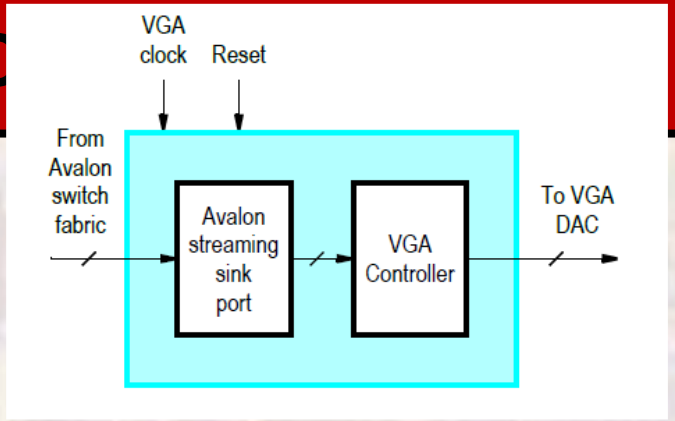

- VGA Controller Block
  - Receives VGA data to be displayed
  - Adds the required VGA timing signals
  - Transmits the new data to the VGA block (DAC) on the DE10 Lite board
  - Supports various screen resolutions from VGA 640×480 pixels to WSXGA 1680x1050, including HDTV 1280x720
    - Note - different resolutions require different clock frequencies
  - Input: Requires 3 planes (RGB) of 10bits each
    - Note – The DE10 DAC outputs 4 bit data
    - It's not clear how the 10bit to 4bit conversion is mapped

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- SDRAM Controller
  - Creates the signals required to R/W the external SDRAM
  - Does not provide the external SDRAM clock signal
  - SDRAM requirements dictate controller parameters
    - -3ns offset for the external SDRAM clock