NIOS SPI

Last updated 10/12/20

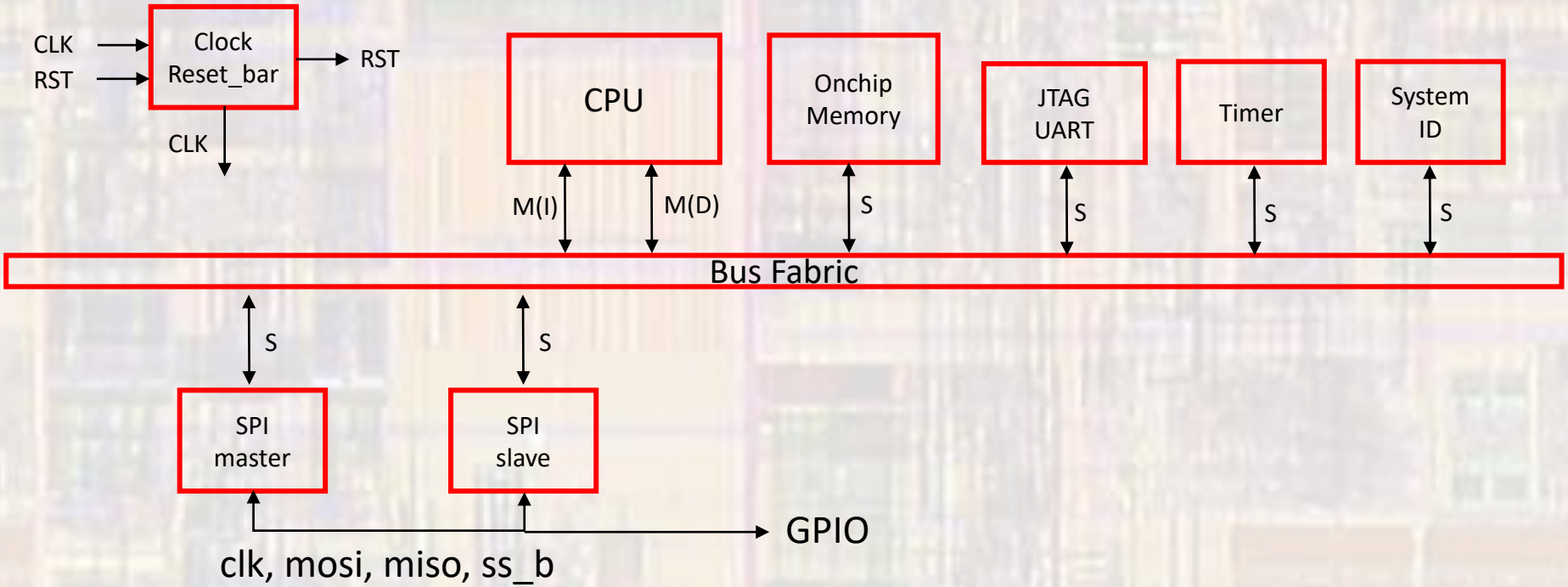
NIOS SPI

These slides describe the operation of the Serial Peripheral Interface (SPI) in a NIOS system

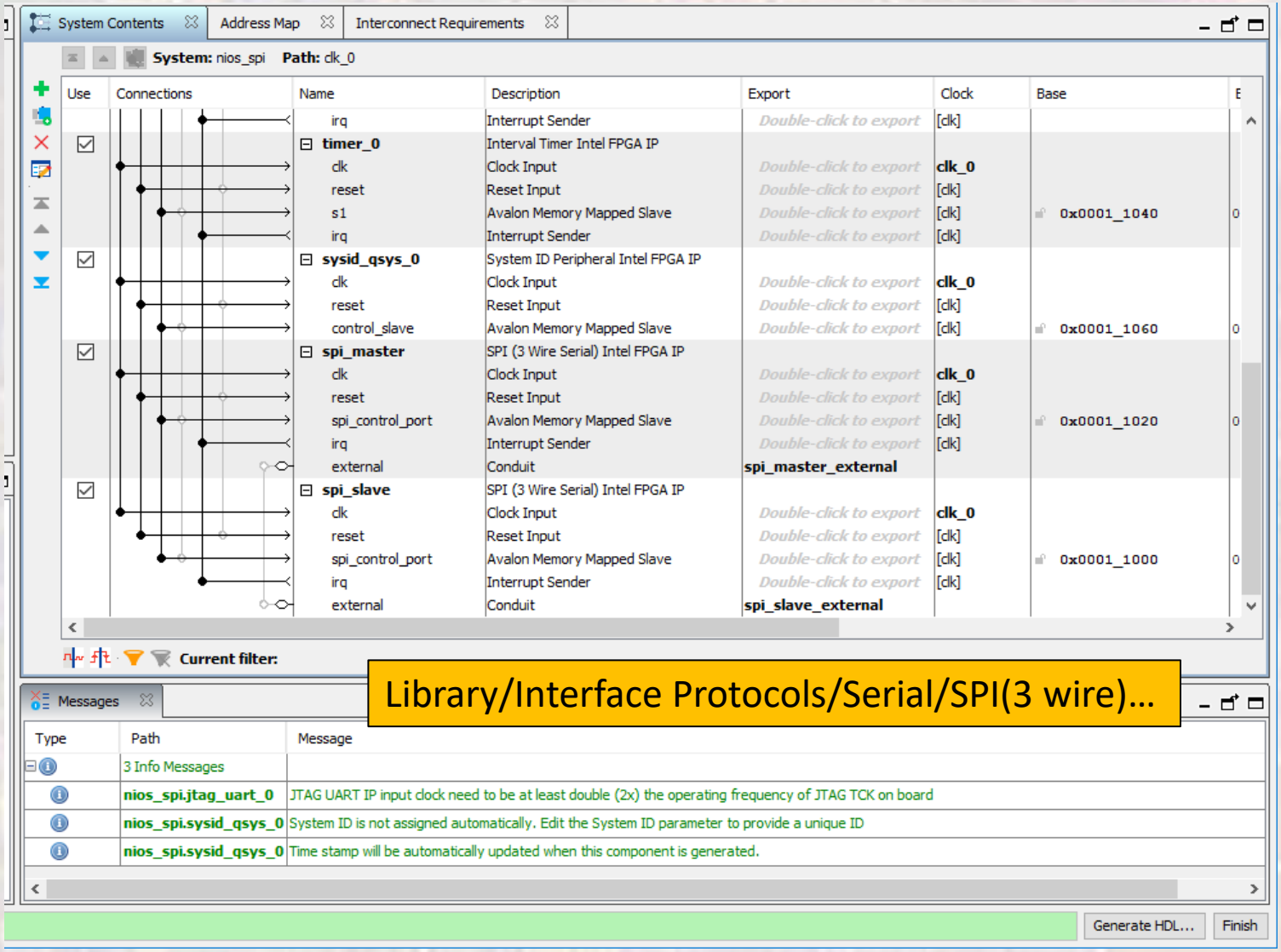
Upon completion: You should be able to develop your own NIOS based SPI System

NIOS SPI

- NIOS SPI System
  - Use 2 SPI modules, in loopback mode



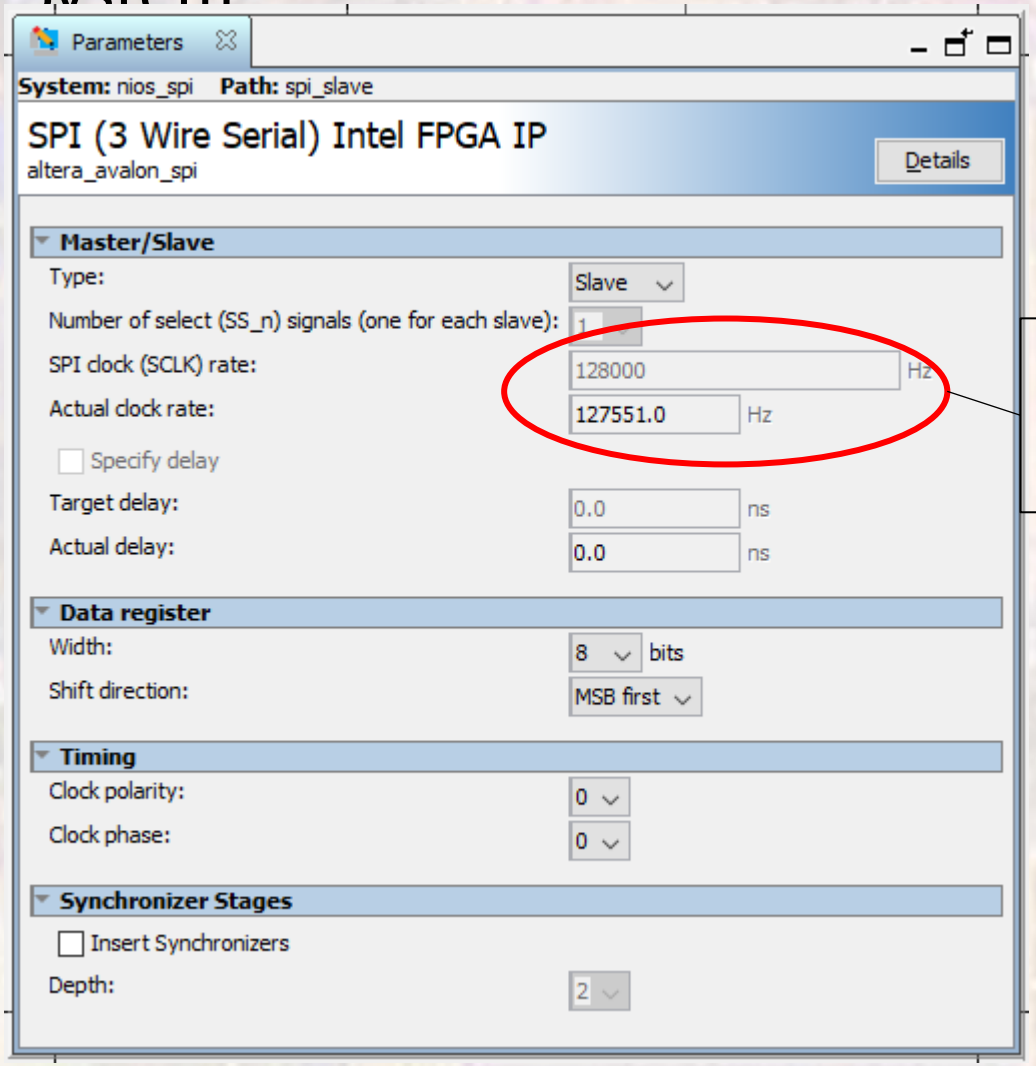
NIOS SPI



Library/Interface Protocols/Serial/SPI(3 wire)…

NIOS SPI

- NIOS SPI System



Creates the required divide by circuity in the Master

NIOS SPI

- NIOS SPI System

```
--------------------------------------
--
-- nios_spi_de10.vhdl
--
-- Created  9/18/18
-- by:      johnsontimoj
-- rev:     0
--
--------------------------------------
--
-- Basic Nios system - with spi - loopback
--
--------------------------------------

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity nios_spi_de10 is
   port(
      CLOCK_50 :     in std_logic;
      GPIO:          out std_logic_vector(3 downto 0)
   );
end entity;
```

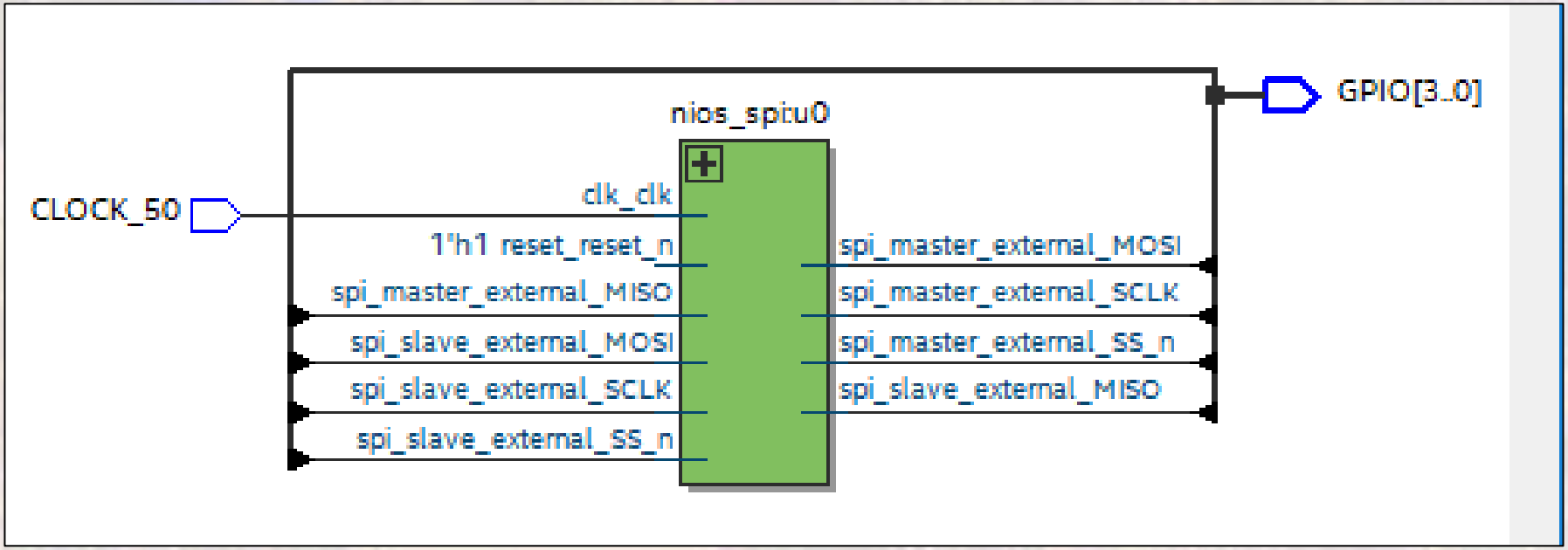
```
architecture behavioral of nios_spi_de10 is

    component nios_spi is
        port (
            clk_clk                 : in  std_logic := 'X'; -- clk
            reset_reset_n           : in  std_logic := 'X'; -- reset_n
            spi_slave_external_MISO  : out std_logic;       -- MISO
            spi_slave_external_MOSI  : in  std_logic := 'X'; -- MOSI
            spi_slave_external_SCLK  : in  std_logic := 'X'; -- SCLK
            spi_slave_external_SS_n  : in  std_logic := 'X'; -- SS_n
            spi_master_external_MISO : in  std_logic := 'X'; -- MISO
            spi_master_external_MOSI : out std_logic;       -- MOSI
            spi_master_external_SCLK : out std_logic;       -- SCLK
            spi_master_external_SS_n : out std_logic        -- SS_n
        );
    end component nios_spi;

   signal MISO:   std_logic;
   signal MOSI:   std_logic;
   signal SCLK:   std_logic;
   signal SS_bar: std_logic;

begin

 u0 : component nios_spi
        port map (
            clk_clk                 => CLOCK_50,        --                 clk.clk
            reset_reset_n           => '1',             --               reset.reset_n
            spi_slave_external_MISO  => MISO,           --  spi_slave_external.MISO
            spi_slave_external_MOSI  => MOSI,           --                    .MOSI
            spi_slave_external_SCLK  => SCLK,           --                    .SCLK
            spi_slave_external_SS_n  => SS_bar,         --                    .SS_n
            spi_master_external_MISO => MISO,           -- spi_master_external.MISO
            spi_master_external_MOSI => MOSI,           --                    .MOSI
            spi_master_external_SCLK => SCLK,           --                    .SCLK
            spi_master_external_SS_n => SS_bar          --                    .SS_n
        );

        GPIO(0) <= MISO;
        GPIO(1) <= MOSI;
        GPIO(2) <= SCLK;
        GPIO(3) <= SS_bar;

end architecture;
```

loopback signals

access for Analog Discovery

NIOS SPI

- NIOS SPI System



NIOS SPI

- NIOS SPI System

nios_spi_1.c | altera_avalon_spi_regs.h

```
33
34 #include <io.h>
35
36 #define ALTERA_AVALON_SPI_RXDATA_REG                    0
37 #define IOADDR_ALTERA_AVALON_SPI_RXDATA(base)           __IO_CALC_ADDRESS_NATIVE(base, ALTERA_AV
38 #define IORD_ALTERA_AVALON_SPI_RXDATA(base)             IORD(base, ALTERA_AVALON_SPI_RXDATA_REG)
39 #define IOWR_ALTERA_AVALON_SPI_RXDATA(base, data)       IOWR(base, ALTERA_AVALON_SPI_RXDATA_REG,
40
41 #define ALTERA_AVALON_SPI_TXDATA_REG                    1
42 #define IOADDR_ALTERA_AVALON_SPI_TXDATA(base)           __IO_CALC_ADDRESS_NATIVE(base, ALTERA_AV
43 #define IORD_ALTERA_AVALON_SPI_TXDATA(base)             IORD(base, ALTERA_AVALON_SPI_TXDATA_REG)
44 #define IOWR_ALTERA_AVALON_SPI_TXDATA(base, data)       IOWR(base, ALTERA_AVALON_SPI_TXDATA_REG,
45
46 #define ALTERA_AVALON_SPI_STATUS_REG                    2
47 #define IOADDR_ALTERA_AVALON_SPI_STATUS(base)           __IO_CALC_ADDRESS_NATIVE(base, ALTERA_AV
48 #define IORD_ALTERA_AVALON_SPI_STATUS(base)             IORD(base, ALTERA_AVALON_SPI_STATUS_REG)
49 #define IOWR_ALTERA_AVALON_SPI_STATUS(base, data)       IOWR(base, ALTERA_AVALON_SPI_STATUS_REG,
50
51 #define ALTERA_AVALON_SPI_STATUS_ROE_MSK                (0x8)
52 #define ALTERA_AVALON_SPI_STATUS_ROE_OFST               (3)
53 #define ALTERA_AVALON_SPI_STATUS_TOE_MSK                (0x10)
```

NIOS SPI

- NIOS SPI System

```
/*
 * nios_spi_1.c
 *
 *  Created on: Oct 22, 2018
 *      Author: johnsontimoj
 */
////////////////////////////////
//
// SPI with NIOS loopback example - no spi_command
//
////////////////////////////////

#include "alt_types.h"
#include "altera_avalon_spi_regs.h"
#include "altera_avalon_spi.h"
#include "system.h"
#include <stdio.h>
#include <unistd.h>// usleep

int main(void){
   printf("Entered Main\n");
   alt_u8 send_M;
   alt_u8 send_S;
   alt_u8 rcvd_S;
   alt_u8 rcvd_M;
   alt_u8 count;
   count = 0;
```

```
   while(1){
      send_M = count;
      send_S = 255 - count;

      // Load Slave TX buffer THEN load Master TX buffer
      // loading master TX causes transmission to start
      //
      IOWR_ALTERA_AVALON_SPI_TXDATA(SPI_SLAVE_BASE, send_S);
      IOWR_ALTERA_AVALON_SPI_TXDATA(SPI_MASTER_BASE, send_M);

      // Wait for transfer to complete
      //
      usleep(75);

      // Read Master and Slave RX buffers
      //
      rcvd_S = IORD_ALTERA_AVALON_SPI_RXDATA(SPI_SLAVE_BASE);
      rcvd_M = IORD_ALTERA_AVALON_SPI_RXDATA(SPI_MASTER_BASE);

      // Print results
      printf("master sent = %i\tslave recv'd = %i\n", send_M, rcvd_S);
      printf("slave sent = %i\tmaster recv'd = %i\n", send_S, rcvd_M);

      // Setup for next loop
      count ++;
      usleep(1000000);
   } // end while

  return 0;
} // end main
```

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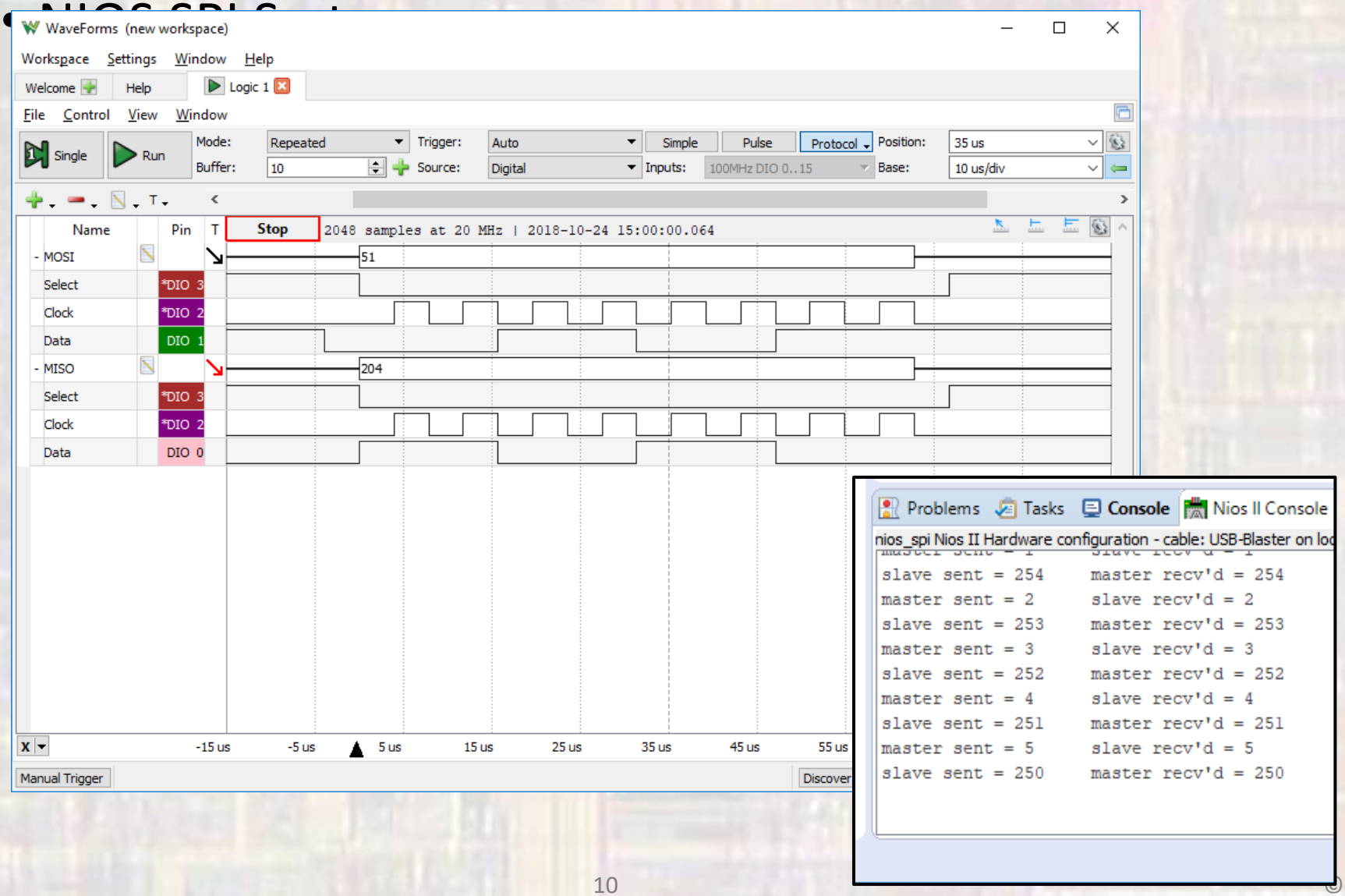
WaveForms (new workspace)
Workspace Settings Window Help
Welcome Help Logic 1
File Control View Window
Single Run
Mode: Repeated
Buffer: 10
Trigger: Auto
Source: Digital
Simple Pulse Protocol
Inputs: 100MHz DIO 0..15
Position: 35 us
Base: 10 us/div
Name Pin T Stop
2048 samples at 20 MHz | 2018-10-24 15:00:00.064
MOSI
Select *DIO 3
Clock *DIO 2
Data DIO 1
MISO
Select *DIO 3
Clock *DIO 2
Data DIO 0
51
204
-15 us -5 us 5 us 15 us 25 us 35 us 45 us 55 us
Manual Trigger
Discover
Problems Tasks Console Nios II Console
nios_spi Nios II Hardware configuration - cable: USB-Blaster on loc
slave sent = 254 master recv'd = 254
master sent = 2 slave recv'd = 2
slave sent = 253 master recv'd = 253
master sent = 3 slave recv'd = 3
slave sent = 252 master recv'd = 252
master sent = 4 slave recv'd = 4
slave sent = 251 master recv'd = 251
master sent = 5 slave recv'd = 5
slave sent = 250 master recv'd = 250