3921
Johnson

Project Report Requirements

Required content:

- Title page
  - Project name
  - Group members
  - "Final Project"
  - "EE3921 – Digital System Design"
  - Date
- Table of Contents
- Problem description (what problem your project is solving and why it is important)
- Problem solution
  - Overview (brief, high-level description of your project)
  - Block diagrams (hardware – DE10_Lite components, Nios II design, etc.)
  - Flow chart(s) (C-code)
  - State diagram/table/ASM chart (VHDL state machine)
  - Description of solution – detailed
  - Testing – description, results
  - Conclusion – summary of project, difficulties encountered and how solved, etc.)
- Appendices
  - VHDL code listing(s) (not wizard generated code)
  - RTL
  - HDL simultions
  - Qsys system content screen capture and any relevant settings
  - C-code listing(s)
  - Quartus compile summary statistics
  - Task list and who did what