EE 3921

Final Project

Dr. Johnson

2 pages

Goals:

This Project is intended to ensure students can develop, document, and present a complex hardware/software system using the Altera FPGA platform and software.

Requirements:

1 to 3 students/team. Team members must contribute equally in the development of the project. In order to receive an A your project must include the use of a NIOS processor, C program, FPGA logic, and 1 on board peripheral.

ABSOLUTELY NO LATE DEMONSTRATIONS OR REPORTS (LATE = 0)

Proposal:

1. Cover sheet
    a. Project name
    b. Course name/number/section
    c. Final project
    d. Date
    e. Names of group members
    f. Group name (optional)
2. Project Idea
    a. Description of problem and proposed solution
    b. Preliminary description of hardware/software components
        i. Description
        ii. Block diagram
        iii. Flow chart
    c. Preliminary workload (tasks) and assignments
    d. Preliminary schedule

Due 8:00 am, Monday morning week 7, via email in pdf format

Demo:

Presented during final lab time – 10min

Must demonstrate that your project functions according to your specification and solves the problem you are addressing
Documentation required at presentation:

- Block diagram(s)
- Flow chart(s)
- VHDL code
- Qsys (screen capture of system contents)
- C-code
- Description of product and user instructions

Report:

Write-up

Your lab write-up should conform to the FORMAL report standard documented in the *Project_Report_Requirements* on the website.

Due Friday of the last week of class, 5:00 pm via email in PDF format. START EARLY! No late checkoffs.