Last updated 8/11/20

These slides describe the use of the SignalTap tool inside of Quartus

Upon completion: You should be able create your own SignalTap environments to debug designs

- Your simulation showed your design works
- but
- Your hardware does not work
 - Review test coverage of simulations
 - Add signals to the design and bring them out to pins to see them
 - Signal Tap

- SignalTap II
 - Embedded Logic Analyzer
 - System-level debugging tool that captures and displays signals



- SignalTap II
 - This modifies our baseline design
 - Potentially impacts timing
 - Potentially impacts implementation
 - Not an issue for our simple designs



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Signal Tap HDL Instance

- SignalTap II
 - Uses on-device memory to store samples
 - Allows high speed data storage
 - Uses up some available memory



6

Signal Tap HDL Instance

- SignalTap II
 - Incremental Flow



- The SignalTap II
 - Simple Example Switches tied to LEDs

Monitor the internal switch signals

© ti



- The SignalTap II
 - Open a SignalTap Logic Analyzer file
 - File → New → SignalTap Logic Analyzer file



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	Signal Tap Logic Analyzer - D:/GDrive/MSC Eile Edit View Project Processing D Eile Edit View Proc	E/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signa Cools Window Help Id JTAG configuration Enabled E Memory: 0 Small: NA ng O cells 0 bits NA	Itap_scomple - [stp1.stp] - X JTAG Chain Configuration: No devices detected Medium: NA L Hardware: - Device: None Detected >> SOF Manager:	X X X Chain
	auto_signaltap_0 Node Type Alias Name Double-click to add nodes	Lock mode: ▲ Allow all changes ▼ Data Enable Trigger Enable Trigger Conditions 0 0 1 ⊠ Basic AND ▼	Signal Configuration: Clock: Data Sample depth: 128 V RAM type: Auto Segmented: 2 64 sample segments Nodes Allocated: Auto Manual: Pipeline Factor. Storage qualifier: Type: Continuous V Input port: Nodes Allocated: Auto Manual: View Manual:	
Acres 12721	ጆ Data 🐺 Setup		۲¢ .	
	Hierarchy Display: X	i Data Log: 强		×
	auto_signaltap_0			
		10	0% 00.0	<u></u>

- The SignalTap II
 - Save the file
 - Click OK when it complains "Input Data and Trigger is empty"
 - Click yes to enable the file





- Under Assignments → Settings → SignalTap Logic ...
 - Check/uncheck enable to enable/disable SignalTap
 - You can change the current SignalTap file

General	Signal Tap Logic Analyzer
Files	Specify compilation options for the Signal Tap Logic Analyzer.
Libraries	
✓ IP Settings	🗹 Enable Signal Tap Logic Analyzer
IP Catalog Search Locations	Signal Tan File name: stn1 stn
Design Templates	spractap richanc. spr.sp
 Operating Settings and Conditions 	
Voltage	
Temperature	
Compilation Dracoss Sottings	

- Select nodes to monitor
 - Double click in the node window

auto_signaltap_0		Lock mode:	💕 Allow all chan	ges 🔹
	Node	Data Enable	Trigger Enable	Trigger Conditions
Type Alias	Name	0	0	1 🗹 Basic AND 🔻

- Expand the top section arrows or right
- Select pre-synthesis under filter
- Make sure your design is listed under Look in

🟸 Node Finder			×
Named: * Options Filter: Signal Tap: pre-synthesis		~	List <
Look in: signaltap_example_de10	\rightarrow	✓ … ✓ Include subentities	Hierarchy view
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Name	Assignments	Name	Assignments
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- Click List
 - All the nodes in your design will be listed

Node Finder						Х
amed: *				~	List	;
Options						
Filter: Signal	Tap: pre-synthesis				 Customize 	
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LEDR[1]	-reg0	Unassigned				
LEDR[2]	-reg0	Unassigned				
LEDR[3]	-reg0	Unassigned	>			
LEDR[4]	-reg0	Unassigned	>>			
LEDR[5]	-reg0	Unassigned	<			
LEDR[6]	-reg0	Unassigned	<<			
LEDR[7]	-reg0	Unassigned				
LEDR[8]	-reg0	Unassigned				
LEDR[9]	-reg0	Unassigned				
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 Expand the SW node and copy them to the right window and then insert

🕫 Node Fii	nder						×
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- 👆 L	EDR[9]~reg0	Unassigned			in	SW[1]	PIN_C11
> 👑 🗉	EDR	Unassigned			in	SW[2]	PIN_D12
🗙 🏲 s	W	Unassigned			in_	SW[3]	PIN_C12
in	- SW[0]	PIN_C10			in_	SW[4]	PIN_A12
in	– SW[1]	PIN_C11		>		SW[5]	PIN_B12
in	– SW[2]	PIN_D12		>>	in_	SW[6]	PIN_A13
in	– SW[3]	PIN_C12		<	in_	SW[7]	PIN_A14
in	– SW[4]	PIN_A12		<<	in_	SW[8]	PIN_B14
in	- SW[5]	PIN_B12			in_	SW[9]	PIN_F15
in	- SW[6]	PIN_A13					
in	– SW[7]	PIN_A14					
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	_ SW[9]	PIN_F15	U				
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- Note the sample depth this is how many data points to keep
- Select "..." beside the clock entry box

nce	s and s	Status	Enabled L	Es: 518	Memory: 1280	Small: 0/0	Medium: 1/182 L	Handware		T	Cabua
auto	o_signaltap_0 N	lot running	5	18 cells	1280 bits	0 blocks	1 blocks 0	Device: None De	tected	- S	can Chain
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-	SW[9]						Туре:	Continuous			-
							Input p	oort:			
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archy	Display:	×□	Data Log: 📴								×
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Copy the CLOCK_50 signal over to the right window

Node Fir	nder					×
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Options						
Filter:	Signal Tap: pre-synthesis					▼ Customize
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8 – L	EDR[9]~reg0	Unassigned				
> 📛 u	EDR	Unassigned				
> 🏲 s	w	Unassigned				
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					O	K Cancel

- Setup the data capture trigger(s)
 - There are a number of simple and complex triggering mechanisms available
 - Select Basic AND in the pull down
 - Right click on the right column of sw0 and select falling edge
 - Right click on the right column of sw1 and select high (1)

auto_signaltap_0			Lock mode:	📫 Allow all chan	ges 🔹	
		Node	Data Enable	Trigger Enable	Trigger Conditions	
Туре	Alias	Name	10	10	1 🗹 Basic AND 🔹	
in —		SW[0]	\checkmark	\checkmark		Trigger on
in		SW[1]	\checkmark	\checkmark	1	ingger on
in		SW[2]	\checkmark	\checkmark		SW(1) high
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in —		SW[4]	\checkmark			AND
in		SW[5]	\checkmark	\checkmark		
in —		SW[6]	\checkmark	\checkmark		SW(0) ↓
in		SW[7]				
in		SW[8]	\checkmark	\checkmark		
in		SW[9]				

- Connect the DE10 Board
 - Select Setup in the upper right hand corner of the SignalTap window
 - Select the USB-Blaster
 - Save

ım: 1/182	× Li	JTAG Chai Hardware:	n Configuration:	JTAG ready B-0]	Setup
ks	0	Device:	@1: 10M50DA(. Manager:	ES)/10M50DC ▼	Scan Chain
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Hardware Setup							
Hardware Settings	JTAG S	ettings					
Select a programmin hardware setup appli	ig hardwa ies only to	re setup the curr	to use wher ent progran	n programming nmer window.	devices. T	This programming	
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Hardware USB-Blaster			Server Local	Port USB-0		Add Hardware Remove Hardware	2
						Clos	e

- Recompile
 - In the main Quartus window compile your design
 - You will see the SignalTap modules along with your own design

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-									

Program the board

Review resources

Flow Summary 7

<<Filter>>

Flow Status

Ouartus Prime Version

Revision Name

Top-level Entity Name

Family

Device

Timing Models

Total logic elements

Total registers

Total pins

Total virtual pins

Total memory bits

Embedded Multiplier 9-bit elements

Total PLLs

UFM blocks

ADC blocks



Our design has 10 registers and 21 pins – everything else is part of SignalTap

≻

Successful - Sat Aug 18 16:00:39 2018

signaltap_example

10M50DAF484C7G

650 / 49,760 (1%)

1,280 (< 1 %)

21 360 (6%)

0/288(0%)

0/4(0%)

0/1(0%)

0/2(0%)

MAX 10

Final

- Verify your design
 - Each switch is coupled to an LED via a register clocked at 50MHZ
 - Toggle the switches and see the LEDs turn on and off
 - It appears instantaneous due to the clock speed

- Start the analysis
 - Reset the switches to 0's
 - In the SignalTap window select Processing → Run Analysis

🤊 Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp1.stp]* – 🛛 🗙												
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E	✓ → signaltap_example_de10											

No trigger condition met yet

- Start the analysis
 - Toggle some switches nothing should happen in SignalTap
 - Set SW(1) to '1' and toggle SW(0) from '1' to '0'

* Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp1.stp]* -									\times
<u>File Edit View Project Processing Tools Window Help</u>								com	6
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auto_signaltap_0 Not running	☑ 518 cells	1280 bits	0 blocks	1 blocks	0	Device: @1: 10M50DA(. ES)/1	10M50DC -	Scan Ch	iain
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- Example 2
 - Mod10 Counter with LED outputs
 - Running at full speed impossible to see on LEDs

signalt	tap_example	2_de10.vhdl
by: joł	nnsontimoj	
created	d: 8/18/18	
version	n: 0.0	
 Mod 10 	up counter	
library iee use ieee.st	ee; td_logic_11	.64.all;
entity sign	naltap_exam	ple2_de10 is
	LOCK_50 : N : EDR :	IN STD_LOGIC; IN STD_LOGIC_VECTOR(9 DOWNTO 0) OUT STD_LOGIC_VECTOR(9 DOWNTO 0)
end entity;	;	



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Image: Setup Hierarchy Display: X Data Log: X	Nodes Allocated: @ Auto O Manual: 6 Pipeline Factor: 0 Storage qualifie:: Type::::::::::::::::::::::::::::::::::::	LEDR[4]			ノ	Segme	anted. 2 04 sample segments	
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• Compile, Program and Run Analysis

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Instance Man	nager: 🍳 👂 🔳	Ready to acc	quire					×	JTAG Chain Configuration: JTAG ready X			
Instance		Status	Enabled	LEs: 472	Memory: 768	Small: 0/0	Medium: 1/182	2 L	Hardware: USB-Blaster [USB-0]			
🔝 auto_s	signaltap_0	Not running		472 cells	768 bits	0 blocks	1 blocks	0				
									Device: @1: 10M50DA(. ES)/10M50DC			
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log: Trig @) 2018/08/20 11:42:14	(0:0:6.1 elapsed)		click to insert time bar								
Type Alias	s Nar	ne	<u>16</u> 8			32 40	, 48 	56				
	LEDR[0]											
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*	LEDR[3]		_									
	LEDR[4]											
*	LEDR[5]											
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• Review resources

Flow Summary		and the second se				
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Flow Status	Successful - Fri Se	ep 28 09:23:41 2018				
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Lite Edition					
Revision Name	signaltap_example					
Top-level Entity Name	signaltap_example	e2_de10				
Family	MAX 10					
Device	10M50DAF484C7					
Timing Models	Final	Our design has 4 registers, a little logic				
Total logic elements	588/49,760 (1 %	and 21 pins – everything else is part				
Total registers	437	of Cignal Tan				
Total pins	21/360(6%)	of Signal lap				
Total virtual pins	0					
Total memory bits	768 / ,677,312 (< 1 %)				
Embedded Multiplier 9-bit elements	0/288(0%)					
Total PLLs	0/4(0%)					
UFM blocks	0/1(0%)					
ADC blocks	0/2(0%)					