SPI Review

Last updated 6/15/20

SPI Review

These slides review the operation the Serial Peripheral Interface (SPI)

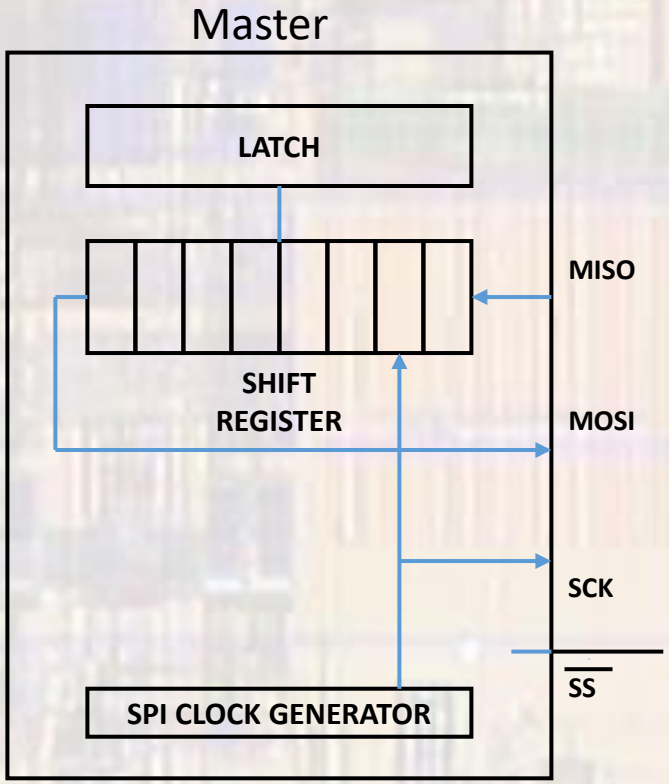
Upon completion: You should be able to describe the operation of a SPI and interpret signals

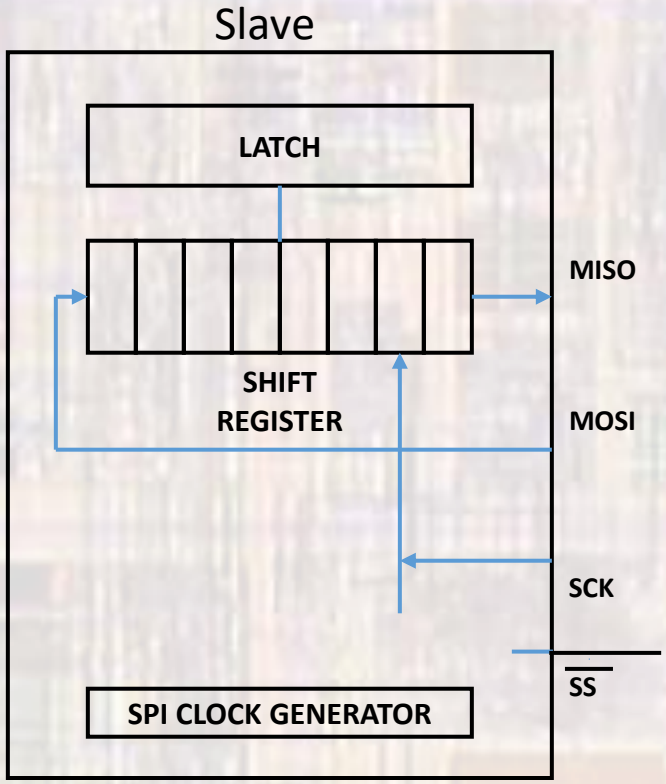
SPI Review

- Overview
  - 8 bit synchronous shift register used to communicate externally
  - Most often used to communicate with peripherals
    - displays, sensors, converters
  - Can be used for inter-processor communication
  - Two modes of operation
    - Master – responsible for providing the clock
    - Slave – receives clock from the master

SPI Review

- Overview





MISO – Master:IN or Slave:OUT

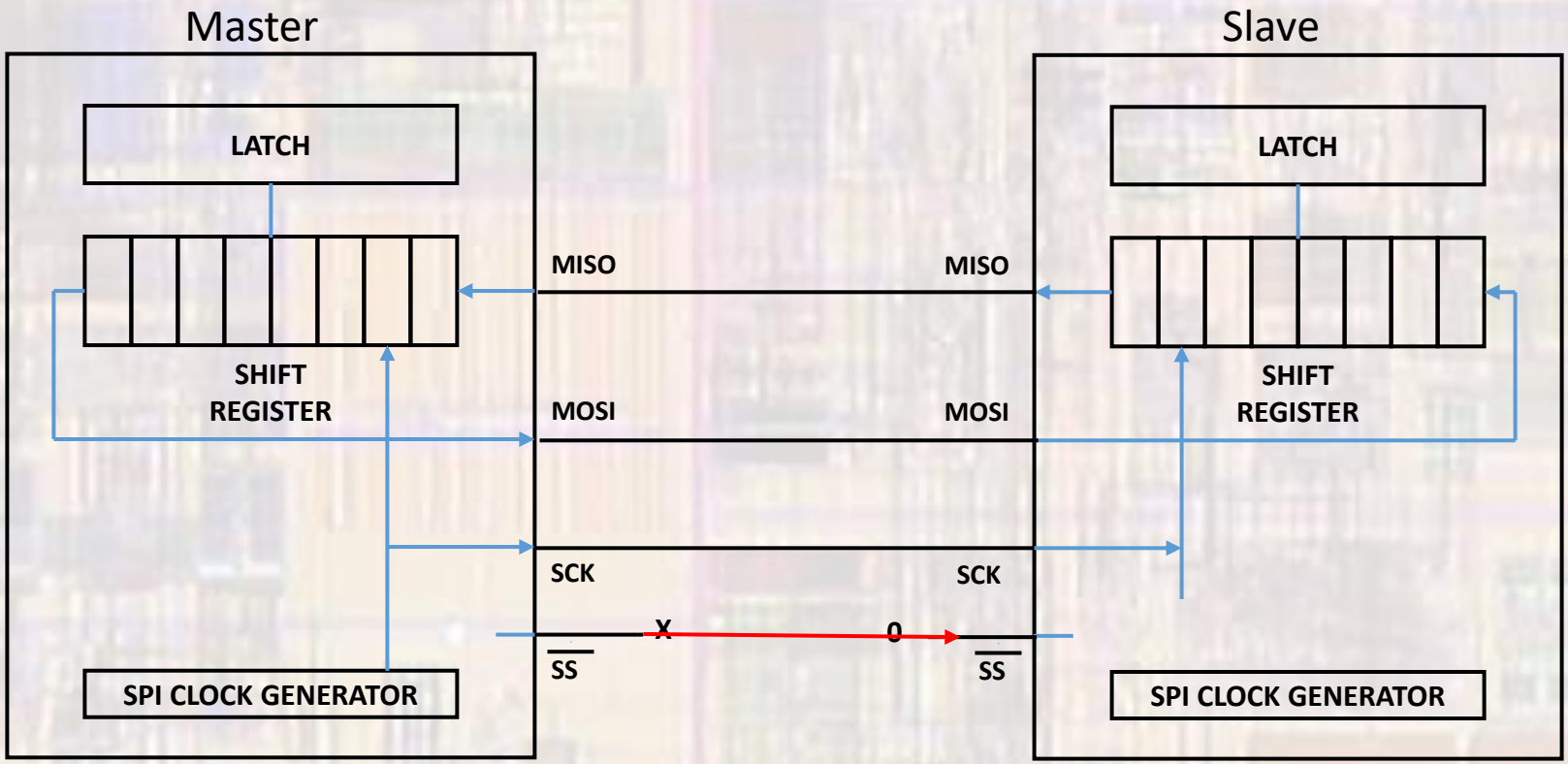
MOSI – Master:OUT or Slave:IN

SCK – SPI CLK

$\overline{SS}$ – Slave Select Bar

SPI Review

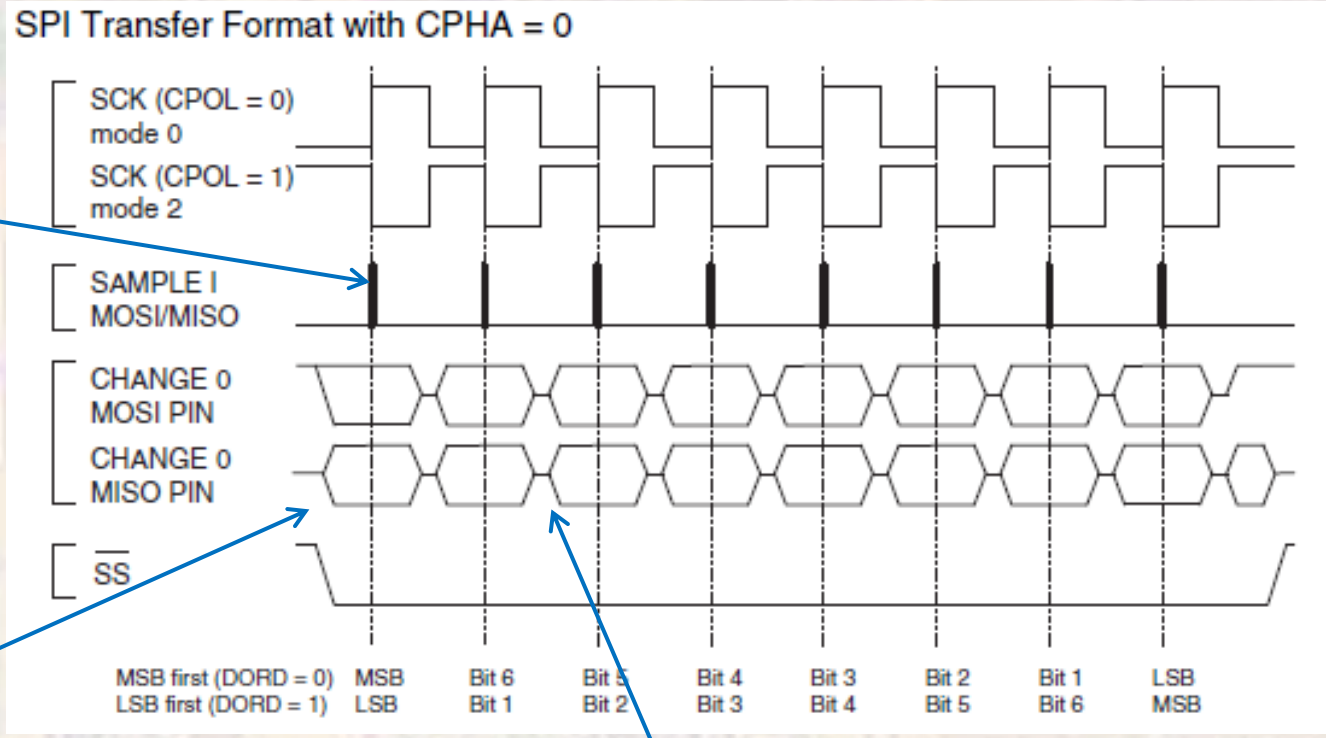
- Operation



Latch → Shift Register in both master and slave
Master generates 8 clocks → shifts both registers (swaps content)
Shift Register → Latch in both master and slave

SPI Review

- Operation
  - CPHA = 0



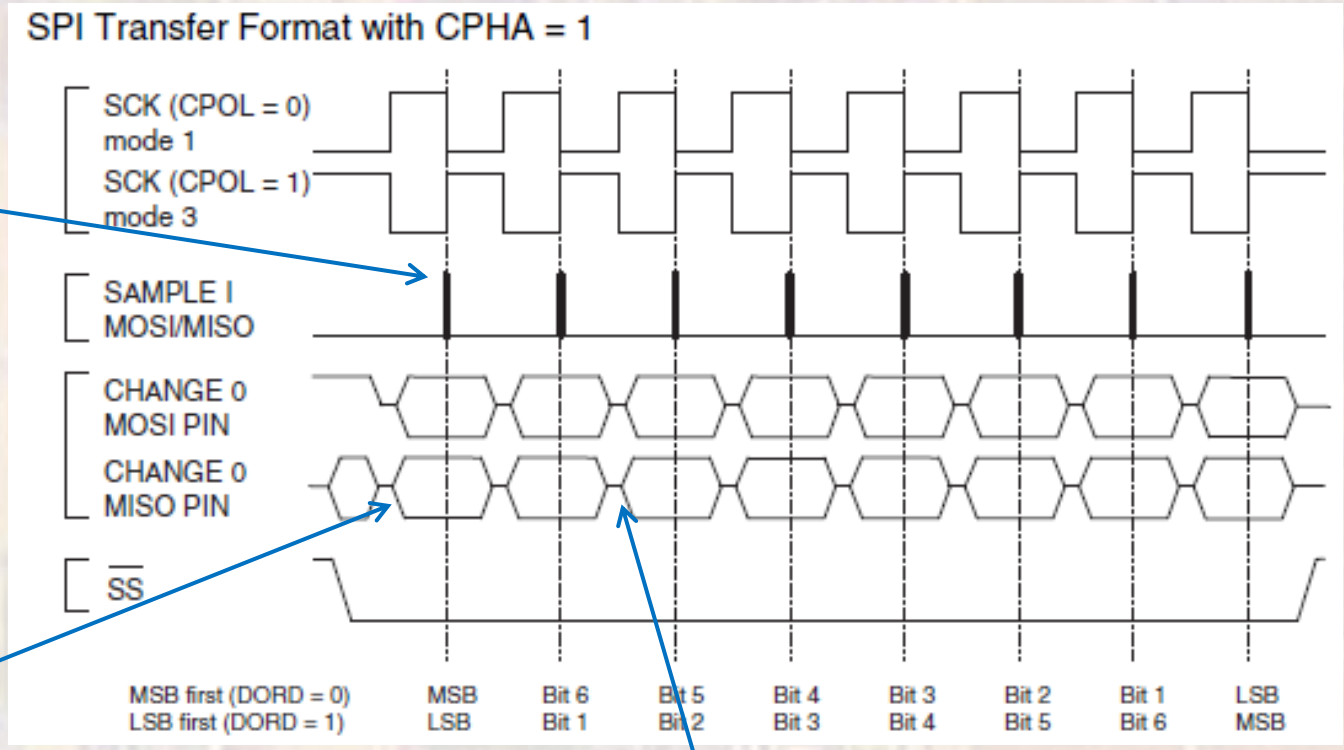
Captured in register on leading clock edge

Values active on pins as soon as SSbar goes low

New values placed on pins on trailing clock edge

SPI Review

- Operation
  - CPHA = 1



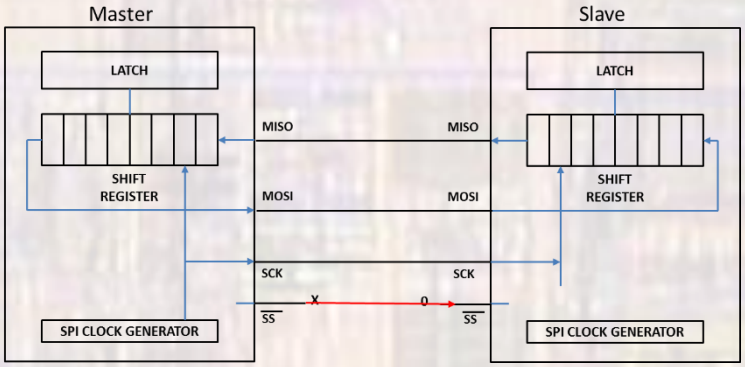
Captured in register on trailing clock edge

Values active on pins on first clock edge

New values placed on pins on leading clock edge

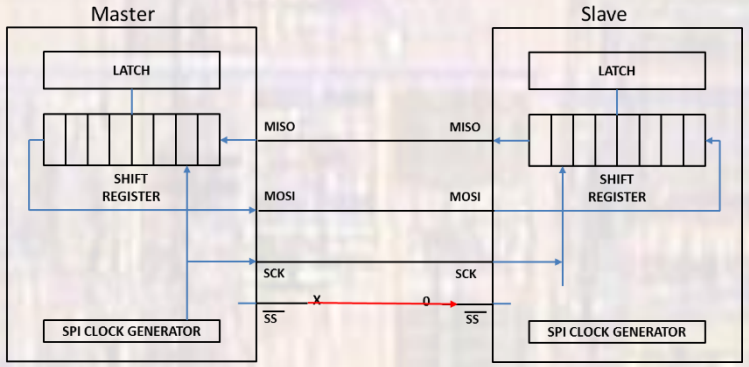
SPI Review

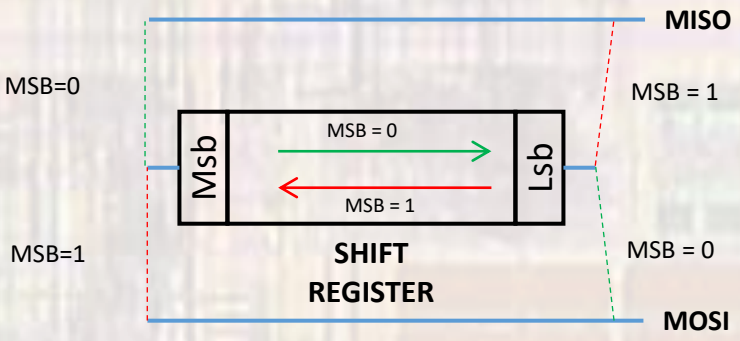
- Operation
  - Configure 1 device as master
  - Configure 1 or more devices as slaves
  - Load values into register(s)
  - Pull SSbar low on the desired slave device
  - Initiate transfer by writing to the data register
    - The master will generate the appropriate clocks
  - If interrupts are enabled – an interrupt will be generated on completion



SPI Review

- Operation
  - 2 options for clock polarity
    - CKPL = 0 → rising edge triggered
    - CKPL = 1 → falling edge triggered
  - 2 options for clock phase
    - CKPH = 0 → leading edge triggered
    - CKPH = 1 → trailing edge triggered
  - 2 options on transfer direction
    - MSB = 0 → LSB transferred first
    - MSB = 1 → MSB transferred first





SPI Review

- Operation
  - Multiple Slave Configuration

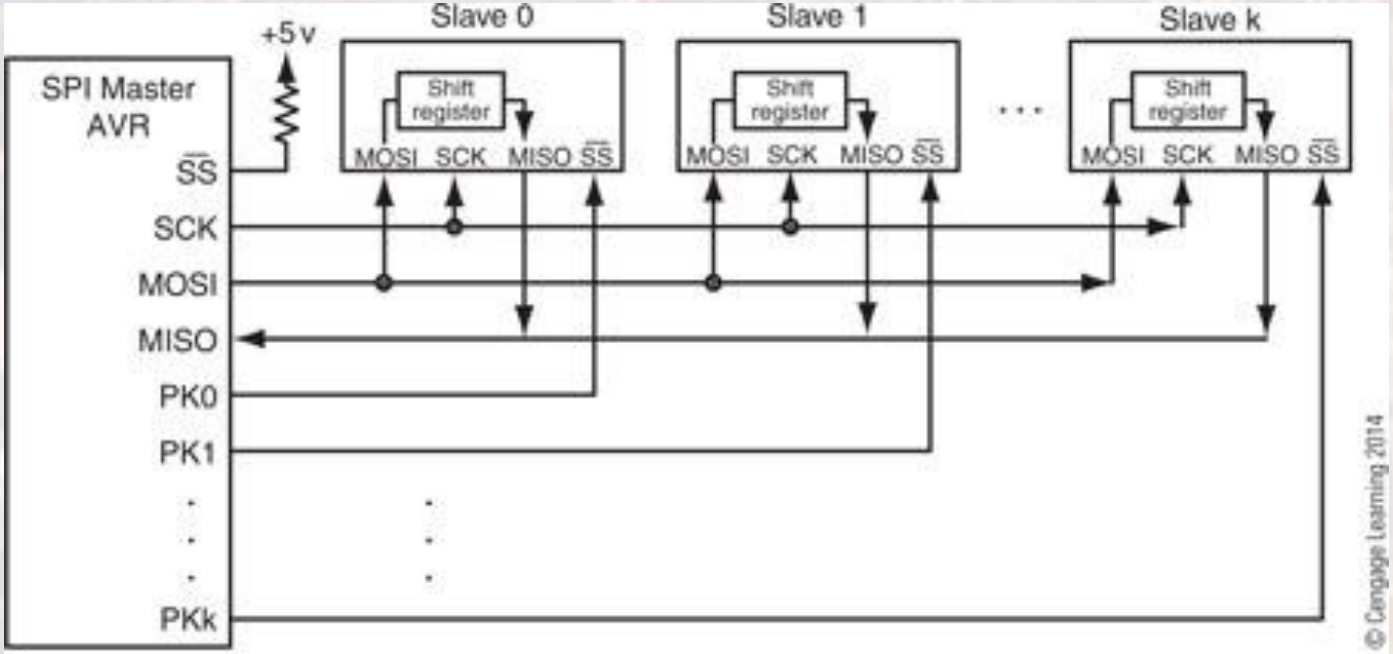


Figure 14.7 ■ Single-master and multiple-slave device connection (method 1)

SPI Review

- Operation
  - Multiple Slave – Extended Shift Configuration

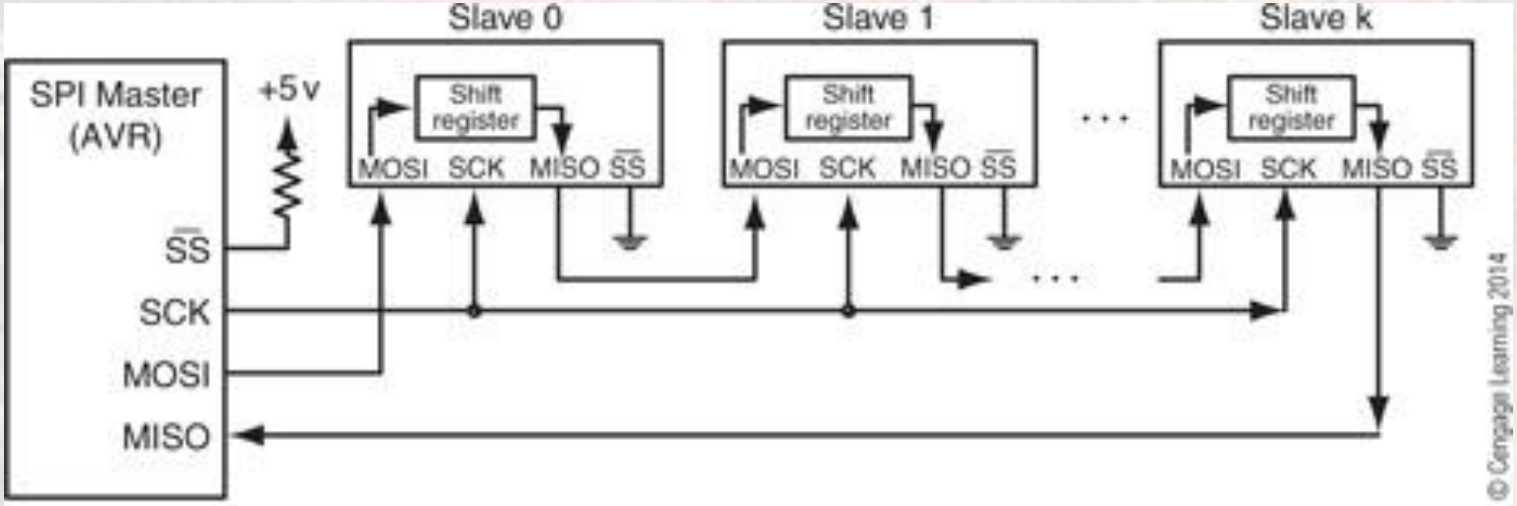


Figure 14.8 ■ Single-master and multiple-slave device connection (method 2)