

# CMOS – Chip Level

Last updated 2/25/21

A faded, light-colored image of a CMOS chip layout is visible in the background of the lower half of the slide. It shows a complex grid of lines and rectangular blocks, representing the intricate circuitry of a microchip.

# CMOS – Chip Level

- Millions to hundreds of millions of gates
  - Physical Space
  - Sheer numbers of gates
  - Keeping shared resources close to multiple users (memory)
  - I/O pin access and placement
- Interconnect – getting all the wires connected
  - Typical processes have 6 – 10 layers of interconnect
  - Cell, local, global, power
- Performance
- Power / Heat Dissipation

# CMOS – Chip Level

- Performance Drivers
  - Process Technology
    - Transistor performance
    - Short channel vs. long channel devices
    - High Vt and Low Vt devices
  - Clock Frequency
    - Maximum is set by the longest unit delay
    - Very complex timing tools used to ensure max frequency
  - Interconnect
    - RC delays
    - Capacitive coupling

# CMOS – Chip Level

- Power Drivers
  - Process Technology - Dynamic, Static, Short circuit ( D/S/SC )
  - Number of gates – D/S/SC
  - Clock Frequency – D/SC
    - Dynamic power becomes  $CV^2f$ , where  $f$  is clock frequency
    - Short circuit power is also multiplied by  $f$
  - Supply Voltage – D/S/SC
  - Routing Efficiency – D/SC
    - Minimizing capacitance is critical

# CMOS – Chip Level

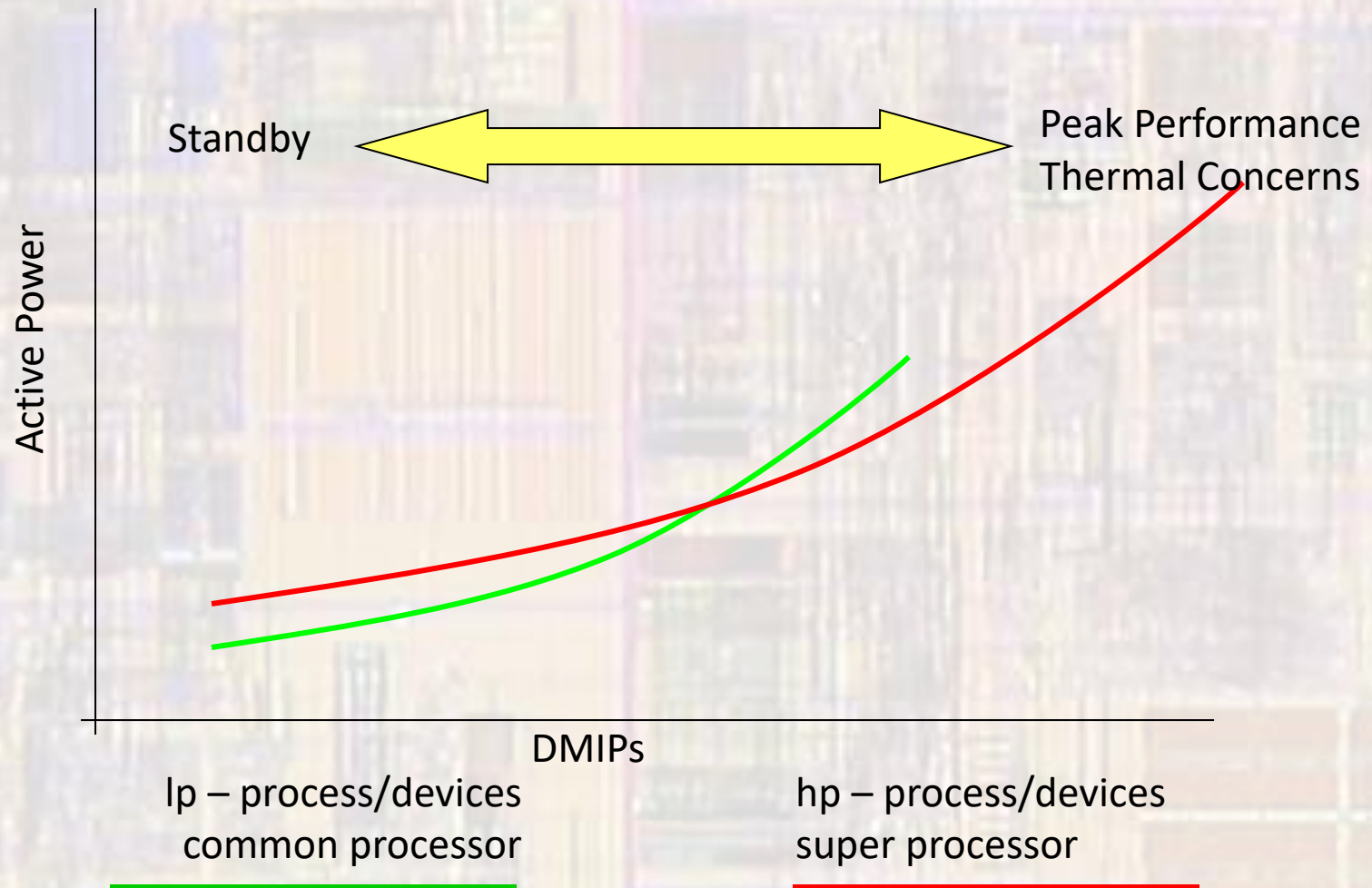
- Power / Performance Balance
  - Device Level Solutions
    - Multiple  $T_{ox}$  ( $V_T$ ) devices
      - Thin  $T_{ox}$  devices for high performance paths
      - Thick  $T_{ox}$  devices
        - Lower leakage
        - Higher voltages
  - Chip Level Solutions
    - Reduced interconnect R and C
    - Power islands – gating the power to circuits not in use
    - Clock Gating (module level)
      - Turn off the clocks to circuits not in use
      - Requires synchronization

# CMOS – Chip Level

- Power / Performance Balance
  - System Level Solutions
    - Dynamic Voltage Scaling – changing VDD as needed
    - Dynamic Frequency Scaling – changing the clock frequency as needed
    - Together these are referred to as DVFS
  - Architectural Solutions
    - Pipelining
    - Multi-core processors
      - Homogeneous – dual/quad core
      - Heterogeneous – big/little/GPU
    - Memory Hierarchy

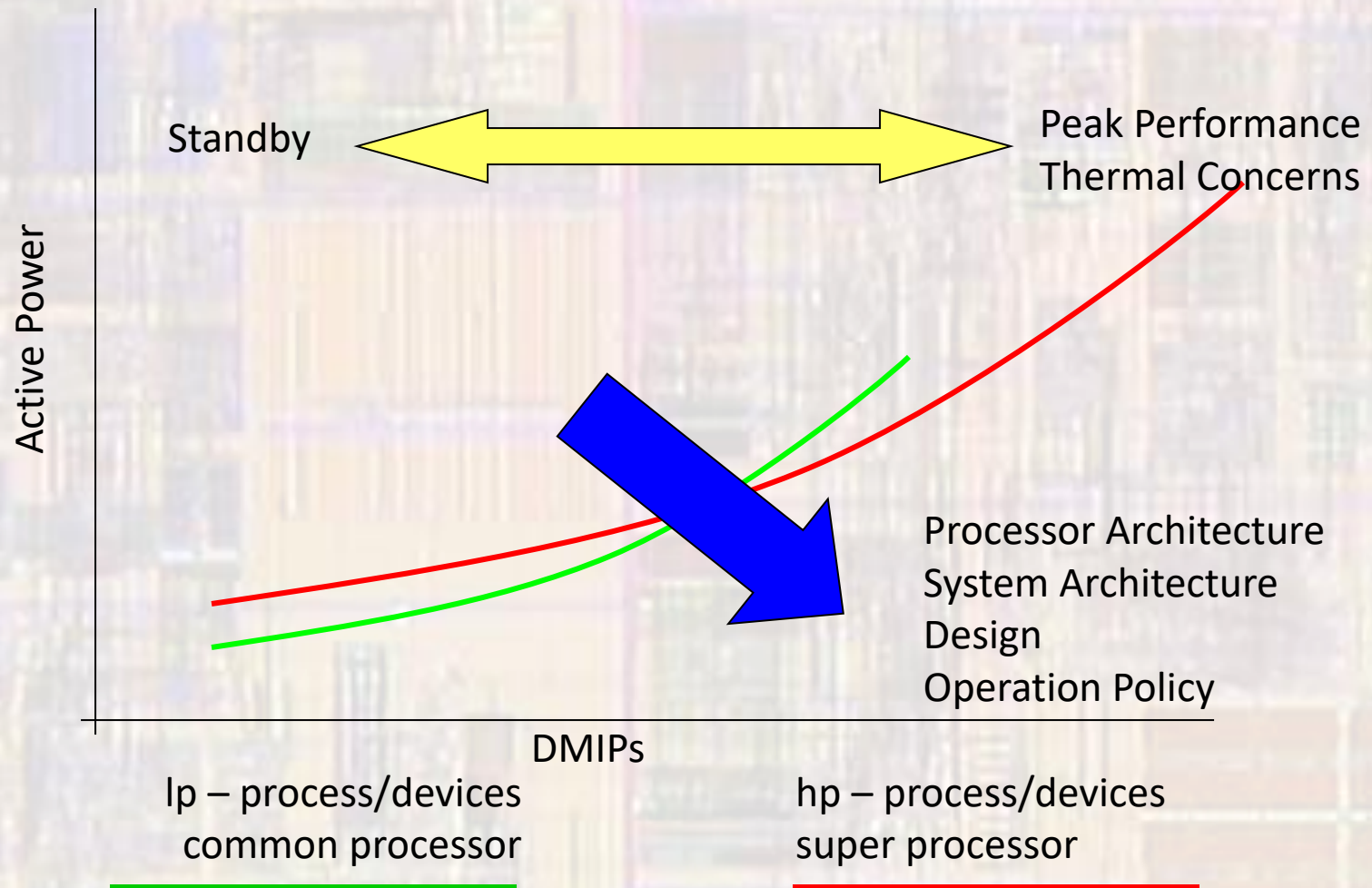
# CMOS – Chip Level

- Power – Performance Tradeoffs



# CMOS – Chip Level

- Power – Performance Tradeoffs

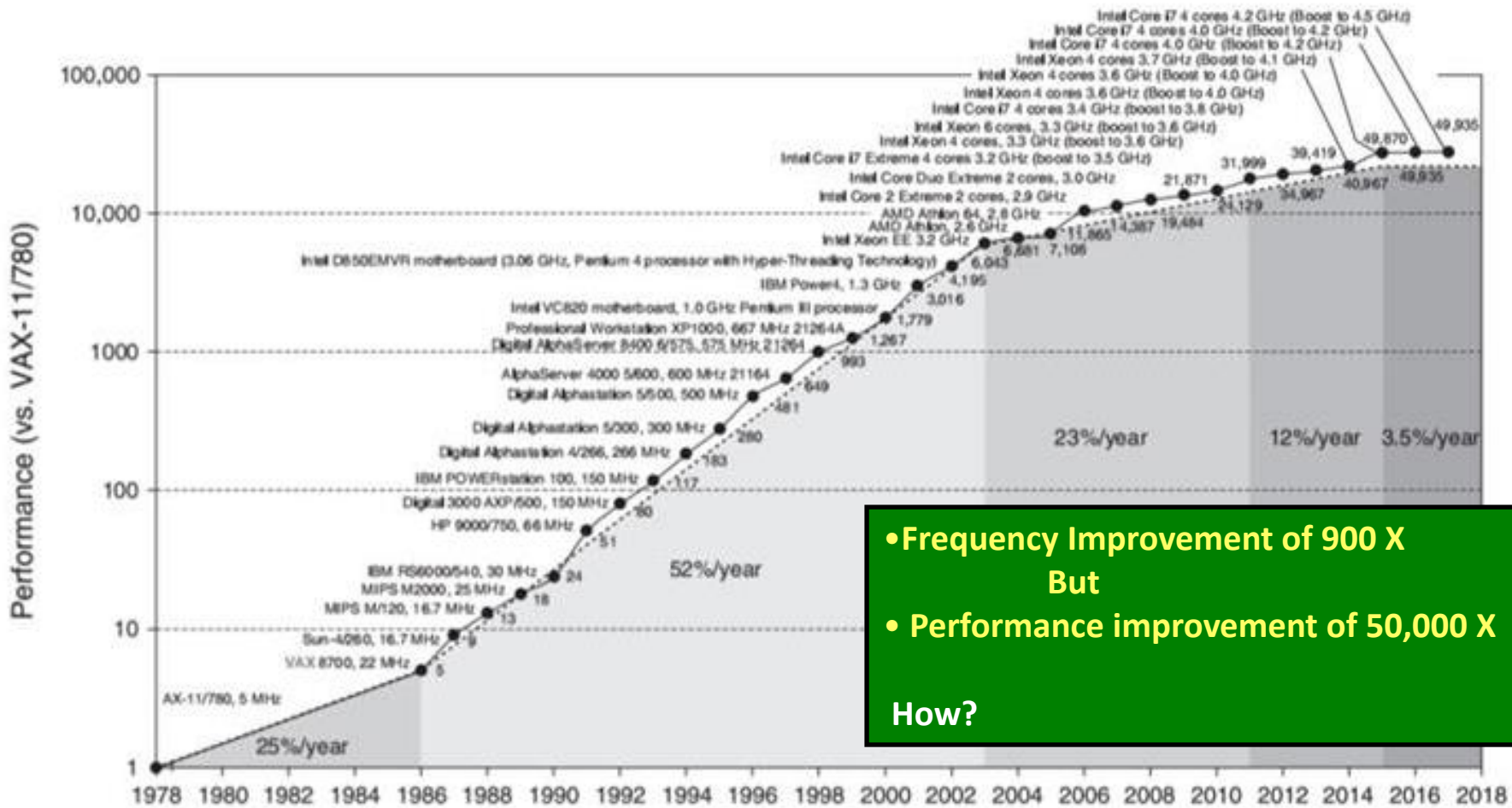




# Technology

- Processor Performance

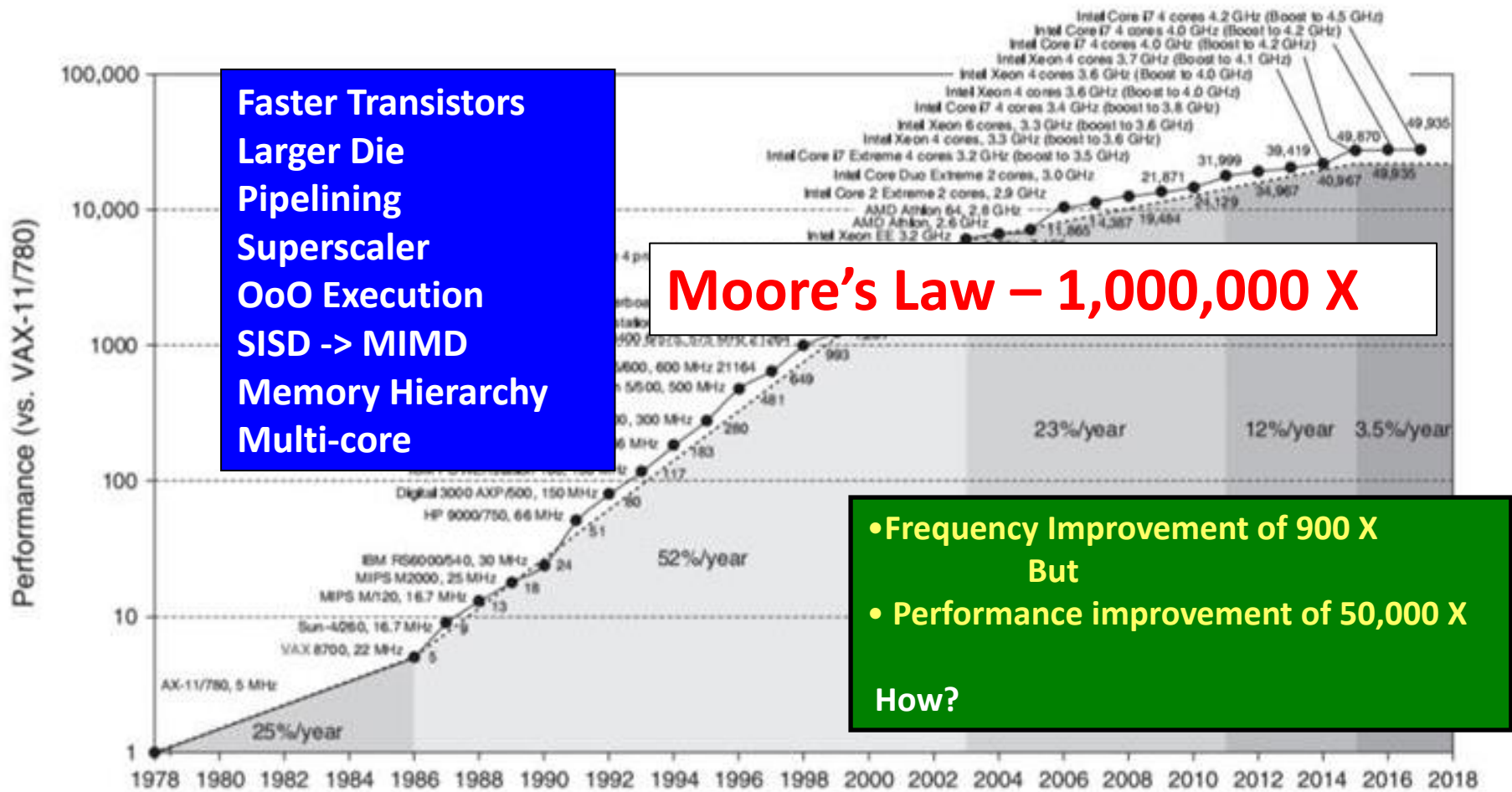
IEEE IRDS



• Frequency Improvement of 900 X  
 But  
 • Performance improvement of 50,000 X  
 How?

# CMOS – Chip Level

- Processor Performance



Source: Computer Architecture, Hennessy and Patterson, 2017 Elsevier Inc

# CMOS – Chip Level

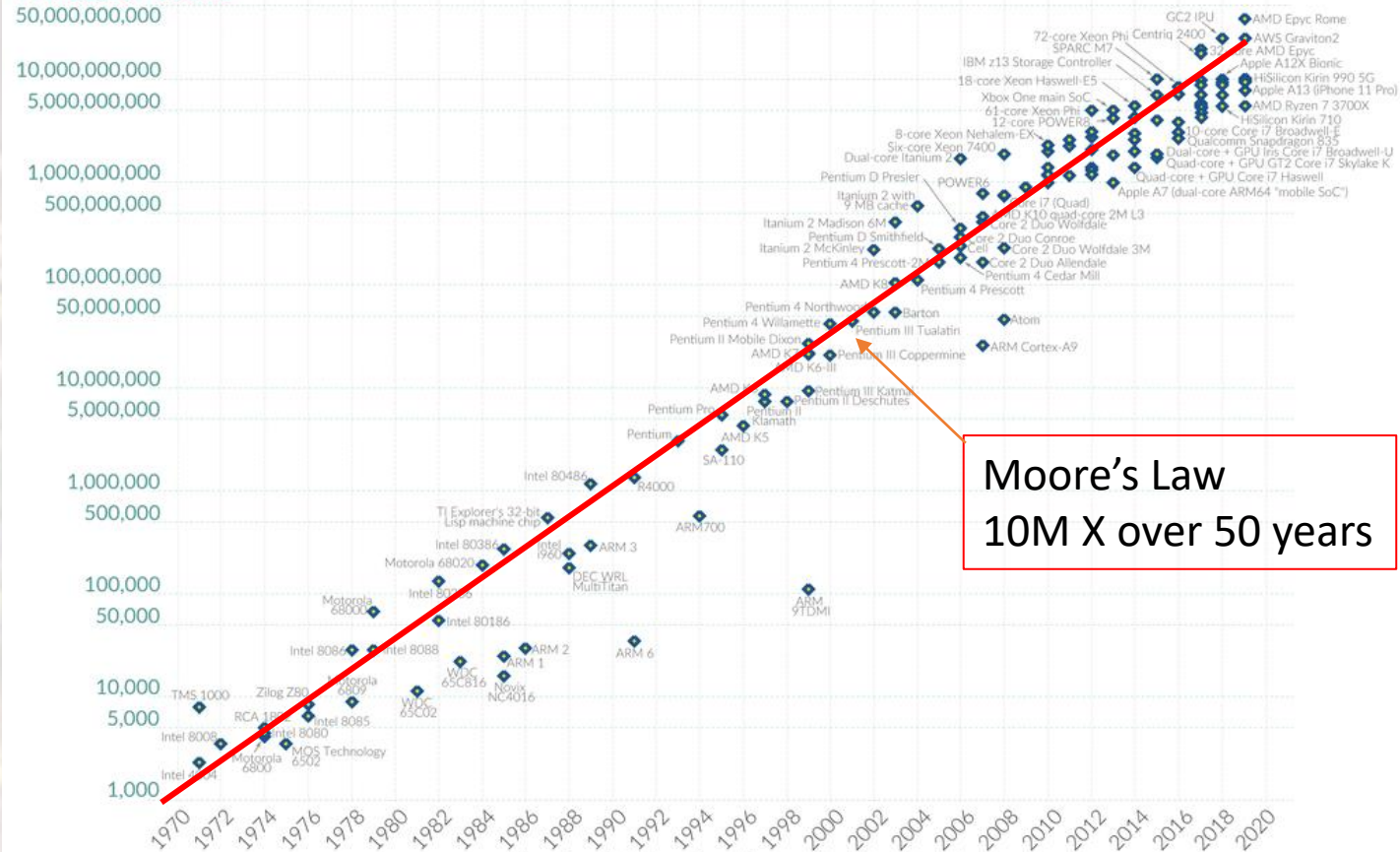
- Transistors per chip

## Moore's Law: The number of transistors on microchips doubles every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

Our World  
in Data

### Transistor count



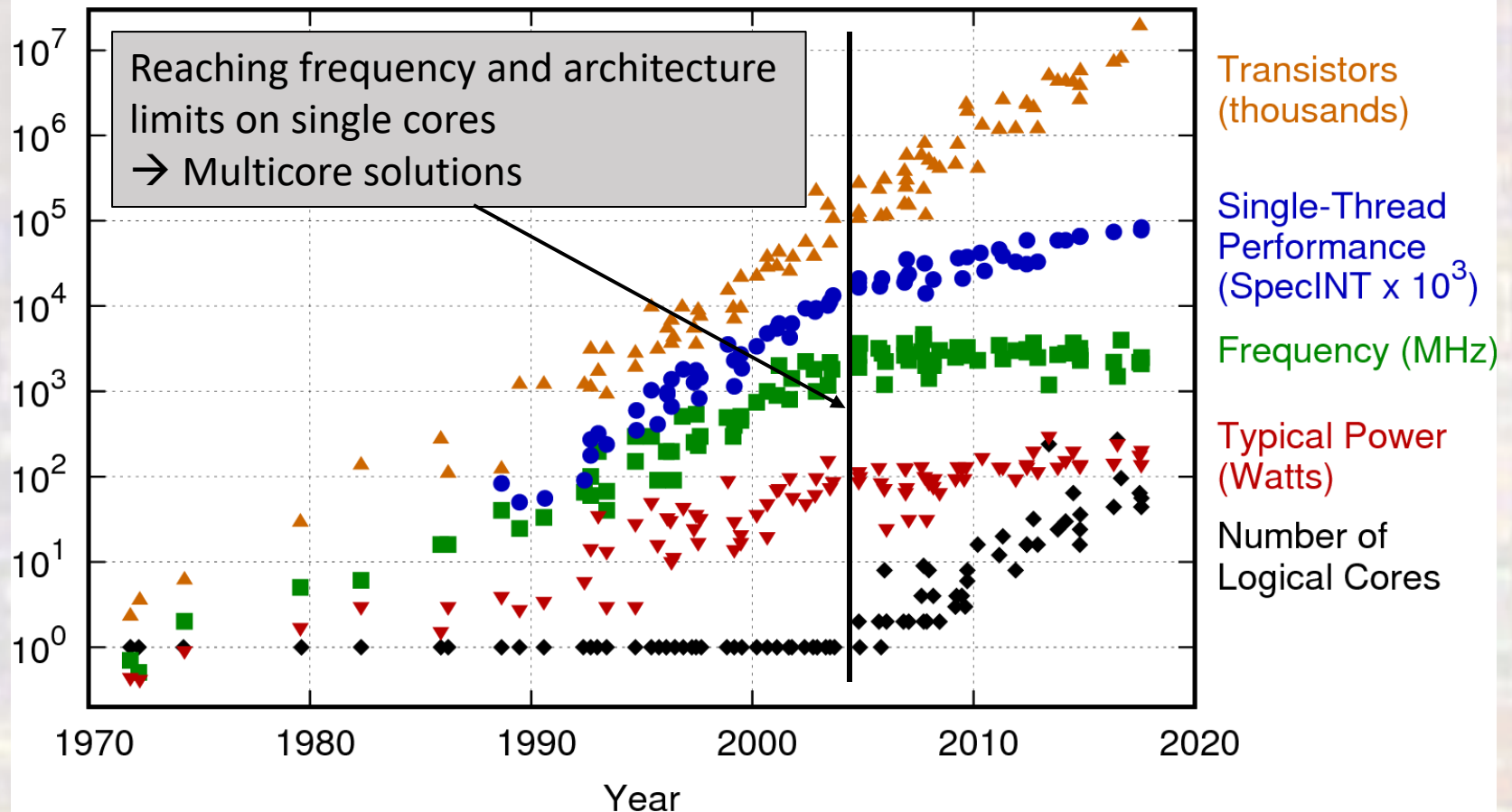
Moore's Law  
10M X over 50 years

Data source: Wikipedia (wikipedia.org/wiki/Transistor\_count)  
OurWorldinData.org – Research and data to make progress against the world's largest problems.  
Licensed under CC-BY by the authors Hannah Ritchie and Max Roser.

# CMOS – Chip Level

- SPECint Performance – single CPU

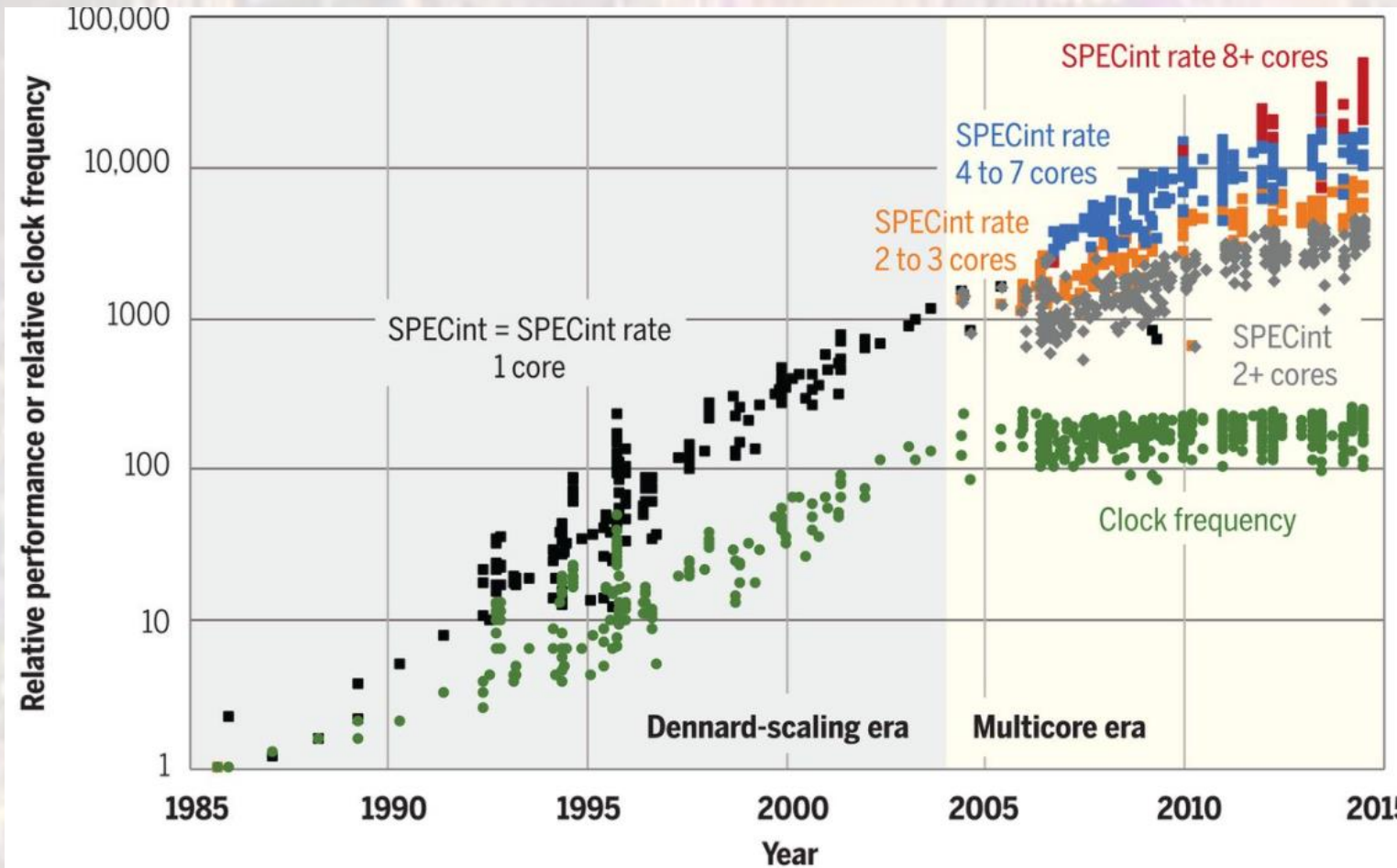
42 Years of Microprocessor Trend Data



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten  
New plot and data collected for 2010-2017 by K. Rupp

# CMOS – Chip Level

- SPECint Performance – Including multi-core



src: Science Magazine – June 2020

# CMOS – Chip Level

- What about Cost \$\$\$



The minimum gate pitch of Intel's 10 nm process shrinks from 70 nm to 54 nm and the minimum metal pitch shrinks from 52 nm to 36 nm. These smaller dimensions enable a logic transistor density of 100.8 mega transistors per mm<sup>2</sup>, which is 2.7x higher than Intel's previous 14 nm technology and is approximately 2x higher than other industry 10 nm technologies.

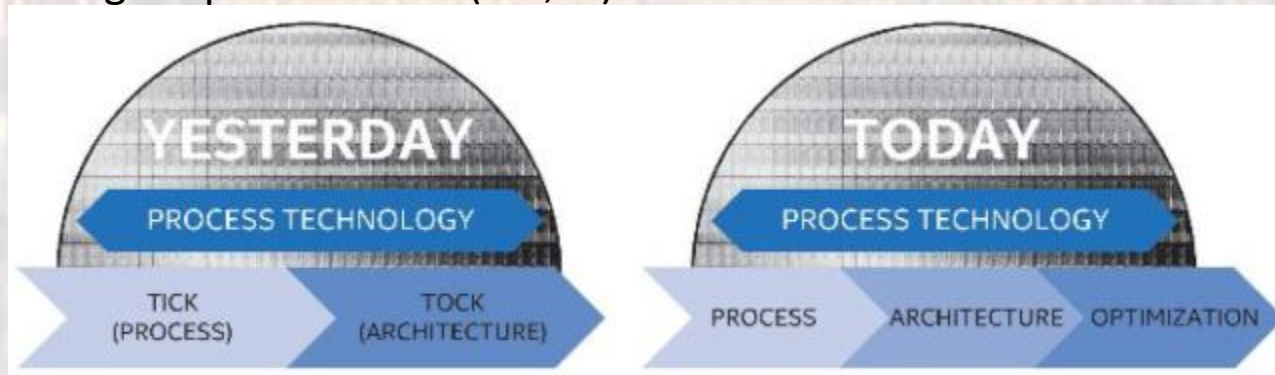
src: Intel

# CMOS – Chip Level

- Design Processes

- Tick-Tock

- 2 year technology cycle
    - Tick - Existing processor design migrated to a new technology node
      - Higher speeds
      - Better power characteristics
    - Tock – New processor design introduced on an existing technology node
      - New features
      - Higher performance (IPC, ...)



# CMOS – Chip Level

- Design Processes

- 3 Phase

- 3 year technology cycle

- Process

- Slight modifications to existing architecture on a new technology node

- Architecture

- New architecture on the technology node

- Optimization

- Optimized architecture on the technology node

