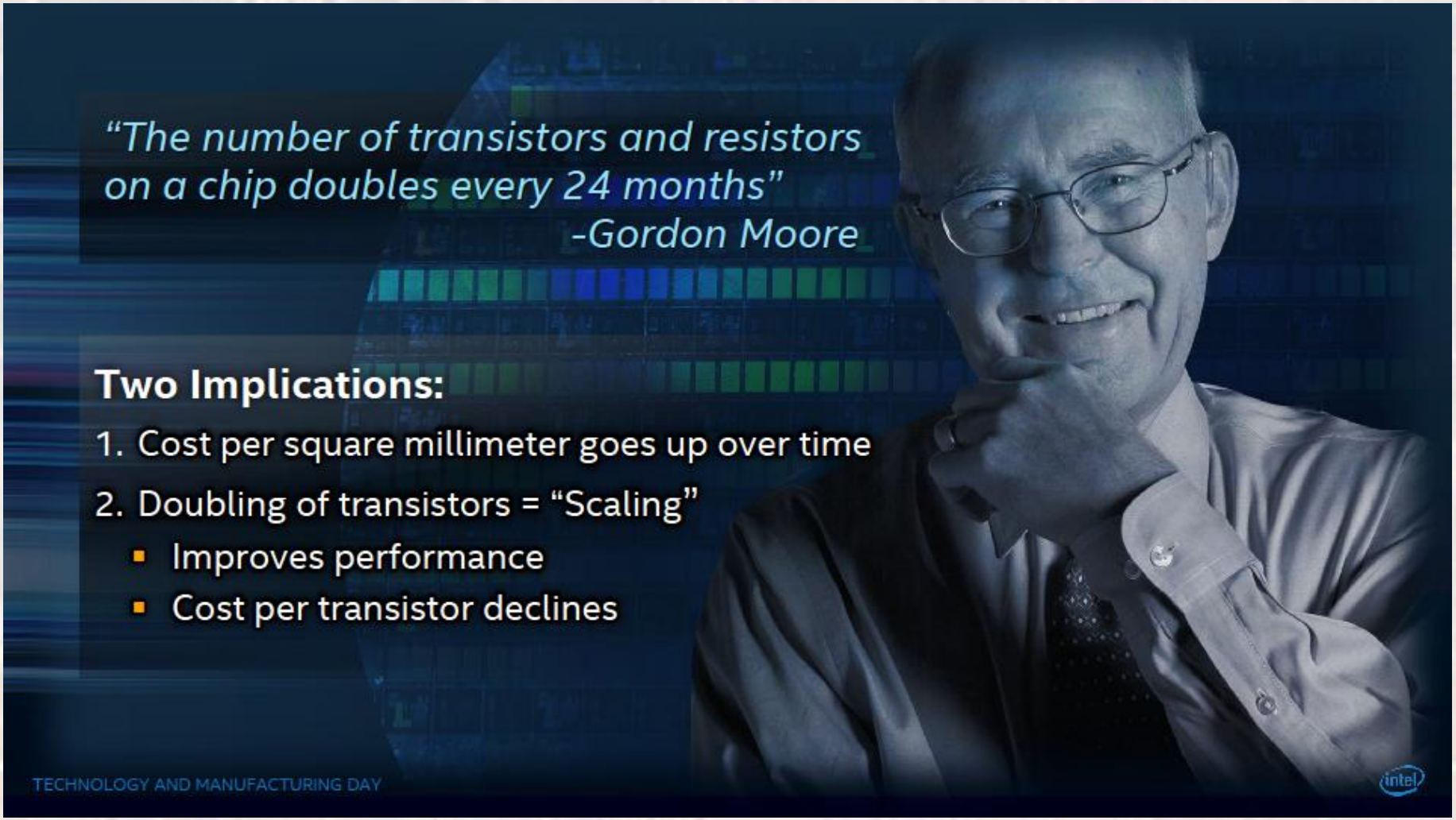
CMOS Cost

Last updated 2/25/21

CMOS Cost

- Semiconductor Technology



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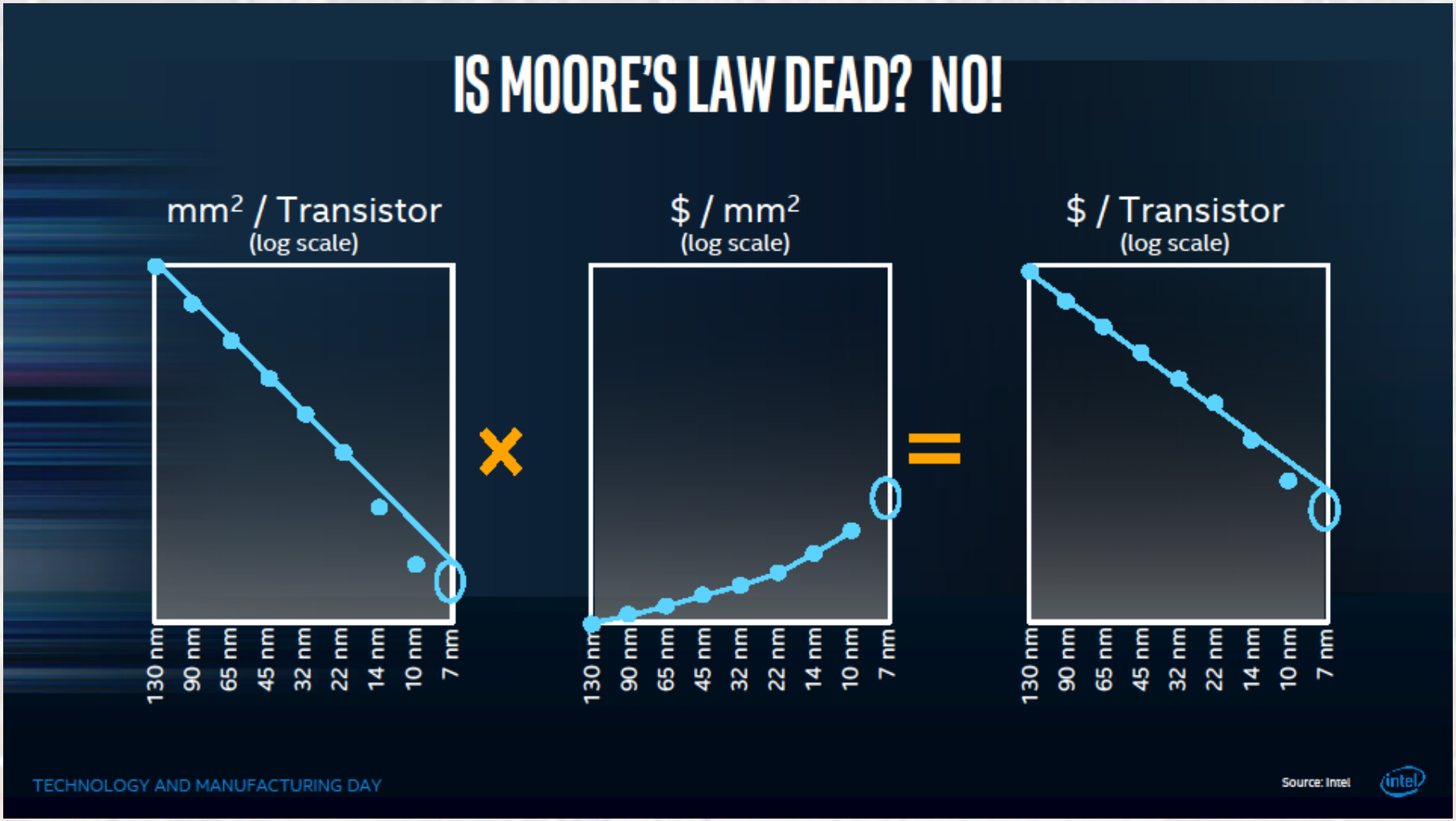
- Semiconductor Technology



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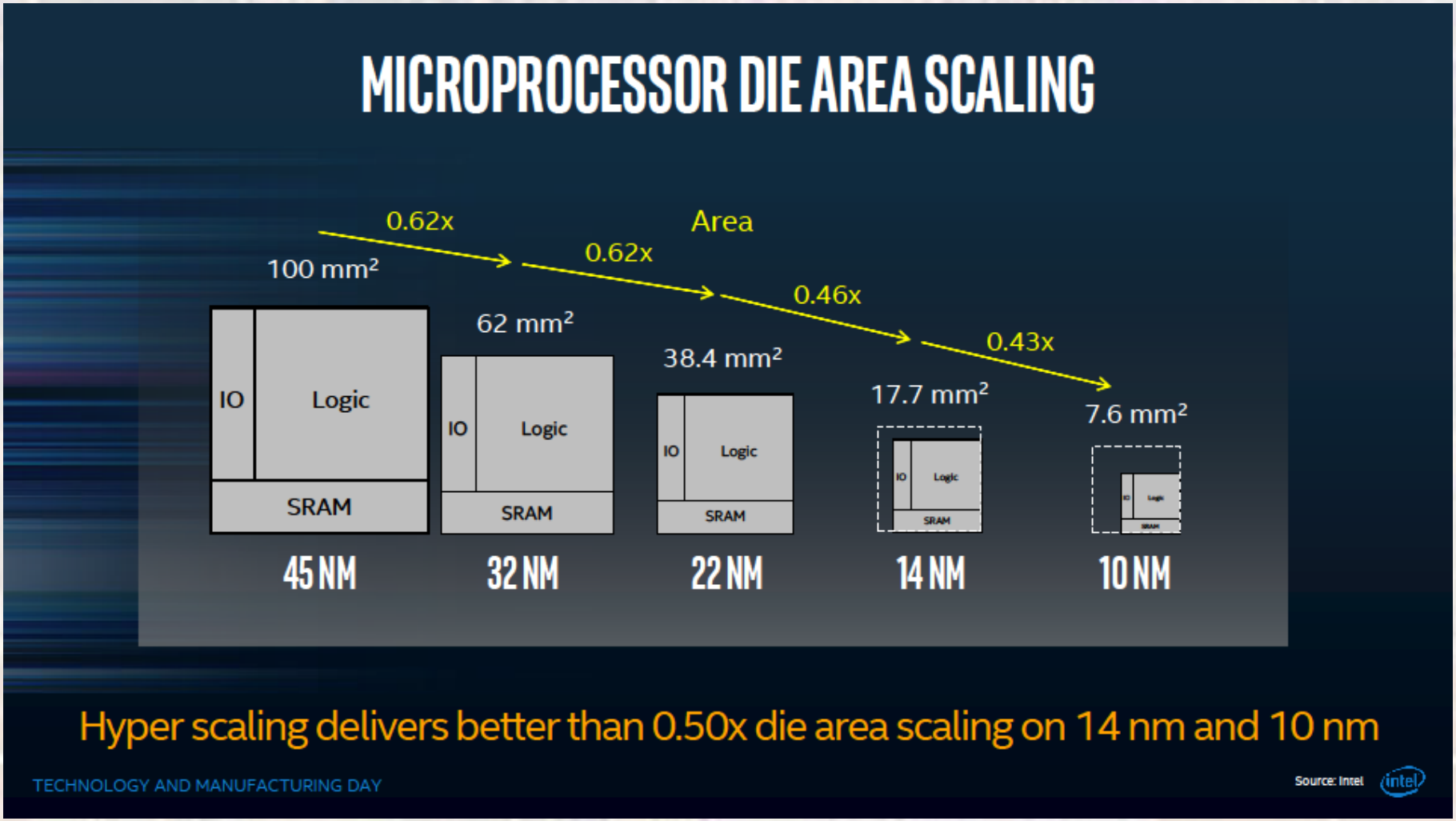

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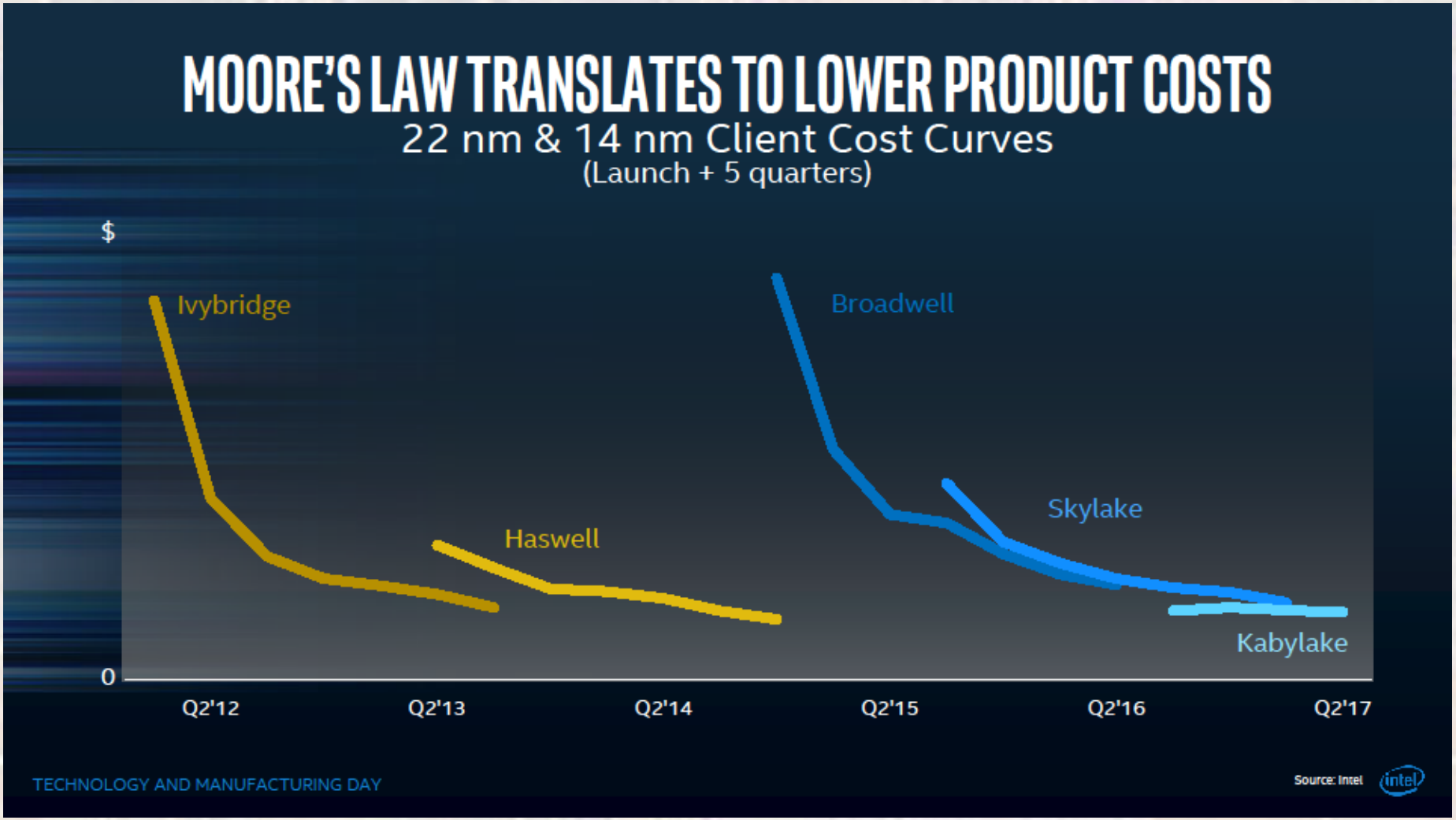
- Semiconductor Technology



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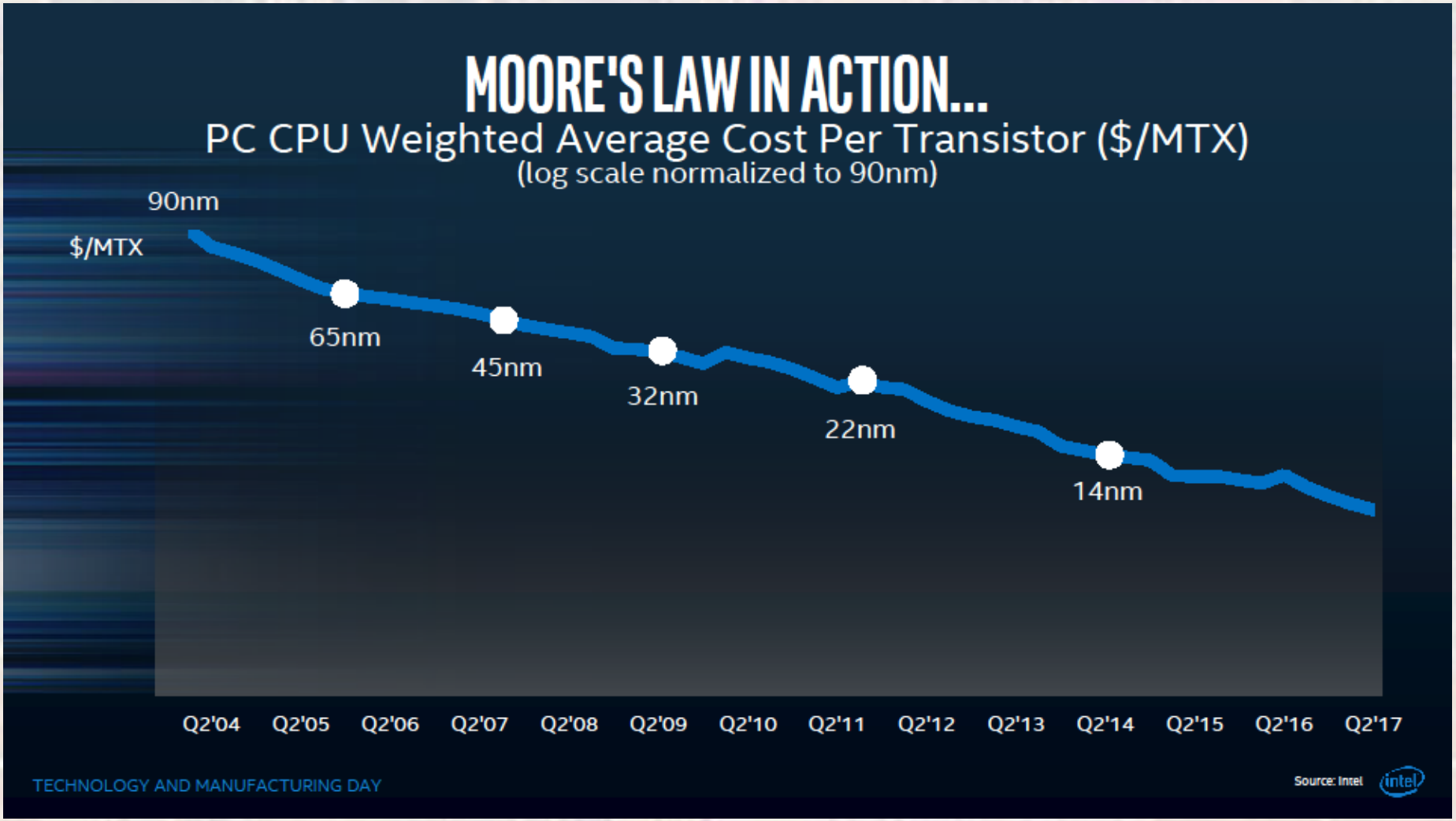
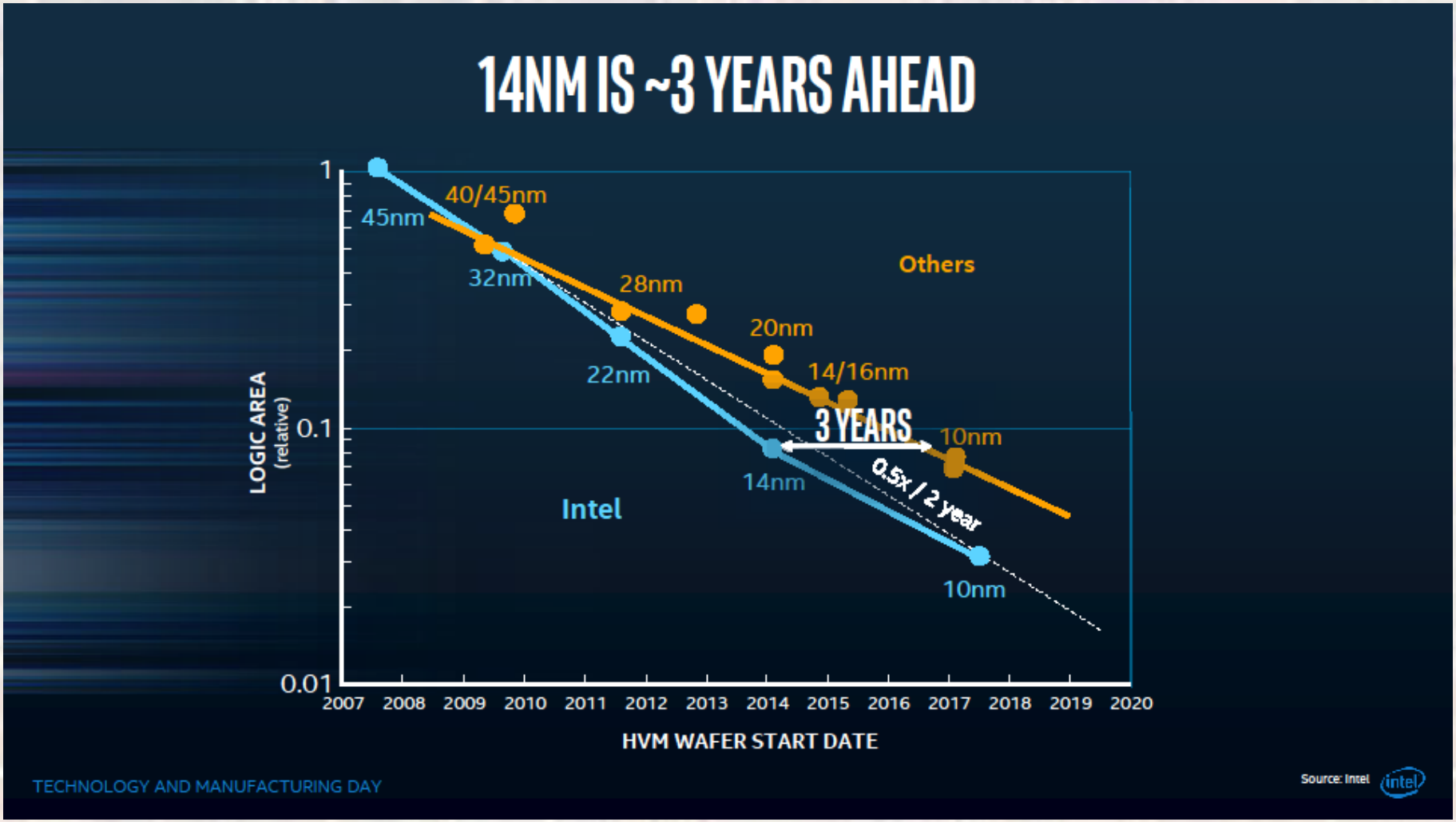
- Semiconductor Technology



CMOS Cost

- Semiconductor Technology

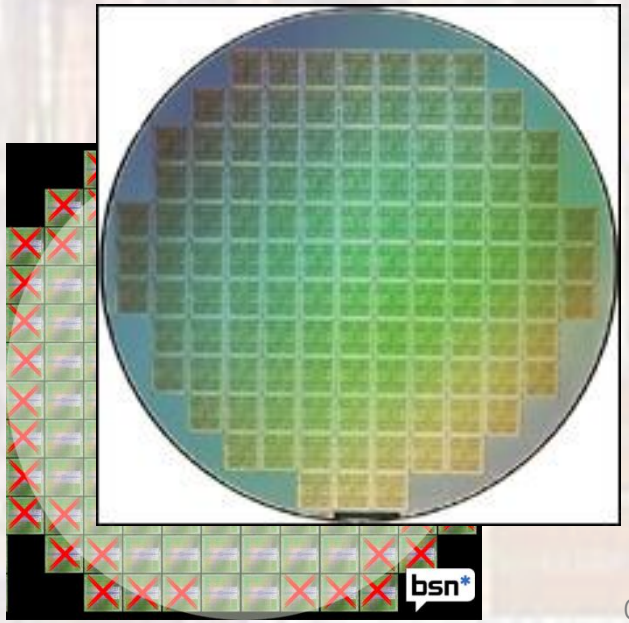


CMOS Cost

- Processor Cost Overview
  - Key Components building to part cost
    - Wafer Cost
      - 300mm wafers range from $5000/wafer (early) down to $1200/wafer (mature)
      - Cost reductions associated with process maturity
      - Wafer Yield = number of wafers that make it through the process with working transistors
    - Die Cost
      - Based on the number of full die that can fit on a wafer
    - Good Die Cost
      - Based on the number of die that are fully functional (may include redundancy)
    - Packaged Part Cost
      - Add the cost of package and packaging process
    - Good Packaged Part Cost
      - Based on the number of fully functional packaged parts (may include redundancy)
    - Margin
      - Additional $ to cover R&D, facilities, … AND profit

CMOS Cost

- Processor Cost Overview
  - Wafer Cost
    - 45nm, 300mm wafers ~ $2000/wafer
    - Typical “lot” of 25 wafers
    - Typical wafer yield of 95%
      - Losses are a combination of single wafers and whole lots
  - Die Cost
    - # of full die that will fit on a wafer
    - Various approaches to maximize die count
    - Die Cost = Wafer Cost / # of Die



CMOS Cost

- Processor Cost Overview

CMOS Cost

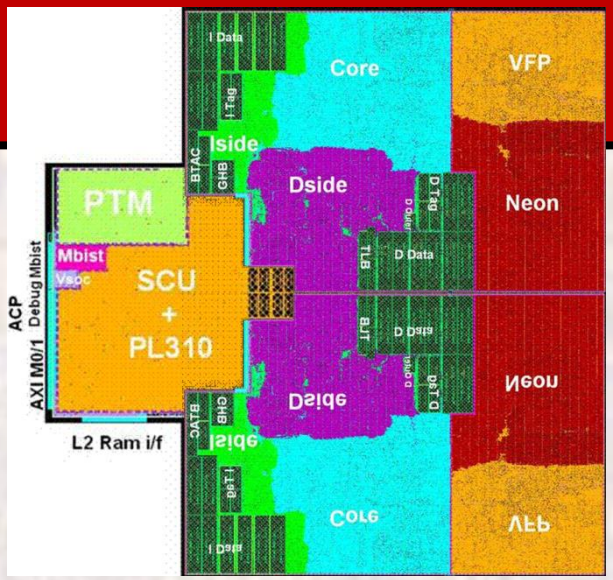
- Processor Cost Overview
  - Good Die Cost
    - Based on the number of die that are fully functional
    - 2 primary yield components
      - Parametric Yield
      - Process Yield
    - Parametric Yield
      - Parts that fail to meet a performance measure
      - Typically max frequency or current drain
      - Can be mitigated by binning (have a fast version of the part and a slow version)
      - Typically 95% on digital parts
    - Process Yield
      - Dominated by defects in the manufacturing process
      - $Y = Y_o(1 + \frac{D_0 A}{\alpha})^{-\alpha}$ NB - negative binomial model
      - Y_0 – portion of area subject to defects (0.8-0.95)(not other failures)
      - D_0 – defect density (100defects/cm^2 (early) – 0.15defects/cm^2(mature))
      - A - die area (20mm^2 – 400mm^2)
      - α - cluster factor (10 – 20)

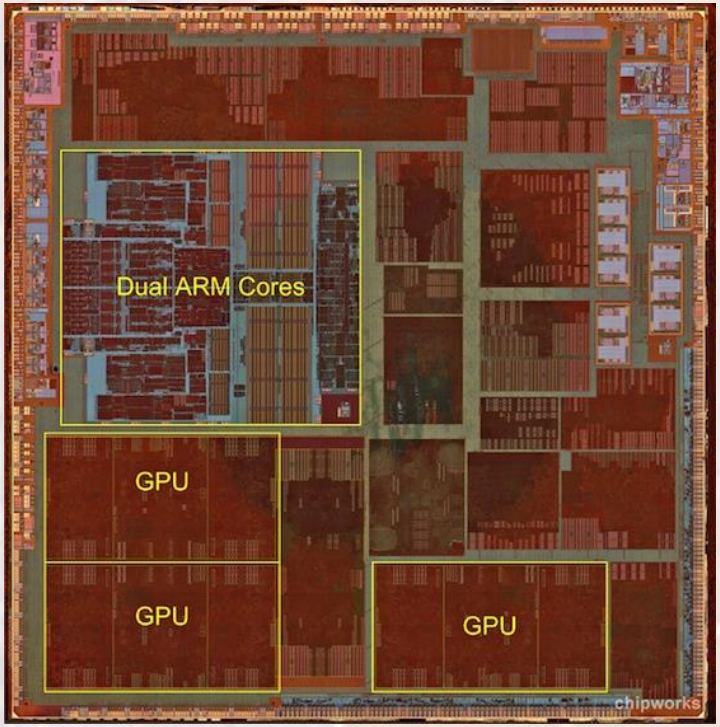
CMOS Cost

- Processor Cost Overview
  - Packaged Part Cost
    - Add the cost of package and packaging process
    - $0.20 for small simple packages
    - $2 - $4 for complex BGAs
    - $1 for POP
  - Good Packaged Part Cost
    - Based on the number of fully functional packaged parts
    - Package yield is typically 95% - 99+%
  - Margin
    - Additional $ to cover R&D, facilities, … AND profit
    - 20% for mature products
    - 50% for new products

CMOS Cost

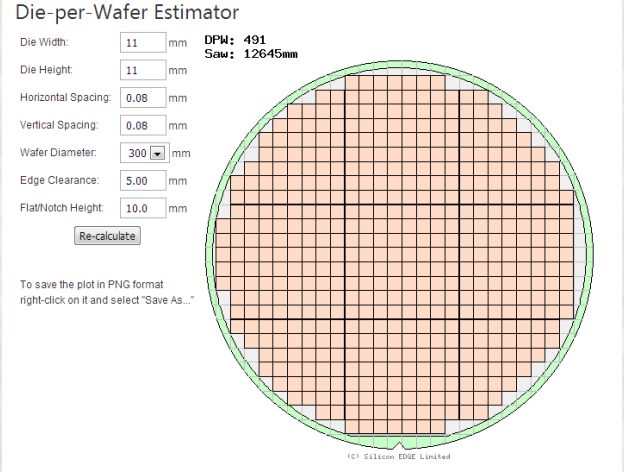
- Processor Cost Example
  - Arm Cortex A9
    - 32kB I/D Cache
    - 26M transistors
    - 500mW @ 2GHz
    - 5mm^2 in 45nm process technology
  - Apple A5
    - Dual - Arm Cortex A9s
    - 45nm Samsung Process
    - Die size = 122mm^2
    - 1300 pin POP - BGA
  - Samsung 45nm process
    - 300mm wafers
    - D_0 = 0.25 defects / cm^2
    - α= 10
    - Y_0A5 = 0.95





CMOS Cost

- Processor Cost Example
  - Wafer Cost
    - 300mm, 45nm → $2000 / wafer
    - Wafer yield – 95% → $2105 / wafer
  - Die Cost
    - 122mm2 → 491 die/wafer → $4.29 / die
  - Good Die Cost
    - $Y = Y_o(1 + \frac{D_0 A}{\alpha})^{-\alpha}$ = $0.95(1 + \frac{(0.25\ defects/cm^2)(122mm2 \times (\frac{1cm}{10mm})^2}{10})^{-10}$ = 0.703
    - Defect driven die cost = $4.29/die / 0.703 = $6.10 / die
    - Parametric yield – 0.98 → $6.22 / die
  - Packaged Part Cost
    - 1300 pin – POP-BGA = $3 → 9.22 / part



CMOS Cost

- Processor Cost Example
  - Good Packaged Part Cost
    - 98% yield → 9.41 / part
  - Margin
    - If this was not an Apple design
      - Margin = 50% → Part cost = $18.82
    - Apple can cover the margin costs at the final product level
      - → Part Cost = $9.41
  - Gut feel cost before margin = $6.50

CMOS Cost

- Product Cost
  - Direct Costs
    - Costs directly associated with the construction and delivery of a product
  - Indirect costs
    - Costs assigned to the development, manufacturing and delivery of a product
  - Non-Product costs
    - Administration, Sales, Marketing, …

CMOS Cost

- Direct Costs
  - Materials used in the product
    - Cost of ICs, other components, PCB boards, displays, housings, …
  - Manufacturing / Assembly
    - Labor
    - Assigned factory costs
    - Rework / Yield / Scrap
  - Other costs
    - Warranty
    - Packaging and delivery

CMOS Cost

- Indirect Costs
  - Development
    - Labor - Engineers, …
    - Resources – Computers, SW, lab equipment, …
    - Validation – development boards, prototypes, …
  - Intellectual Property
    - Unit Licenses
    - Technology Licenses

CMOS Cost

- Development Decision
  - Will this product provide a profit to the company after all costs?

Product Sales Price * # of Units

>

Direct costs * # of units

+

Development Costs

+

Overhead Costs

+

Profit

CMOS Cost

- Development Decision
  - Will this product provide a profit to the company after all costs?

Product Sales Price * # of Units — Unit Price

>

Direct costs * # of units — Unit Cost

+

Development Costs

+

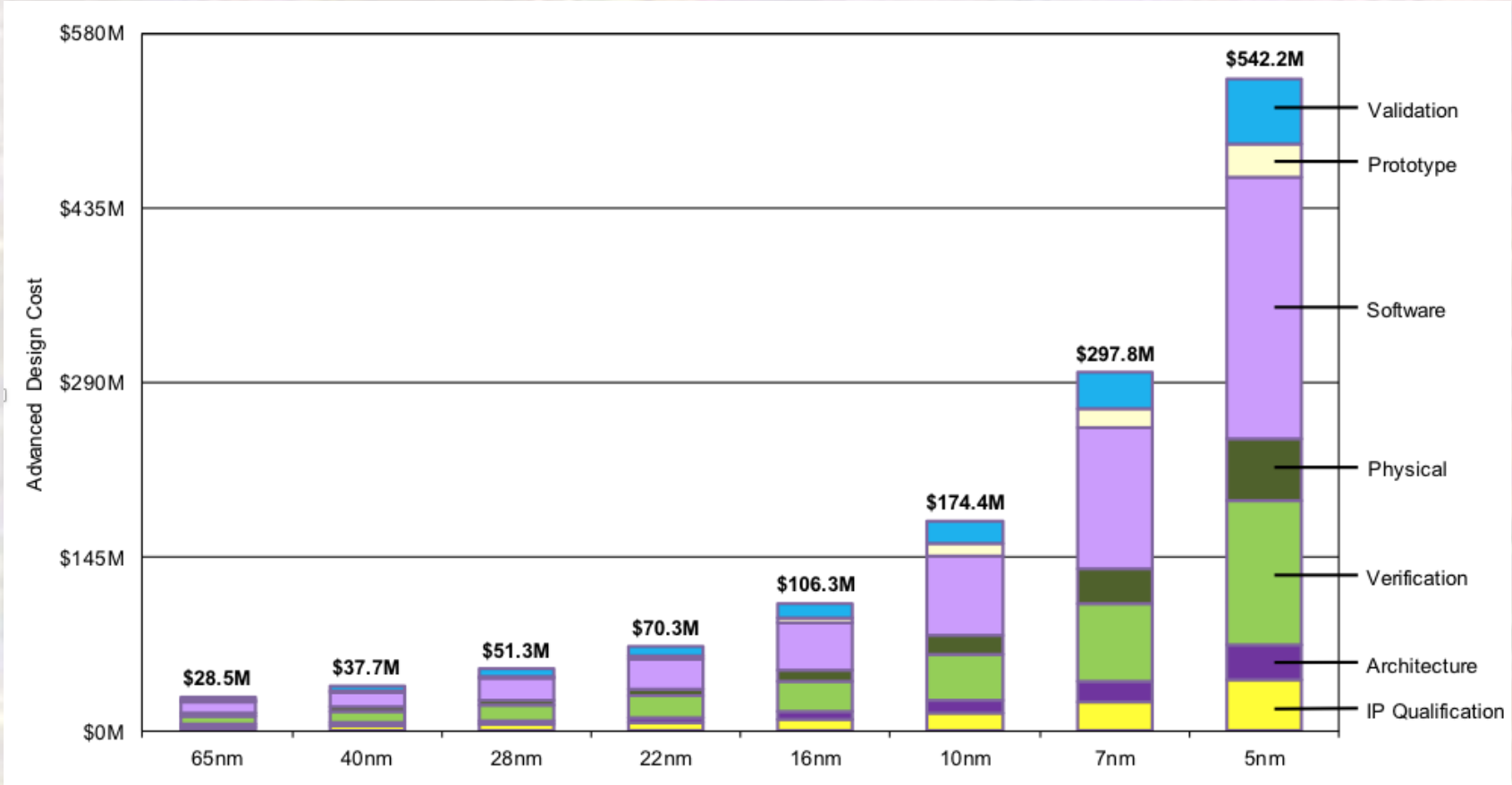
Overhead Costs — Margin

+

Profit

CMOS Cost

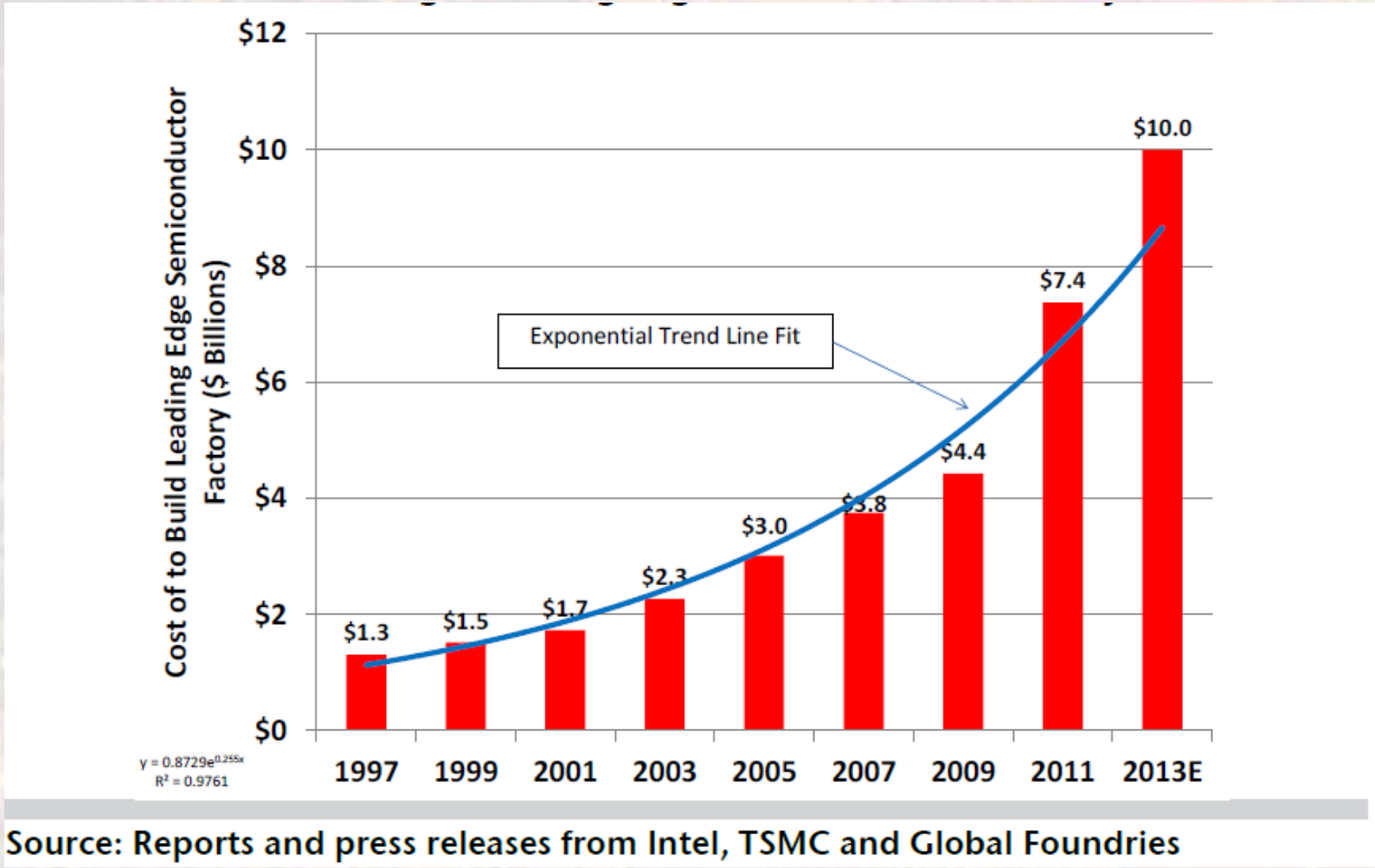
- Design Costs



Extereme tech

CMOS Cost

- Factory Cost Trends



Seeking alpha

CMOS Cost

- Wafer cost trends

semiengineering

CMOS Cost

- Product cost over time