CMOS Devices

Last updated 2/25/21

CMOS Devices

- Mini-History of Main-Stream Integrated Circuits
  - Point Contact Diode
  - Junction Diode
  - JFET – Junction Field Effect Transistor
  - BJT – Bipolar Junction Transistor
  - MOSFET
    - Enhancement Mode Metal Oxide Semiconductor Field Effect Transistor
    - Depletion Mode Metal Oxide Semiconductor Field Effect Transistor
    - N-Channel, P-Channel
  - E + D N-channel transistors → NMOS Technology
  - E_P + E_N channel transistors → CMOS Technology
    - Complementary Metal Oxide Semiconductor Field Effect Transistor
  - BiCMOS – Bipolar + MOS

Planer Process Technology

> 100um > 4mil

< 20nm

Rapidly changing Process Technology
FinFET
Channel All Around
Nano-Tubes

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CMOS Devices

- MOS Terminology
  - Metal Oxide Semiconductor Field Effect Transistor
  - 4 terminal devices
    - Source, Gate, Drain, Body
  - Threshold Voltage (Vth or Vt)
    - The voltage from gate to source (Vgs) required to “turn on” the device
  - Ron / Roff
    - Device impedance in the “on” or “off” state
  - Leakage Current
    - Parasitic current from junctions to substrate or gate to junctions

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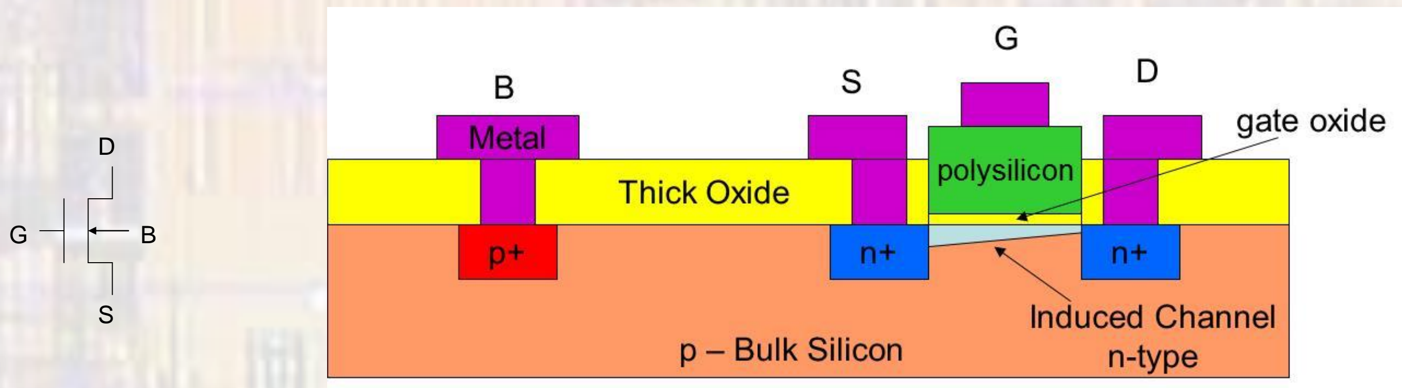
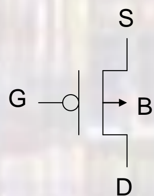
CMOS Devices

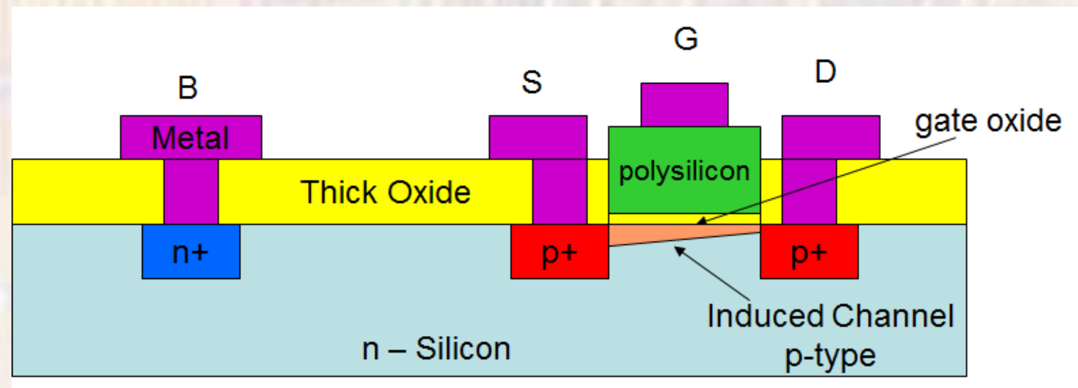
- MOS Terminology
  - N-type (N-channel)
    - Forms a conducting n-channel from source to drain
    - Requires a positive Vgs > Vth to form the channel and "turn on" the device



CMOS Devices

- CMOS Terminology
  - P-type (P-channel)
    - Forms a conducting p-channel from source to drain
    - Requires a negative Vgs > Vth to form the channel and “turn on” the device





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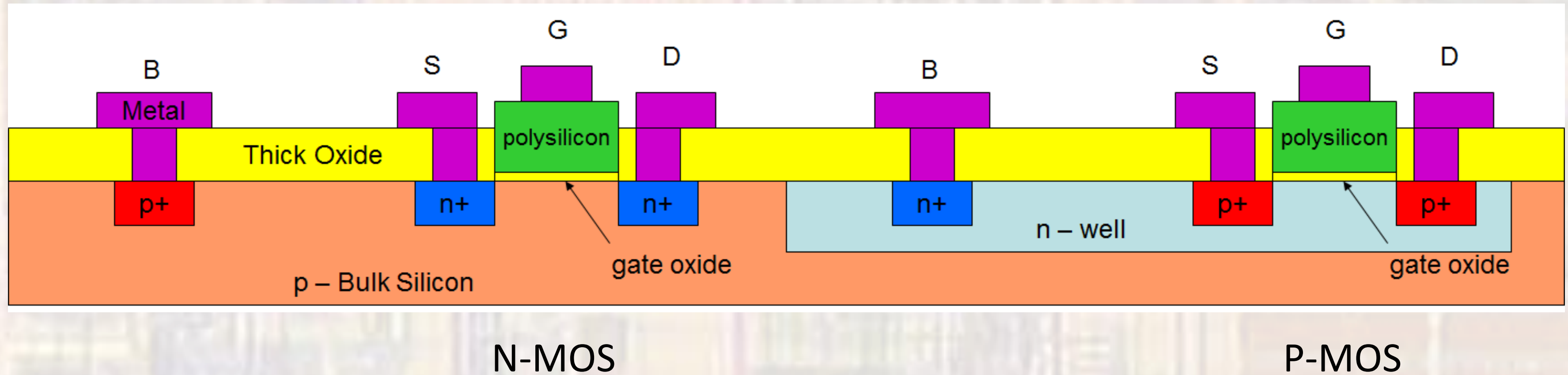
CMOS Devices

- MOS Terminology
  - CMOS
    - Complementary MOS
    - Contains both P-MOS and N-MOS devices
    - Almost all digital circuits today are built using CMOS technology



N-MOS P-MOS

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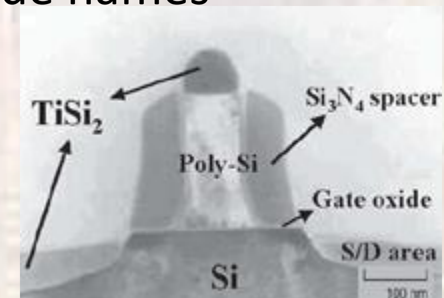
CMOS Devices

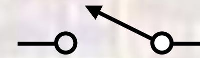
- CMOS Process Technology
  - Traditionally referenced to the gate length or metal 1/2 pitch
    - 0.25 micron process, 130nm process, 14nm process
  - Over the years the relationship between reference name and physical parameters has become tenuous
    - Silicon atom spacing is ~5 angstroms = 5×10^{-10}m
      → 14nm = 28 atoms
    - Reference names more closely tied to L_{eff}
    - Move underway to redefine the technology node names
  - Gate oxide thickness is 2nm
    → 4 rows of atoms



Src: TMS - Vol 57, No. 9

CMOS Devices

- Simplified CMOS Digital Design
  - Use simplified models for the MOSFETs
    - switch – either “on” or “off”



  - N-MOS devices
    - “on” when a logic high is applied to the gate
    - “off” when a logic low is applied to the gate
  - P-MOS devices
    - “on” when a logic low is applied to the gate
    - “off” when a logic high is applied to the gate

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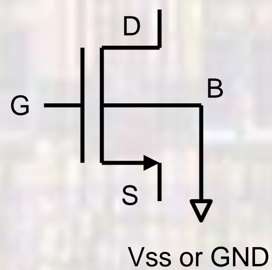
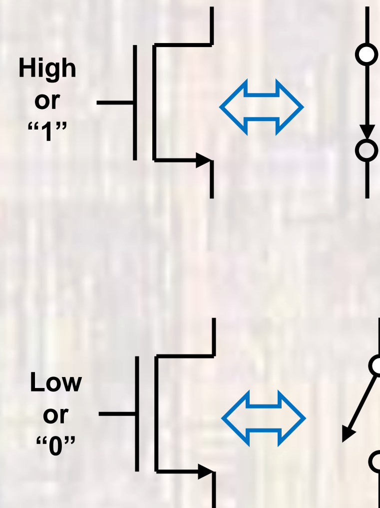
CMOS Devices

- Simplified CMOS Digital Design
  - N-MOS devices
    - “on” when a logic high is applied to the gate
    - “off” when a logic low is applied to the gate





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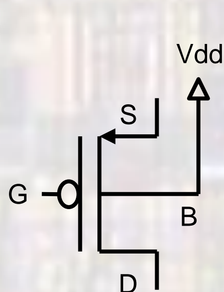
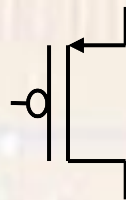
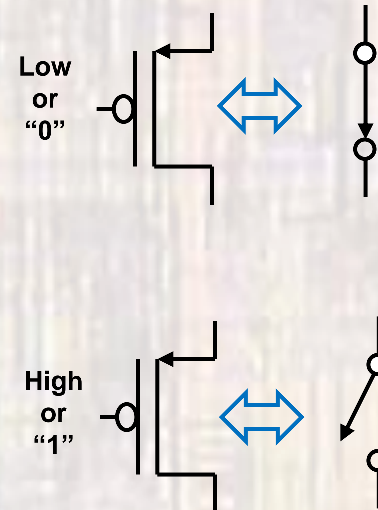
CMOS Devices

- Simplified CMOS Digital Design
  - P-MOS devices
    - “on” when a logic low is applied to the gate
    - “off” when a logic high is applied to the gate

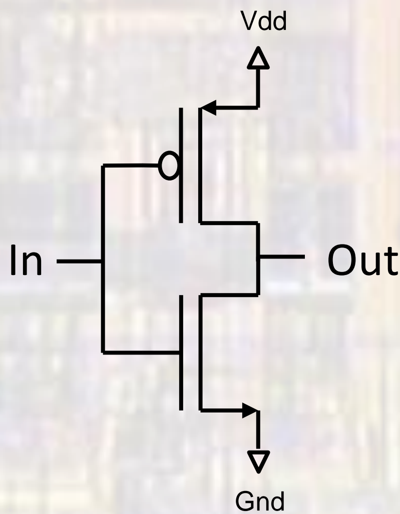


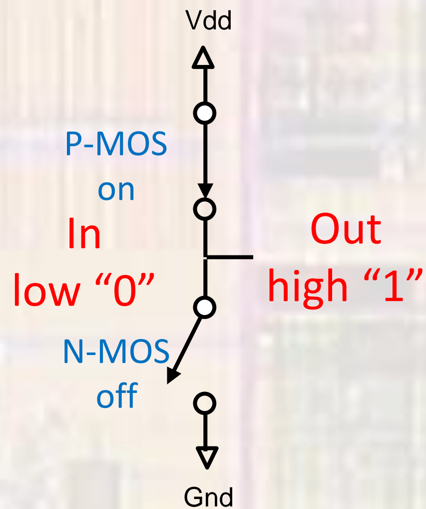


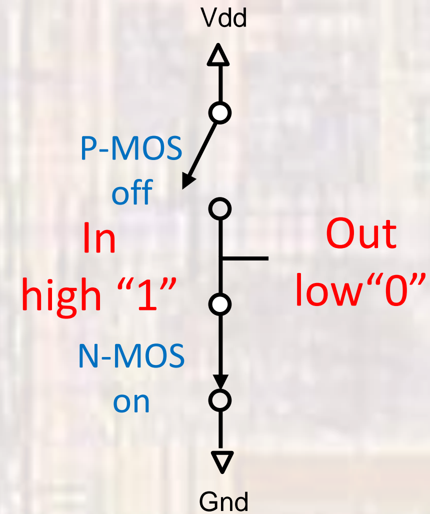


CMOS Devices

- Simplified CMOS Digital Design
  - CMOS Inverter
    - logic low “0” is Gnd
    - logic high “1” is Vdd



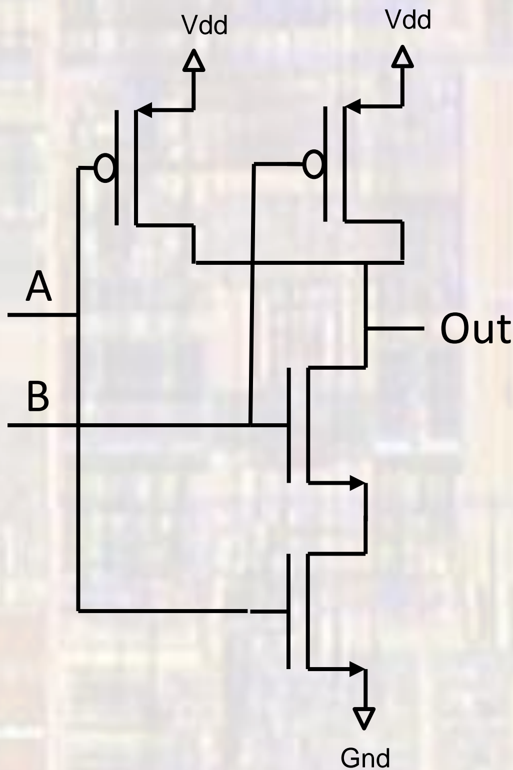


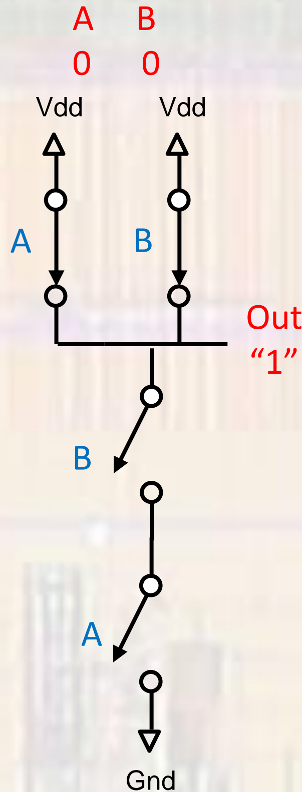


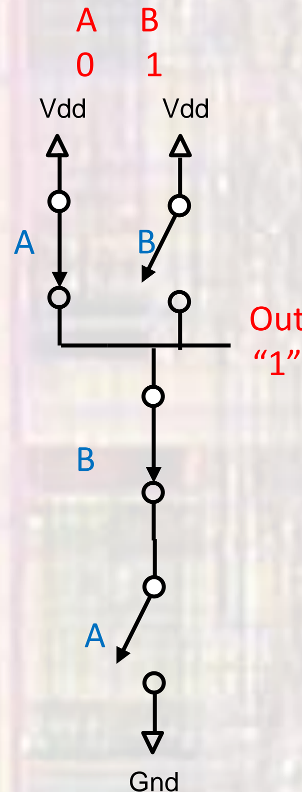
CMOS Devices

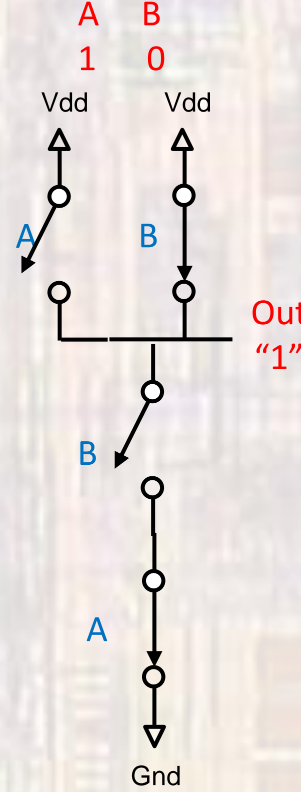
- Simplified CMOS Digital Design
  - CMOS Nand Gate

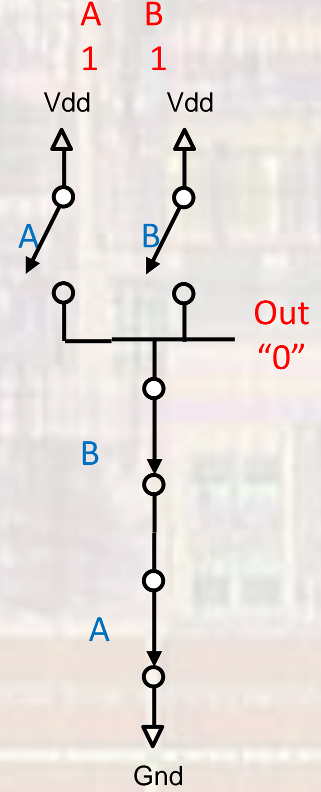
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0











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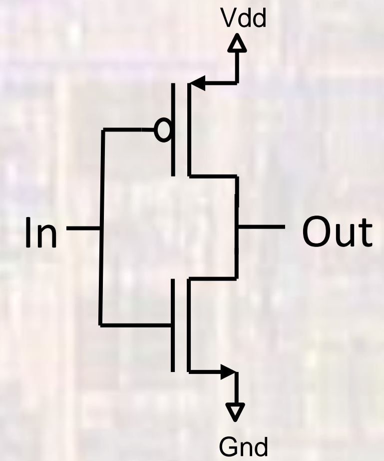
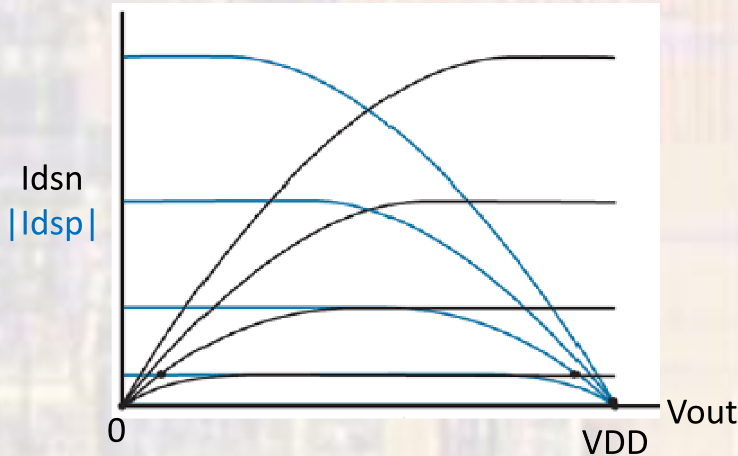
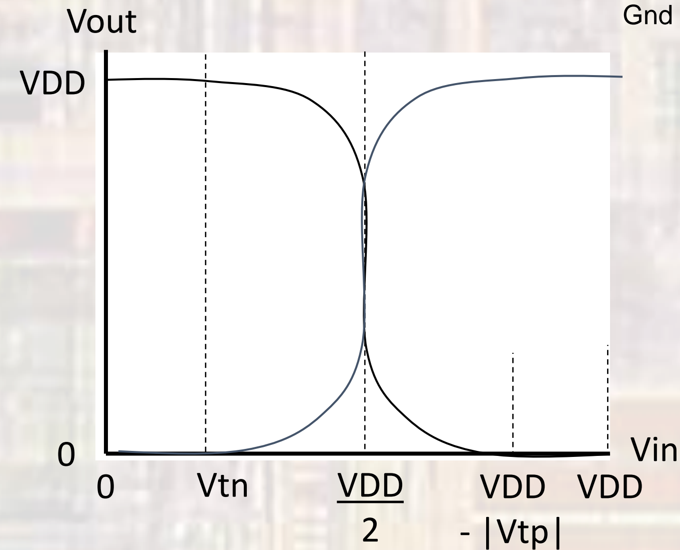
CMOS Devices

- Gate Level Performance

  - DC Characteristics
    - $I_{DS} = \beta[(V_{GS} - V_t)V_{DS} - {V_{DS}}^2/2]$ - linear region
    - $I_{DS} = \beta/2\,(V_{GS} - V_t)^2$ - saturated region
    - $\beta = \frac{\mu\varepsilon}{t_{ox}}\frac{W}{L}$ $\beta_n \cong 2.8\beta_p$







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CMOS Devices

- Gate Level Performance

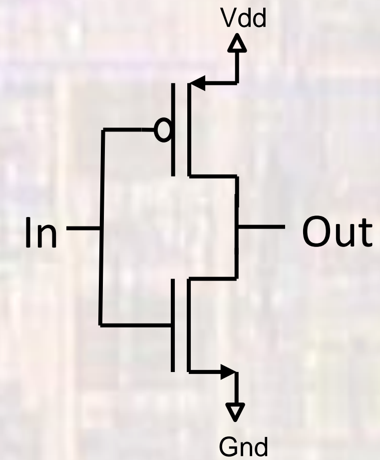
  - Transient Characteristics

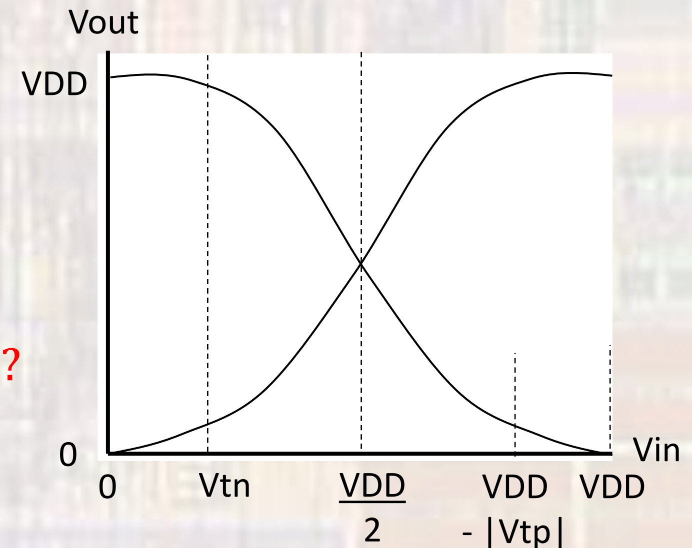
    - Equalize t_r and t_f by making Wp ≅ 2.8 Wn

    - $t_r \cong t_f \cong K_n \frac{C_L}{\beta_n V_{DD}} \cong K_p \frac{C_L}{\beta_p V_{DD}}, \quad Kn \sim Kp \sim 3.5$

    - $t_d \cong t_r/2 \cong t_f/2$

    - Optimize delay
      - reduce C_L
      - increase V_{DD}
      - increase β → reduce t_{ox}
        - why might this be the best approach?





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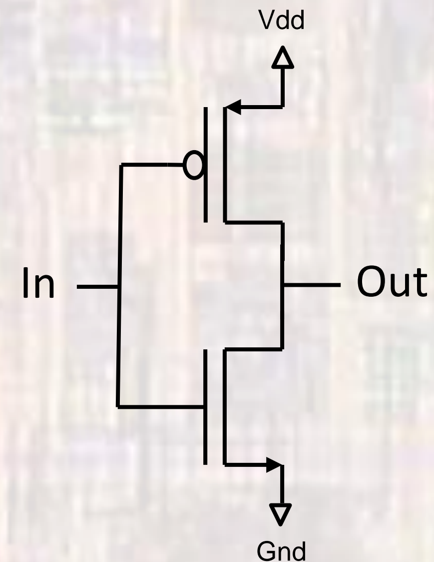
- Gate Level Power
  - 3 primary components of gate level power
  - Static Power (leakage)
  - Dynamic Power (CV^2F)
  - Short Circuit Power (shoot-through)



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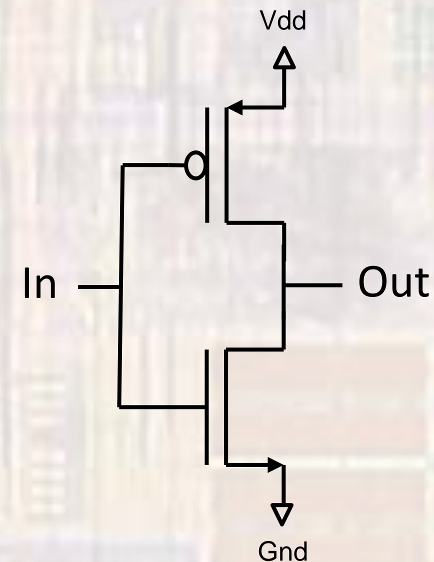
CMOS Devices

- Gate Level Power

  - Static Power
    - Leakage currents through the reverse biased diode junctions – always present
    - Sub-threshold current – current from S-D when the input voltage is below Vt – due to voltage drops
    - Gate leakage current – current from the gate to S/D/Body – due to oxide defects or quantum tunneling

  - Design Considerations
    - Multiple Vt devices
    - Thick oxide devices
    - Reduce supply voltages – why?



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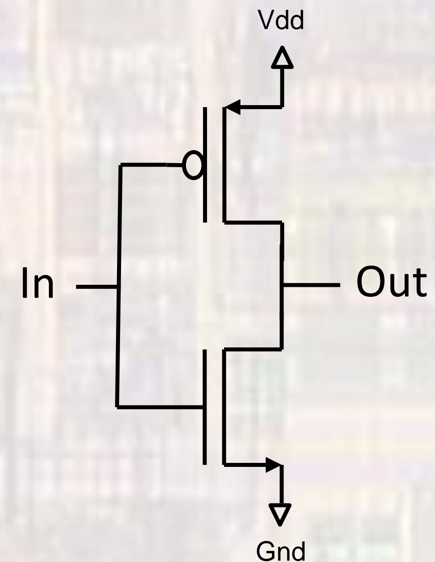
CMOS Devices

- Gate level Power
  - Dynamic Power
    - Power associated with slewing the load capacitance
    - E = $\int Pdt = \int IVdt = \int C\, {}^{dV}/_{dt}\, Vdt = \int CVdv = \frac{CV^2}{2}$
    - energy per transition = $C_L V_{dd}^2/2$
    - Power is energy / time
    - $P_{dynamic} = CV^2f$
  - Design considerations
    - Run circuits at the lowest possible speed
    - Reduce supply voltages
    - Minimize capacitance



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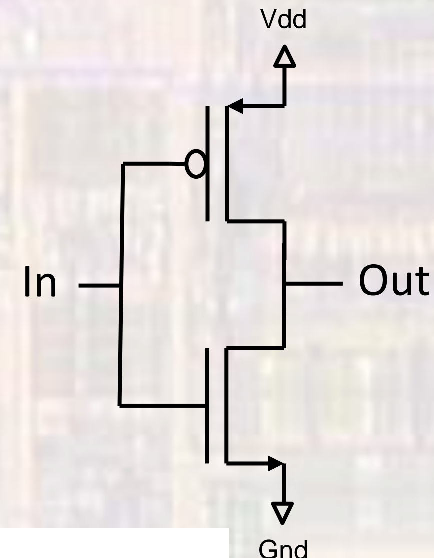
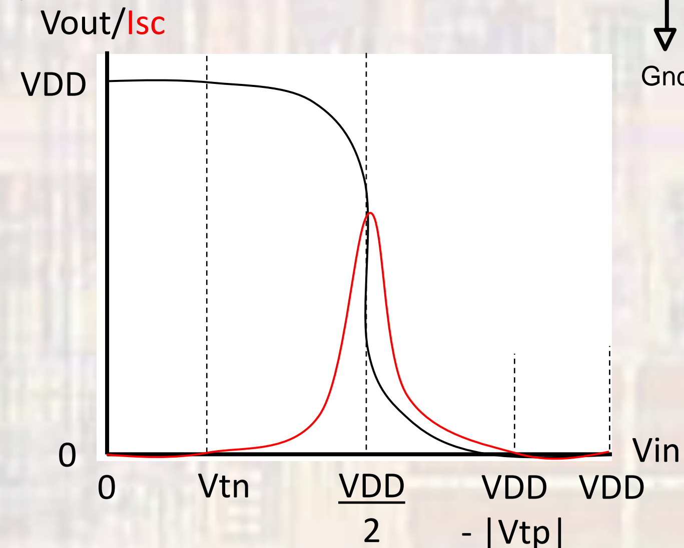
CMOS Devices

- Gate Level Power
  - Short Circuit Power
    - Both devices are on
    - Symmetrical gate →

$$P_{sc} \cong \frac{\beta}{12}(V_{DD} - 2V_t)^3 f\, t_{rf}$$





  - Design Considerations
    - large relative loads → lower Psc
    - small relative loads → higher Psc
    - Match t_r and t_f through the chain
    - Reduce supply voltages

CMOS Devices

- Gate Level Power
  - Resulting Trends
    - Lower Voltages
      - Reduces power
      - Allows thinner junctions
      - Slows down devices
    - Smaller Geometries
      - Lower capacitances
      - More devices / chip
      - Higher process development costs
    - Thinner Oxides
      - Increase β
      - Higher gate capacitance

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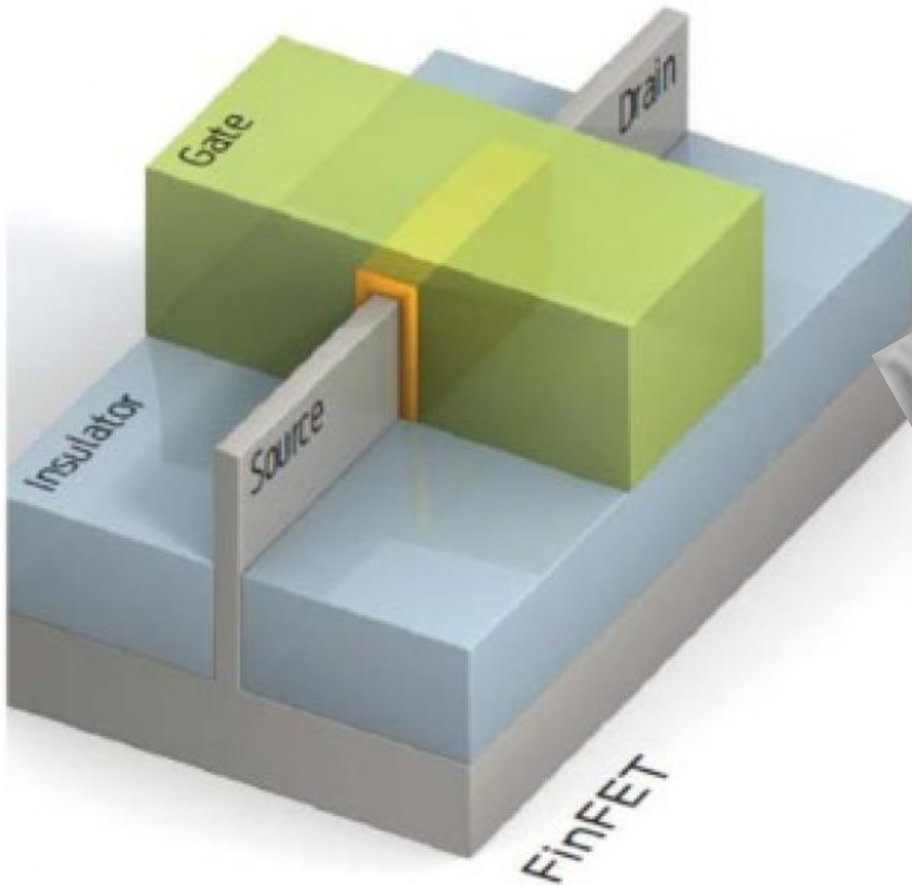
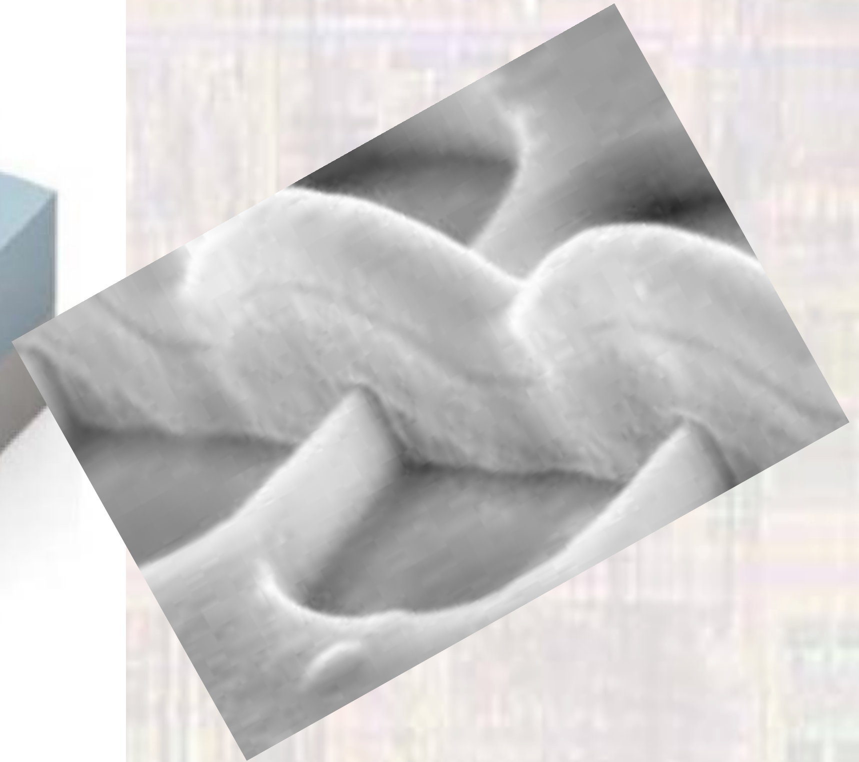
CMOS Devices

- FinFET Technology



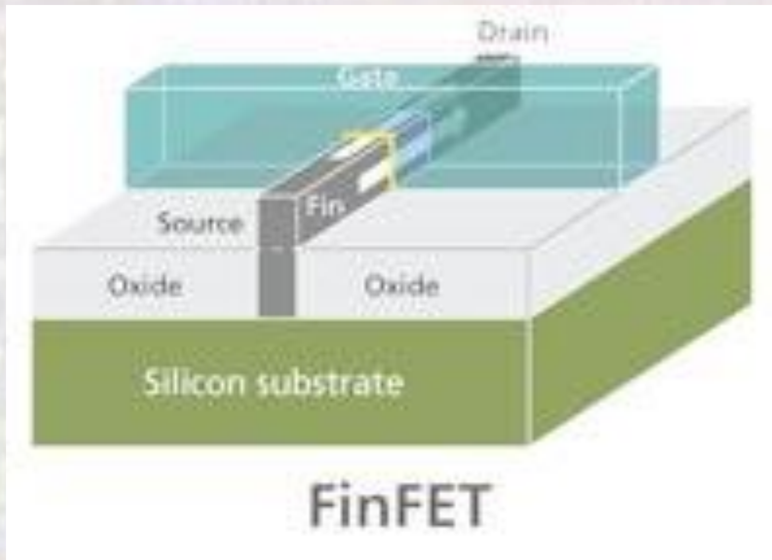
14nm-class FinFET transistor



CMOS Devices

- FinFET Technology

42nm each side + 6nm top = 90nm W_{eff}
with actual pitch of 24nm



All Fins and all Gates are a standard size

Larger devices are created by wiring standard devices in parallel

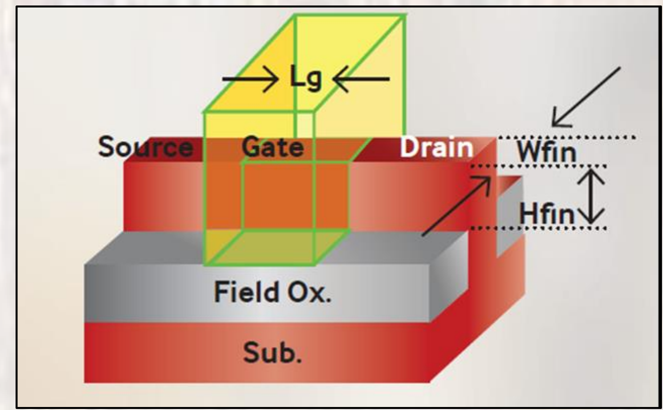
Dummy Fins and Gates can be used to ensure uniformity

CMOS Devices

- FinFET Technology

Physical Properties of Transistors

YEAR OF PRODUCTION	2015	2017	2019	2021
Logic device technology naming	P70M56	P48M36	P42M24	P32M20
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"
Logic device structure options	FinFET FDSOI	FinFET FDSOI	FinFET LGAA	FinFET LGAA VGAA
LOGIC DEVICE GROUND RULES				
MPU/SoC Metalx ½ Pitch (nm)[1,2]	28.0	18.0	12.0	10.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0
Contacted poly half pitch (nm)	35.0	24.0	21.0	16.0
L_g: Physical Gate Length for HP Logic (nm) [3]	24	18	14	10
L_g: Physical Gate Length for LP Logic (nm)	26	20	16	12
FinFET Fin Half-pitch (new) =0.75 or 1.0 M0/M1 (nm)	21.0	18.0	12.0	
FinFET Fin Width (nm)	8.0	6.0	6.0	
FinFET Fin Height (nm)	42.0	42.0	42.0	



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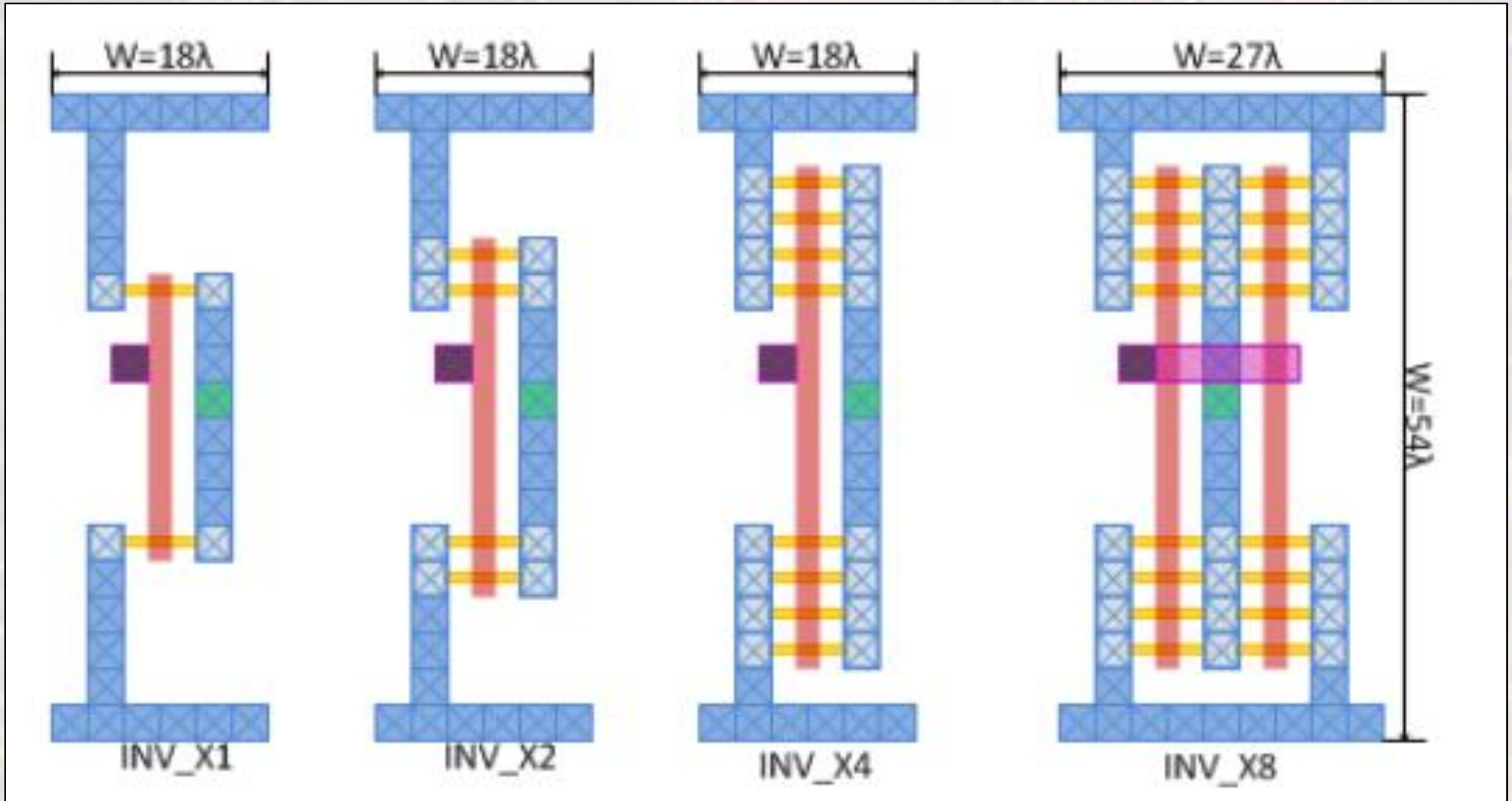
- FinFET Technology



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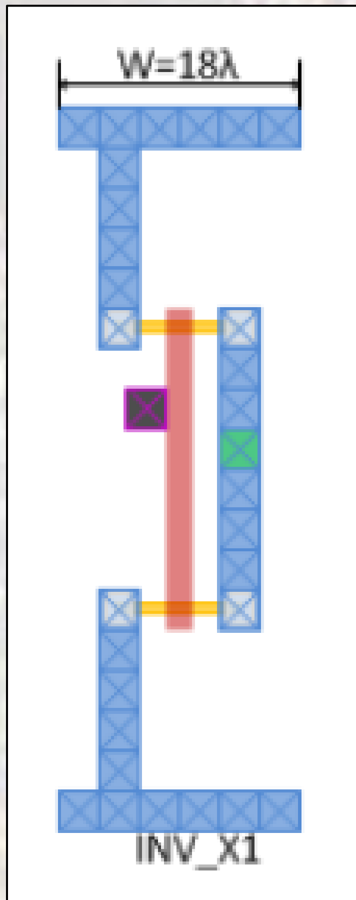
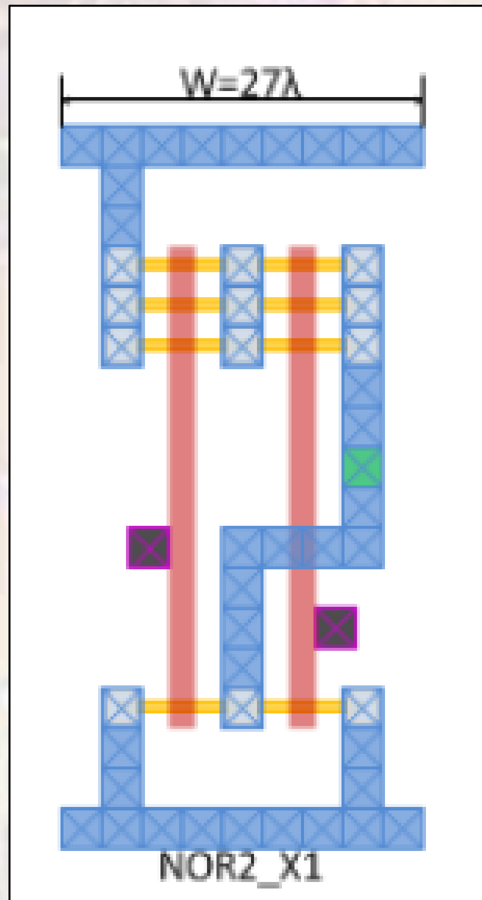
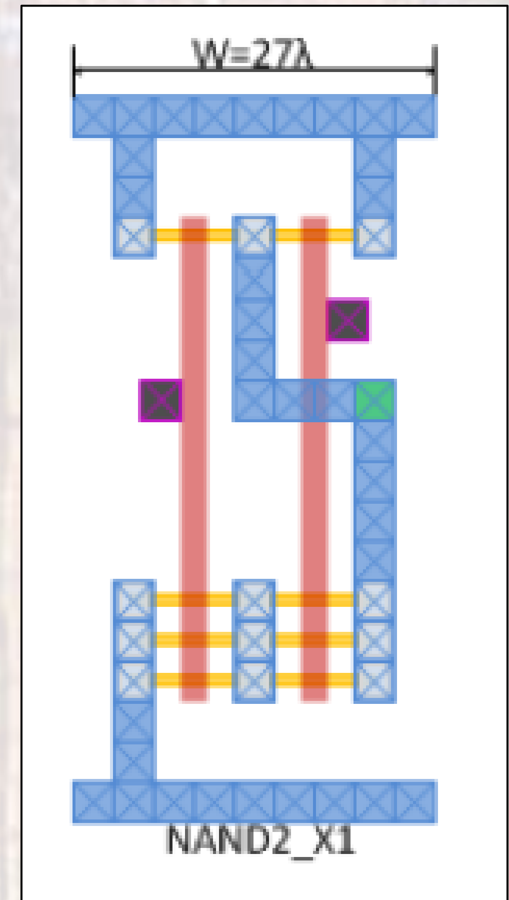
- FinFET Technology







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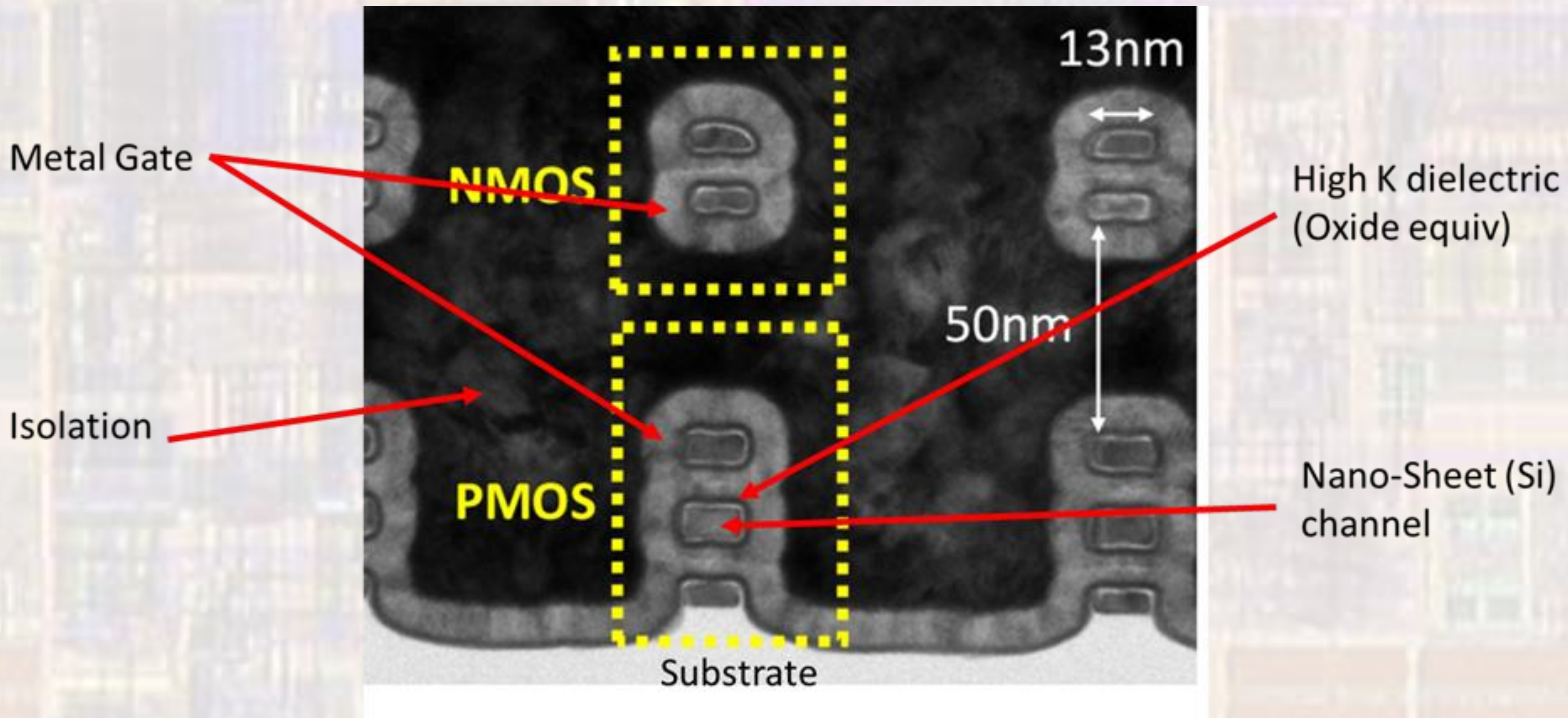
- Intel NanoSheet
  - Vertical stack – gate all around



CMOS Devices

- Technology players dwindling due to dev costs

Number of Semiconductor Manufacturers with a Cutting Edge Logic Fab

180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm
SilTerra										
X-FAB										
Dongbu HiTek										
ADI	ADI									
Atmel	Atmel									
Rohm	Rohm									
Sanyo	Sanyo									
Mitsubishi	Mitsubishi									
ON	ON									
Hitachi	Hitachi									
Cypress	Cypress	Cypress								
Sony	Sony	Sony								
Infineon	Infineon	Infineon								
Sharp	Sharp	Sharp								
Freescale	Freescale	Freescale								
Renesas (NEC)	Renesas	Renesas	Renesas	Renesas						
Toshiba	Toshiba	Toshiba	Toshiba	Toshiba						
Fujitsu	Fujitsu	Fujitsu	Fujitsu	Fujitsu						
TI	TI	TI	TI	TI						
Panasonic	Panasonic	Panasonic	Panasonic	Panasonic	Panasonic					
STMicroelectronics	STM	STM	STM	STM	STM					
HLMC	HLMC		HLMC	HLMC	HLMC					
UMC	UMC	UMC	UMC	UMC	UMC		UMC			
IBM	IBM	IBM	IBM	IBM	IBM	IBM				
SMIC	SMIC	SMIC	SMIC	SMIC	SMIC		SMIC	SMIC		
AMD	AMD	AMD	GlobalFoundries	GF	GF	GF	GF			
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel

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