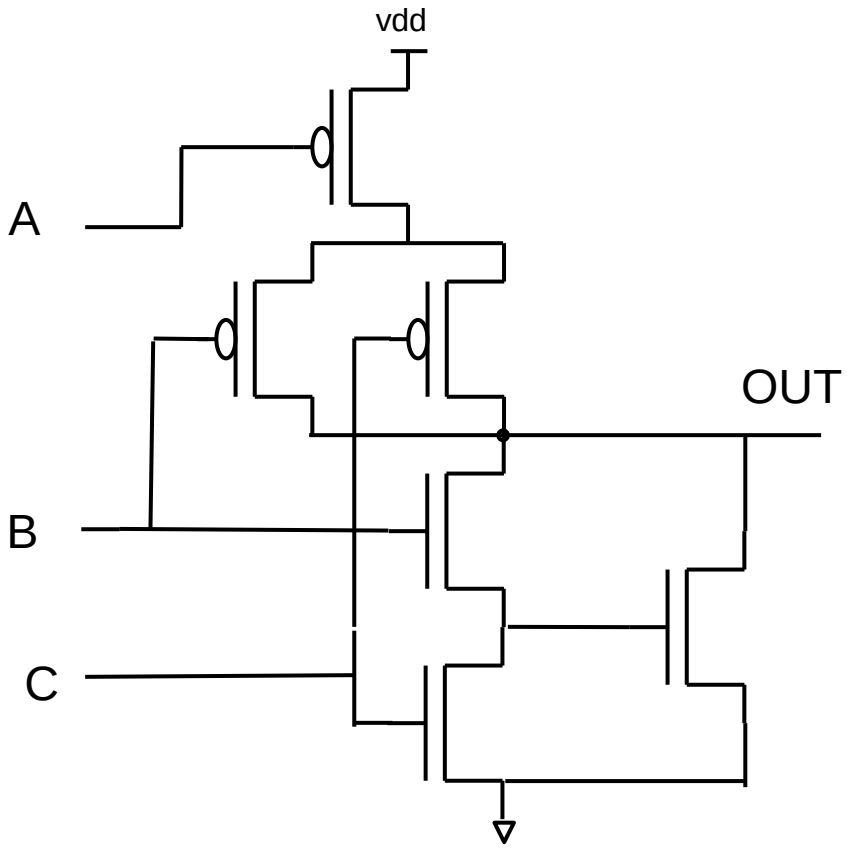
EE 4980
Modern Electronic Systems

HW 2

Create a truth table for the circuit below (assume DC) 10pts

Use:1, 0, z for tristate, x for unknown but 0 or 1, u for unknown



You are responsible for the clock design for a new processor.
Determine the maximum parasitic capacitance allowed on the clock line CLK 20 pts

Design Requirements:

- Target operating frequency: 2.5GHz
- 45 mW of power has been allocated for your clock signal: CLK

Known values:

- Operating voltage: 1.2V
- Static power used in your design: 0.5mW
- Short circuit power used in your design: 2mW @ 2.5GHz
- Flip-Flop clk input capacitance: 0.2pF
- Total # of FF on the CLK line: 50

You have been tasked with determining if supplier A is asking a fair price for a new part you want to buy. Your company has spent money with a 3rd party company to get cost estimate information about the part in question. Determine the expected price for the part. 30pts

Information from the 3rd party:

- Wafer cost: $2500
- Raw wafer yield: 97%
- Defect density: 0.15defects/cm2
- α = 15
- Package Cost: $0.005/ball
- Packaged part yield:96%

Acceptable margin for company A:

- 40%

- Die size: 95mm2
- Parametric yield: 96%
- Package: 32x32 ball BGA
- Y_0=1
- 200mm wafer
- 260 die per wafer

Determine the processor in your laptop and the nominal operating frequency
Search for it in the PassMark database and provide its 10pts

- CPU Mark
- Rank
- Cost

Search and Think 30pts

FinFET devices typically utilize “dummy” fins and gates in their design – provide a short description of why?

FinFETs are clearly the technology of the near future – identify the impact these devices might have on **analog** integrated circuit designs