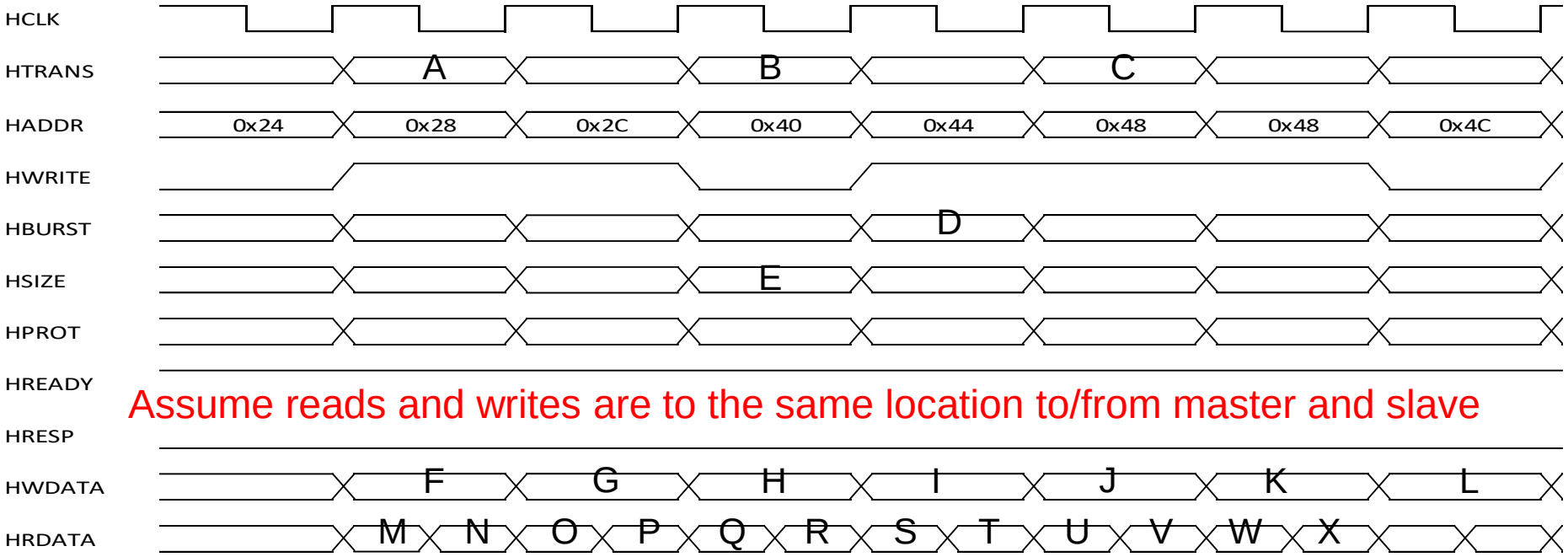
EE 4980
Modern Electronic Systems

HW 5

Below is a trace from an APB bus, fill in the table below (leave unknowns empty) after completion of this trace. 32 bit address and data 15pts

Address	Data: Master (via the bridge)	Data: Slave (peripheral)
0x1234		
0x12AB		
0x4321		
0xAB12		
0xABCD		
0xDCBA		

Below is a trace from an AHB-Lite bus, fill in the values below (leave unknowns empty) 35 pts



Assume reads and writes are to the same location to/from master and slave

Data - Prior to beginning of trace

Address	Master	Slave
0x24	0x00	0x11
0x28	0x01	0x22
0x2C	0x02	0x33
0x40	0x03	0x44
0x44	0x04	0x55
0x48	0x05	0x66
0x4C	0x06	0x77

Location	Value (hex)	Location	Value (hex)
A		M	
B		N	
C		O	
D		P	
E		Q	
F		R	
G		S	
H		T	
I		U	
J		V	
K		W	
L		X	

Assume a PCIe Link operating a 8GT/s 30pts

a) In a 1x configuration what is the Link bandwidth using 8b/10b encoding (don't use the table from the notes – it will not be right)

b) In a 4x configuration what is the Link BW using 128b/130b encoding

c) Assuming a 1x configuration, 8b/10b encoding, a 4DW header, 32 Bytes of data and no ECRC or End, how many bits would transfer in a single read request?

d) Assuming a 4x configuration, 8b/10b encoding, a 4DW header, 32 Bytes of data and no ECRC or End, how long would a single read request take?

Search and Think 20 pts

Identify and explain 3 advantages of using differential signaling

Identify at least 1 disadvantage of differential signaling