EE 4980

Test 2

110 pts

Open Everything
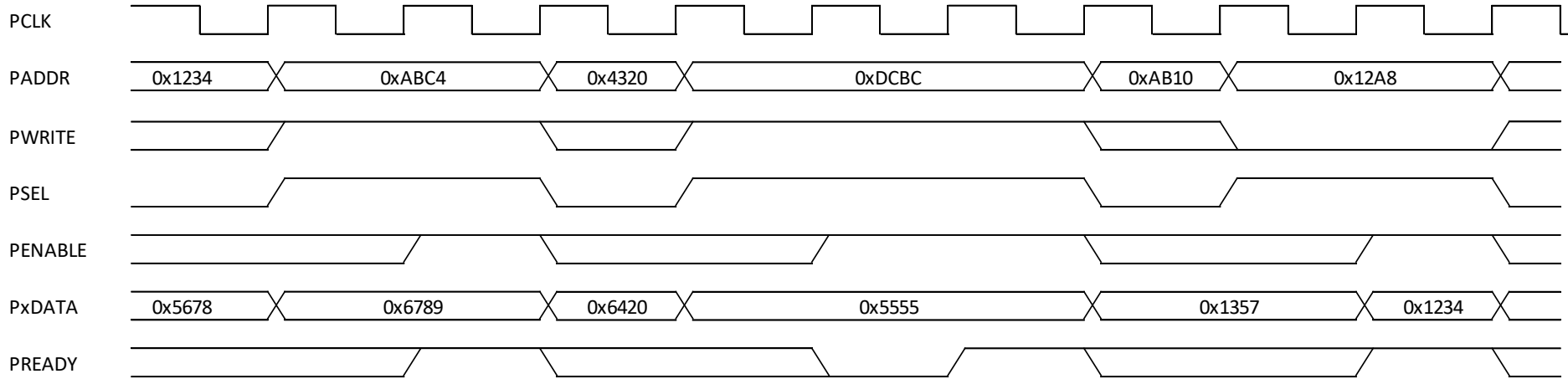No Collaboration

Process:

The test will be posted at 11:00 AM on the test day on the HW web page

Solutions are due 60 minutes later in OneNote inside the Tests tab

I will be available via MS-Teams or email if you have questions or internet issues

1) Below is a trace from an APB bus, fill in the table below (leave unknowns empty) after completion of this trace. 32 bit address and data   10pts

PCLK

| PADDR | 0x1234 | 0xABC4 | 0x4320 | 0xDCBC | 0xAB10 | 0x12A8 |

PWRITE

PSEL

PENABLE

| PxDATA | 0x5678 | 0x6789 | 0x6420 | 0x5555 | 0x1357 | 0x1234 |

PREADY

	Data	
Address	Master (via the bridge)	Slave (peripheral)
0x1234		
0x12A8		
0xAB10		
0xABC4		
0xABD0		
0xDCBC		

2a) PCIe is a _____ interconnect system   10pts

      A) Half Duplex – multi-node network
      B) Point to point network
      C) Star network
      D) Bus based network

2b) PCIe uses 8/10bit and 128/130 bit encoding to achieve what two outcomes:

      _____   _____

2c) Assume a PCIe Link operating at 8GT/s in a 4x configuration with a total of 400 bits in the frame how long would a single read request take?

3) Using the (2,7) RLL decoder from class   10 pts
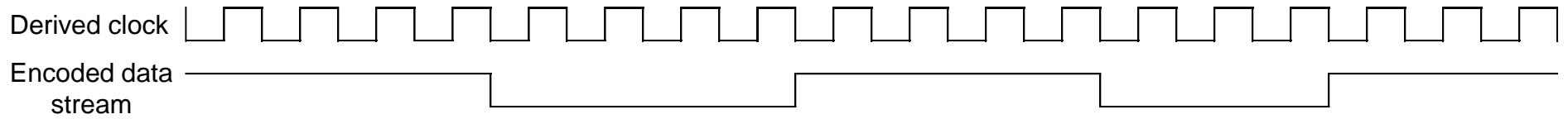
a) Decode the following signal

N N N T N N N N T N N N N N N T N N N N N N T N N N

b) Encode the following signal

001111010000

c) Decode the following waveform (assume positive edge capture by the clock)

Derived clock

Encoded data
stream

4) Consider a 10 in x 10 in resistive touch screen, given the following measurements, locate the touch point: 10pts
Assume: resistivity = 5K ohm / inch
     Drive voltage = 5V at top and right
     Y measurement = 2.77V
     X measurement = 1.43V
     Define the origin at the lower left corner

_____ inches from bottom
_____ inches from left

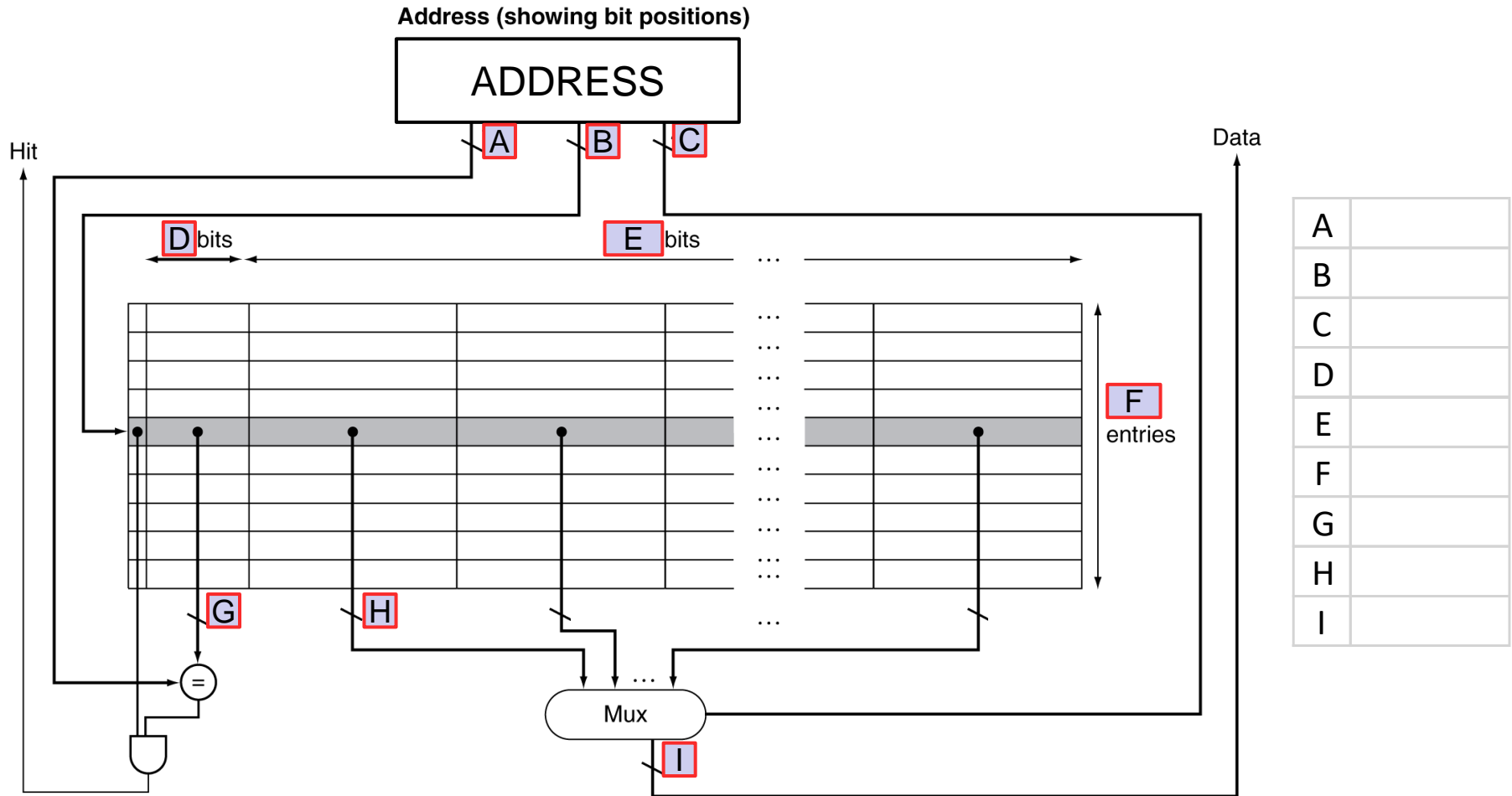5) Assuming a 5 stage pipeline with 1us delay per stage   10pts

A) What is the execution time for each instruction

B) Assuming the processor has been running for a long time – how many instructions complete in a 10us window

C) How many of these pipelines would need to be configured in a superscalar configuration to achieve an IPC of 5

6) Given a 4kB direct mapped cache with 16 bit words, 8 word blocks, and 32 bit addressing – fill in the table referencing each letter. 10 pts

Address (showing bit positions)

ADDRESS

A B C

Hit

Data

D bits   E bits ...

F entries

G H

=

Mux ...

I

A	
B	
C	
D	
E	
F	
G	
H	
I	

7a) Explain why 4 satellites may not be sufficient to get a GPS fix when accounting for the receiver clock error.   5 pts

7b) Identify at least 2 approaches to solve this problem   5 pts

8a) Explain why the range (R) in the RADAR equation is raised to the 4th power   5 pts

8b) Explain why the target cross-section may not be directly related to the size of the target   5 pts

9) In our wireless charging discussion, we said that the device being charged could communicate back to the charging station. Briefly explain the electrical mechanism that makes this possible   5 pts

10) In Bluetooth, what type of link is used for voice communication and why?   5 pts

11) Search and think   10 pts

There are 3 types of RFID tags, passive, active, and battery assistive passive. The passive RFID tags have no battery. How are they able to transmit the tag information to a scanner with no battery?

What technology(ies) that we discussed this term directly relate to RFID technology?

12) Think   10 pts

My car has a number of safety/convenience features. Identify the technology(ies) we discussed this term that applies to each feature

a) Lane assist (warns when I leave my lane)

b) Active cruise control (keeps space to next car)

c) Anti-collision

d) Android Auto (Apple Carplay)

e) Navigation

f) 10in Display

g) keyless entry/start

h) Backup camera