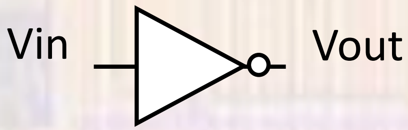
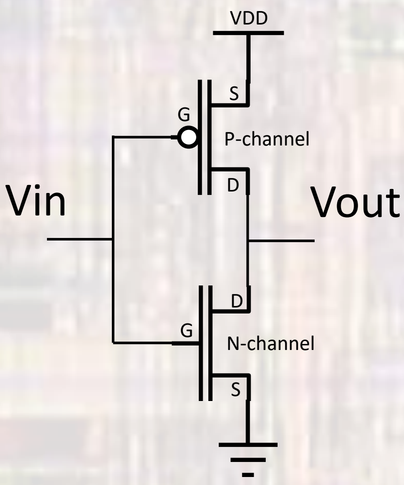
CMOS Inverter Analysis

Last updated 3/22/19

CMOS Inverter

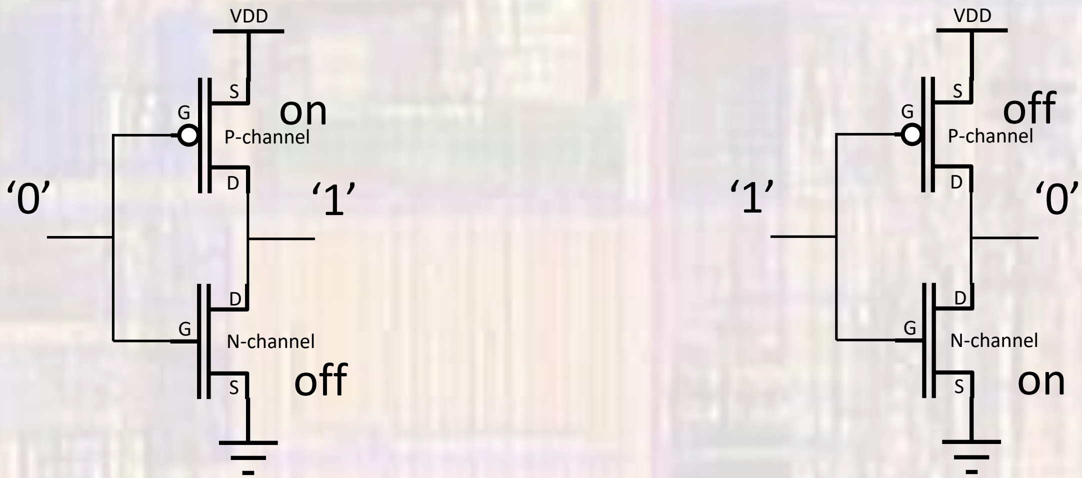
- Inverter Circuit

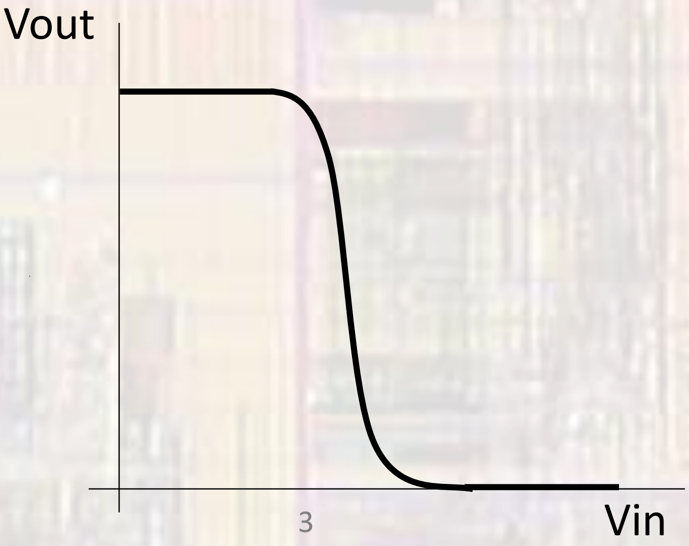




CMOS Inverter

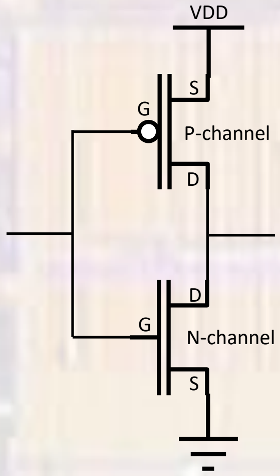
- Inverter Circuit

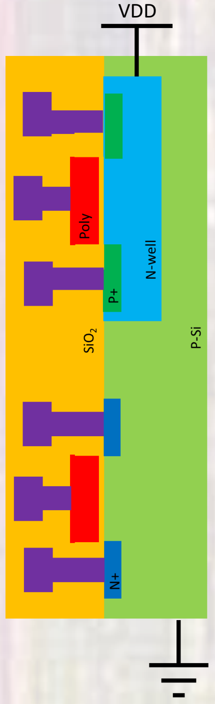




CMOS Inverter

- Inverter Circuit



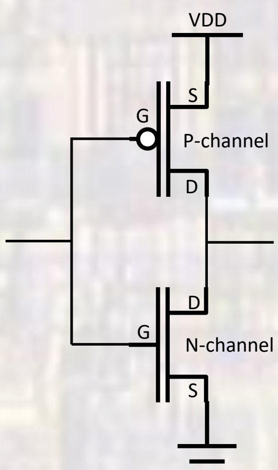


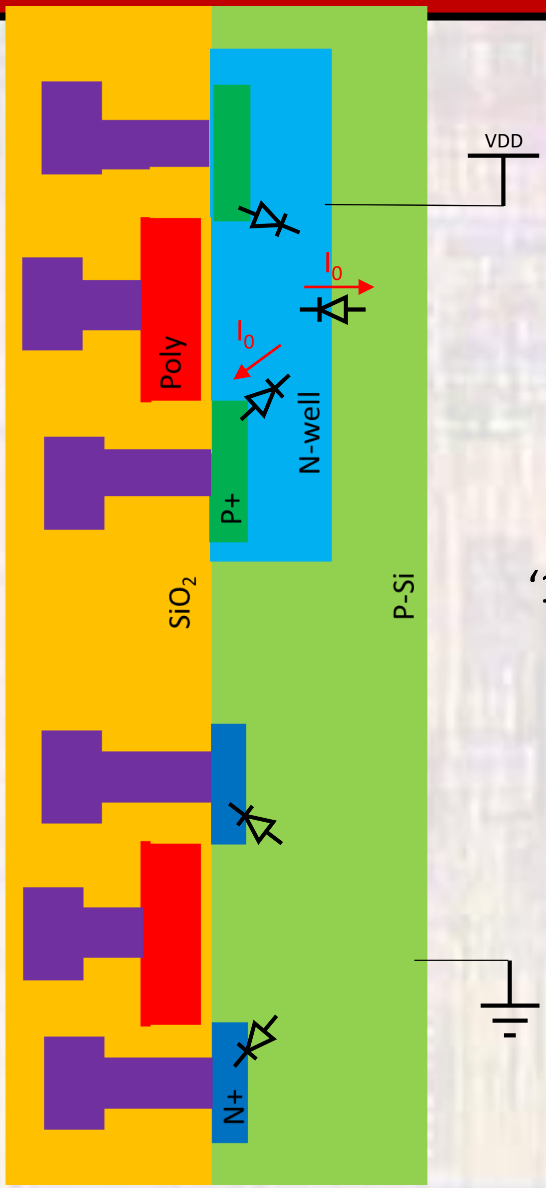
CMOS Inverter

- Inverter Circuit Power
  - Static (DC)
    - No Active power
    - Parasitic currents

      All Diodes are reverse or zero biased

      → I_0 currents





‘1’ in → N-ch on

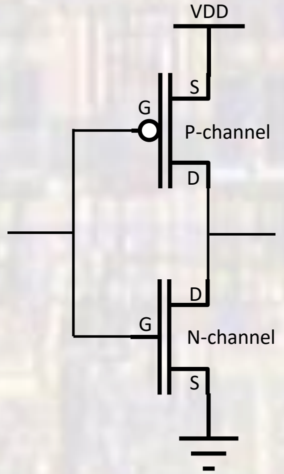
→ P-ch off

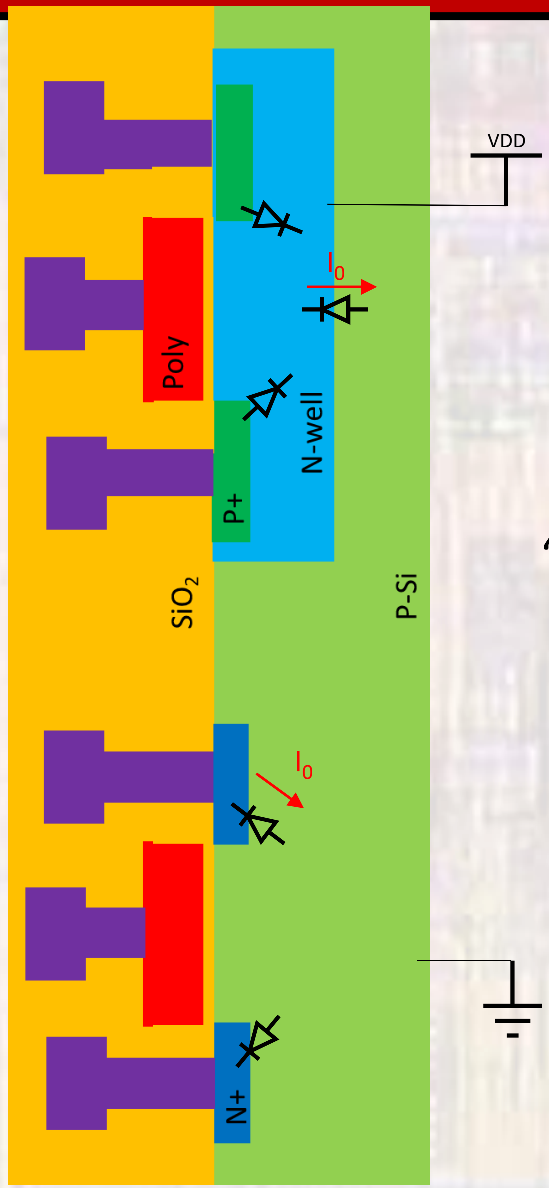
CMOS Inverter

- Inverter Circuit Power
  - Static (DC)
    - No Active power
    - Parasitic currents

      All Diodes are reverse or zero biased

      → I_0 currents

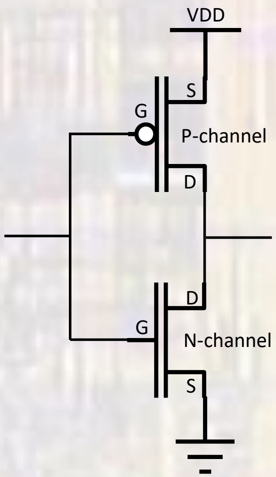


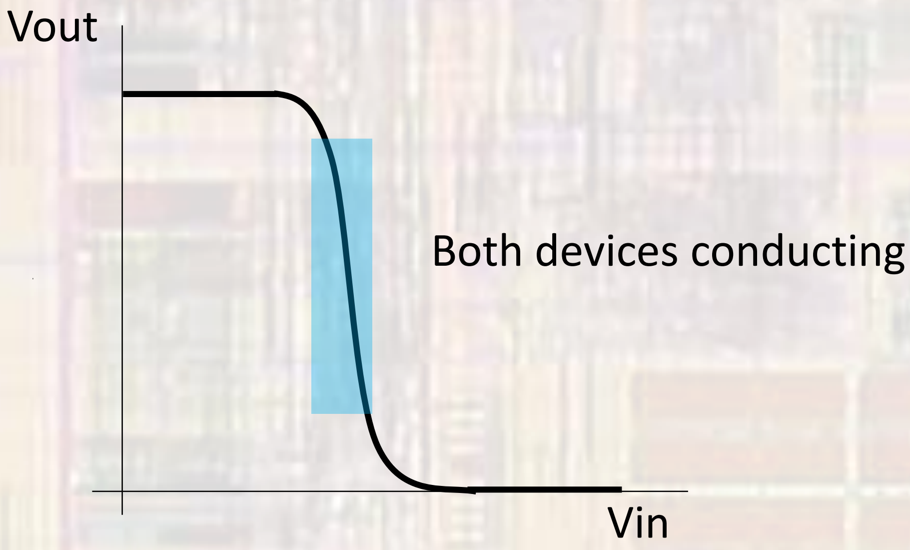


'0' in → P-ch on
→ N-ch off

CMOS Inverter

- Inverter Circuit Power
  - Switching
    - Shoot through current
    - Short period of time where both P and N are on
    - Very “noisy” in synchronous systems

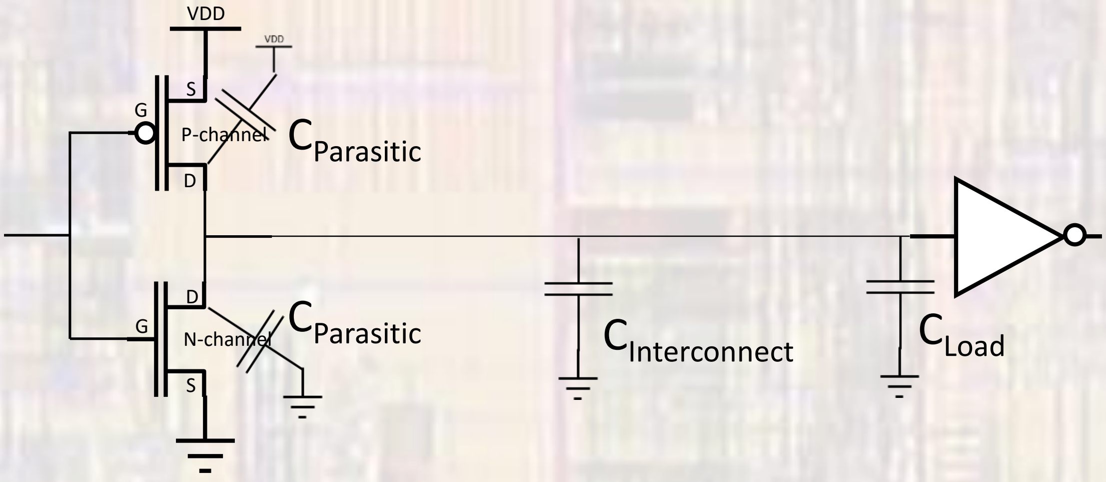




CMOS Inverter

- Inverter Circuit Power
  - Switching
    - Charging / discharging currents
    - Very “noisy” in synchronous systems

$$i = C \, {}^{dv}\!/_{dt}$$

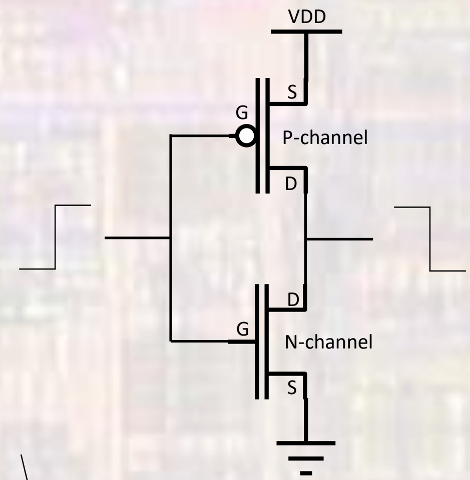


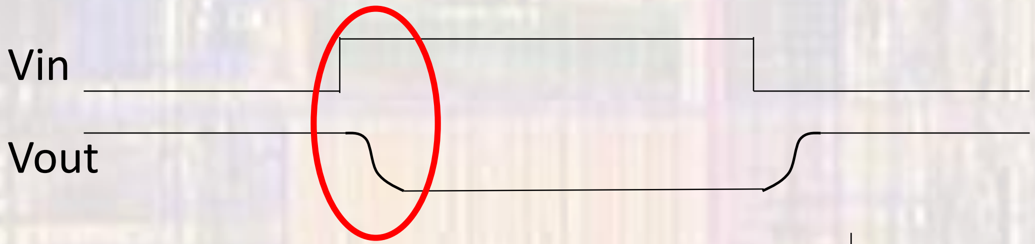
CMOS Inverter

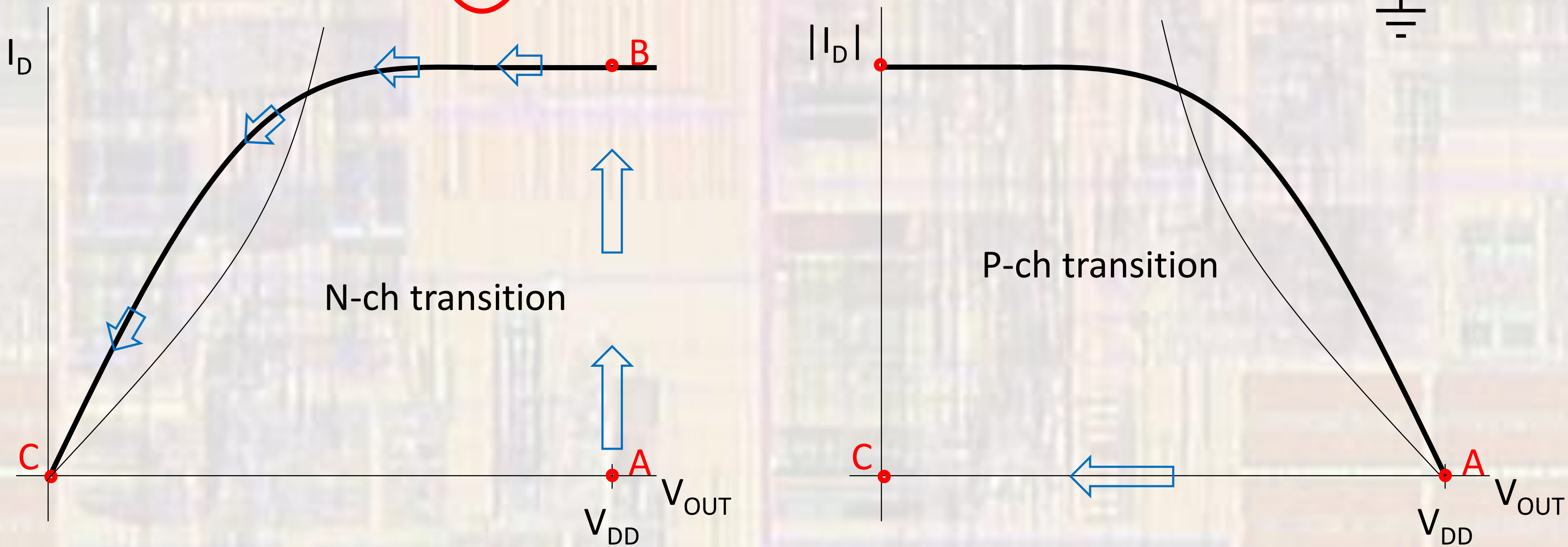
- Inverter Circuit Power
  - Putting it all together
    - $i = i_{static} + i_{shoot\text{-}through} + i_{charging}$
    - i_{static} ~ # of gates
    - $i_{shoot\text{-}through}$ ~ # gates and F
    - $i_{charging}$ ~ F, # gates, wiring
      - $i_{charging} = CVF$
      - $P_{charging} = CV^2F$
        - → reductions in V

CMOS Inverter

- Inverter Switching Analysis (simplified)
  - Fall Time
    - 90% → 10%

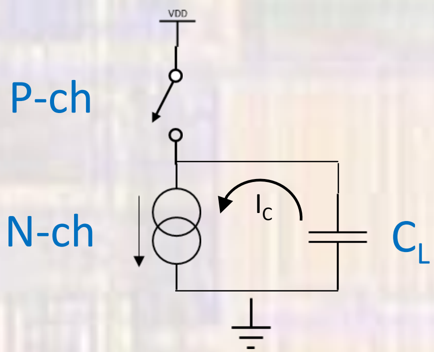




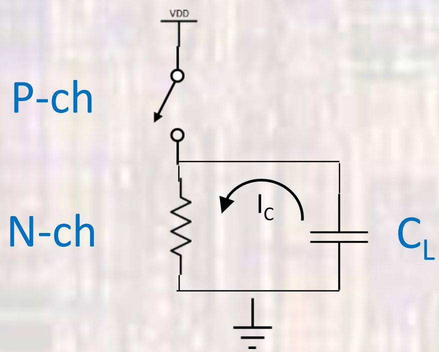


CMOS Inverter

- Inverter Switching Analysis (simplified)
  - Fall Time



Saturation



Linear

$$C_L \frac{dV_o}{dt} + \frac{\beta_n}{2}(V_{DD} - V_{Tn})^2 = 0$$

$$V_o \geq V_{DD} - V_{Tn}$$

$$C_L \frac{dV_o}{dt} + \beta_n\left[(V_G - V_{Tn})V_D - V_D^{\ 2}/2\right] = 0$$

$$V_o < V_{DD} - V_{Tn}$$

CMOS Inverter

- Inverter Switching Analysis (simplified)
  - Fall Time
    - Integrating over the appropriate times

$$t_f = 2\frac{C_L}{\beta_n(V_{DD} - V_{Tn})} \times \left[\frac{V_{Tn} - 0.1 \times V_{DD}}{V_{DD} - V_{Tn}} + \frac{1}{2}\ln\left(\frac{19 \times V_{DD} - 20 \times V_{Tn}}{V_{DD}} \right) \right]$$

    - With V_{Tn}=0.45V and V_{DD}=1.2V

$$t_f = 4.22\frac{C_L}{\beta_n}\left(\frac{1}{Volts}\right)$$

$$t_f = 30.6 \times 10^3 \times C\frac{L}{W}\left(\frac{\sec}{F}\right)$$

$$\beta = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)$$

$$\mu_n = 200 cm^2 / V - \sec$$

$$\varepsilon_{Si} = 3.9\varepsilon_0 = 3.9 \times 10^{-14} F / cm$$

$$t_{ox} = 5nm$$

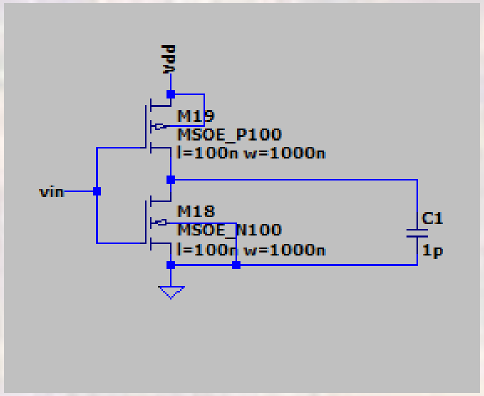
$$\beta_n = \frac{W}{L} \times 138 \mu A / V^2$$

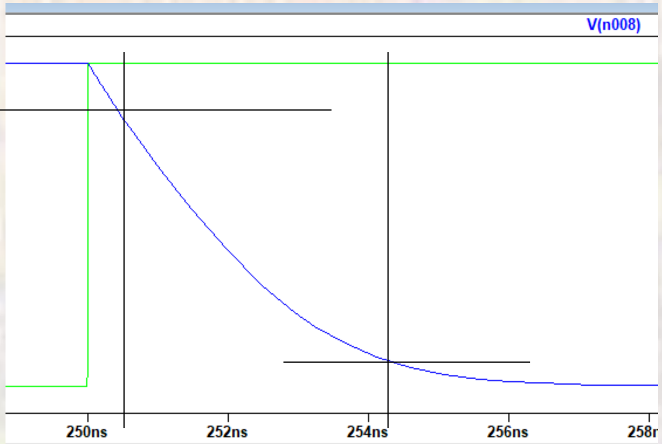
CMOS Inverter

- Inverter Switching Analysis (simplified)
  - Fall Time

$$t_f = 30.6\times10^3 \times C\,\frac{L}{W}\left(\frac{\sec}{F}\right)$$

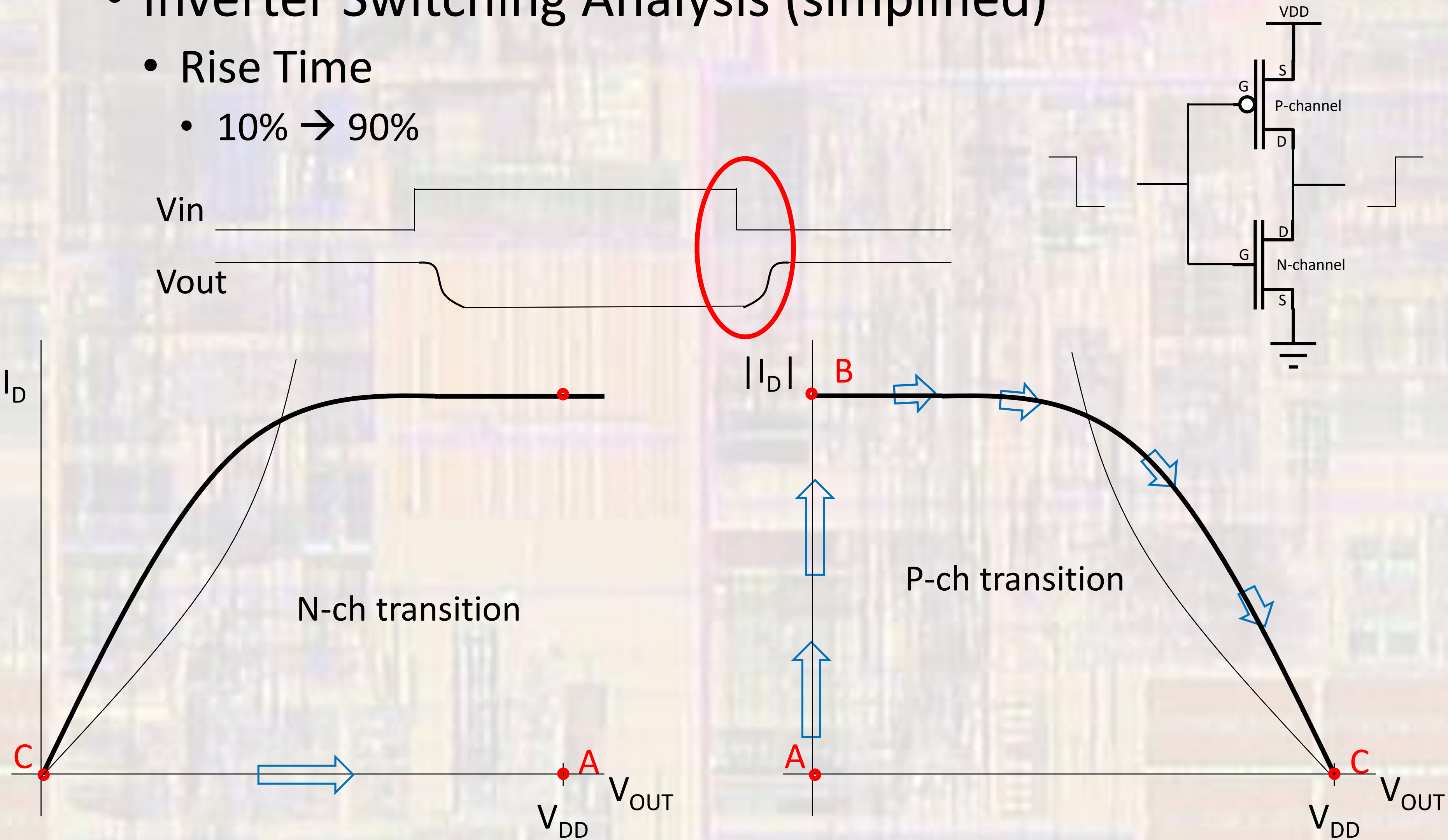
$$t_f = 30.6\times10^3 \times 1pF\,\frac{100n}{1000n}\left(\frac{\sec}{F}\right) = 3.06ns$$





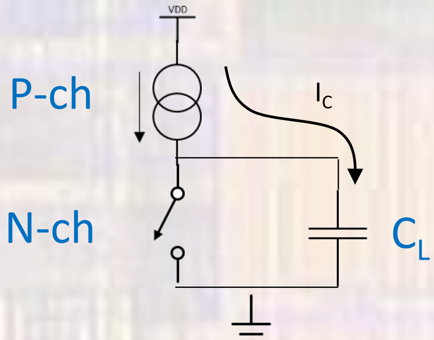
CMOS Inverter

- Inverter Switching Analysis (simplified)
  - Rise Time
    - 10% → 90%



CMOS Inverter

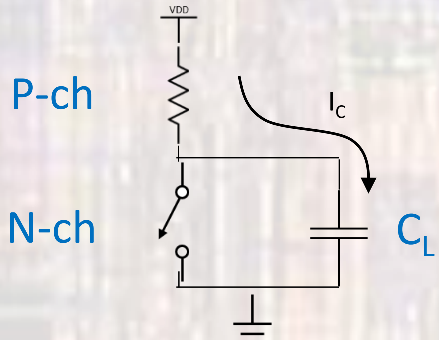
- Inverter Switching Analysis (simplified)
  - Rise Time



Saturation

$$C_L \frac{dV_o}{dt} + \frac{\beta_p}{2}\left(V_{DD} - V_{Tp}\right)^2 = 0$$

$$V_o \geq V_{DD} - V_{Tp}$$



Linear

$$C_L \frac{dV_o}{dt} + \beta_p\left[\left(V_G - V_{Tp}\right)V_D - V_D^{\,2}/2\right] = 0$$

$$V_o < V_{DD} - V_{Tp}$$

CMOS Inverter

- Inverter Switching Analysis (simplified)
  - Rise Time
    - Integrating over the appropriate times

$$t_r = 2\frac{C_L}{\beta_p(V_{DD} - |V_{Tp}|)} \times \left[\frac{|V_{Tp}| - 0.1 \times V_{DD}}{V_{DD} - |V_{Tp}|} + \frac{1}{2}\ln\left(\frac{19 \times V_{DD} - 20 \times |V_{Tp}|}{V_{DD}} \right) \right]$$

    - With V_{Tp}=0.45V and V_{DD}=1.2V

$$t_r = 8.44\frac{C_L}{\beta_p}\left(\frac{1}{Volts}\right)$$

$$t_r = 61.2 \times 10^3 \times C\frac{L}{W}\left(\frac{\sec}{F}\right)$$

$$\beta = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)$$

$$\mu_p = 100cm^2 / V - \sec$$
$$\varepsilon_{Si} = 3.9\varepsilon_0 = 3.9 \times 10^{-14} F / cm$$
$$t_{ox} = 5nm$$

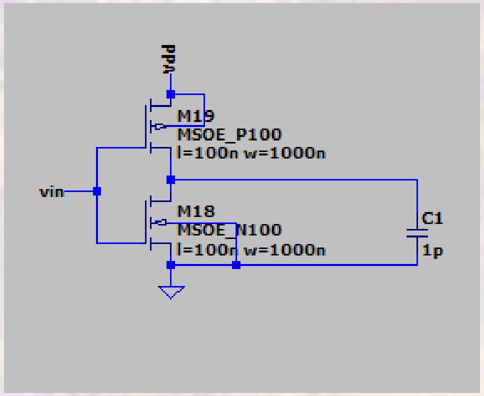
$$\beta_p = \frac{W}{L} \times 69\mu A / V^2$$

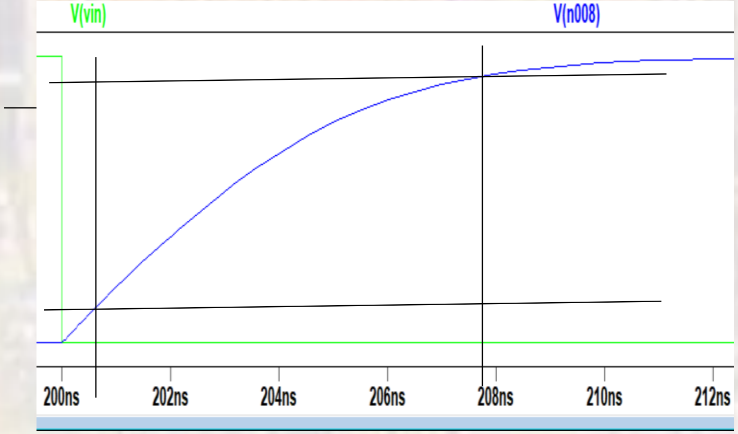
CMOS Inverter

- Inverter Switching Analysis (simplified)
  - Fall Time

$$t_r = 61.2 \times 10^3 \times C \frac{L}{W}\left(\frac{\sec}{F}\right)$$

$$t_r = 61.2 \times 10^3 \times 1pF \frac{100n}{1000n}\left(\frac{\sec}{F}\right) = 6.12ns$$

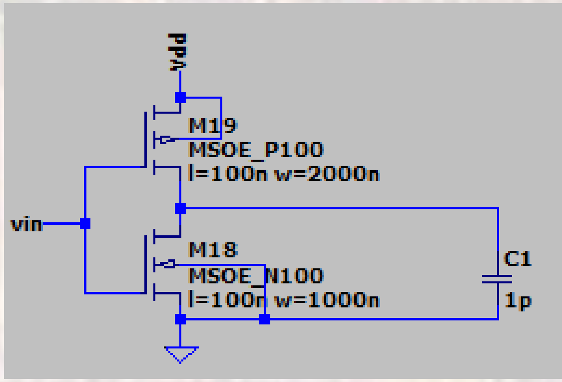




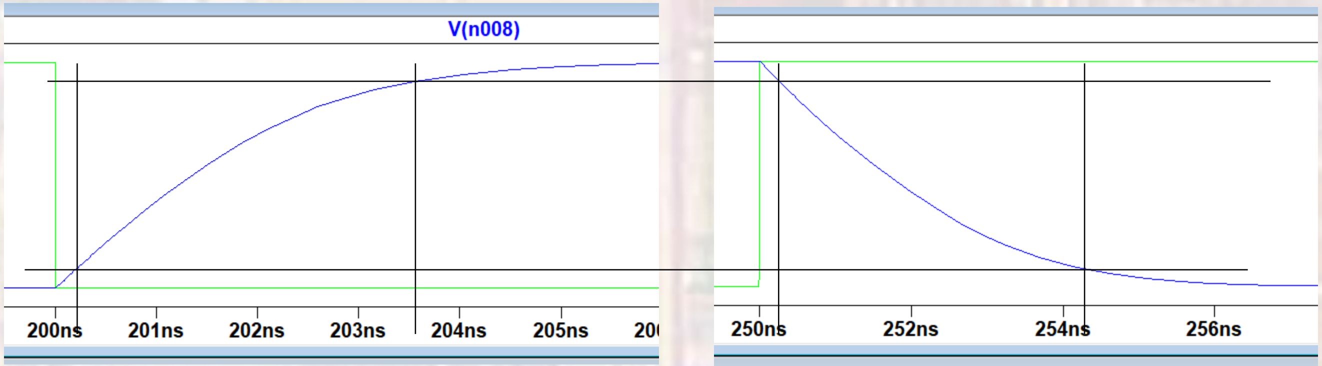
CMOS Inverter

- Inverter Switching Analysis (simplified)
  - W/L scaling

$$t_r = 61.2\times10^3 \times C\frac{Lp}{Wp}\left(\frac{\sec}{F}\right) \qquad t_f = 30.6\times10^3 \times C\frac{Ln}{Wn}\left(\frac{\sec}{F}\right)$$



  - Assuming Ln=Lp=Lmin
  - Scale Wp = 2xWn
  - `



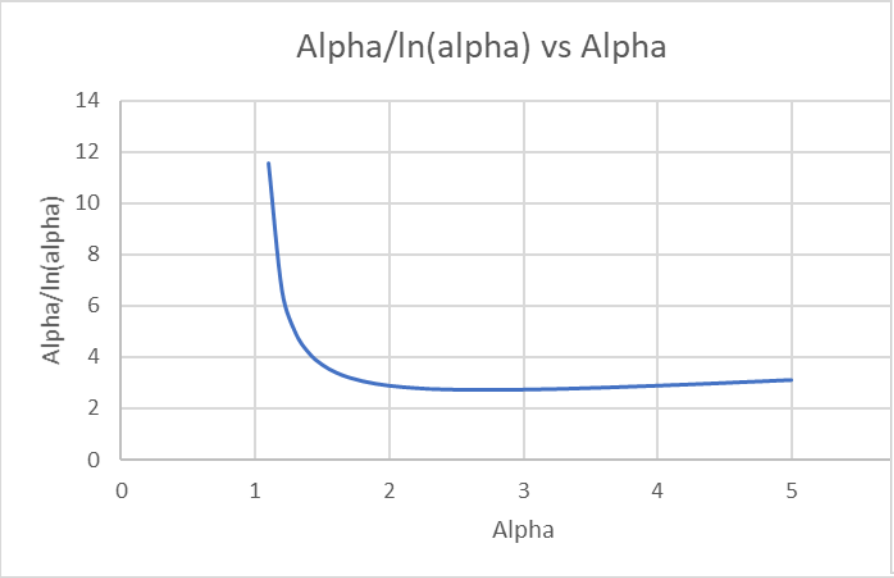
CMOS Inverter

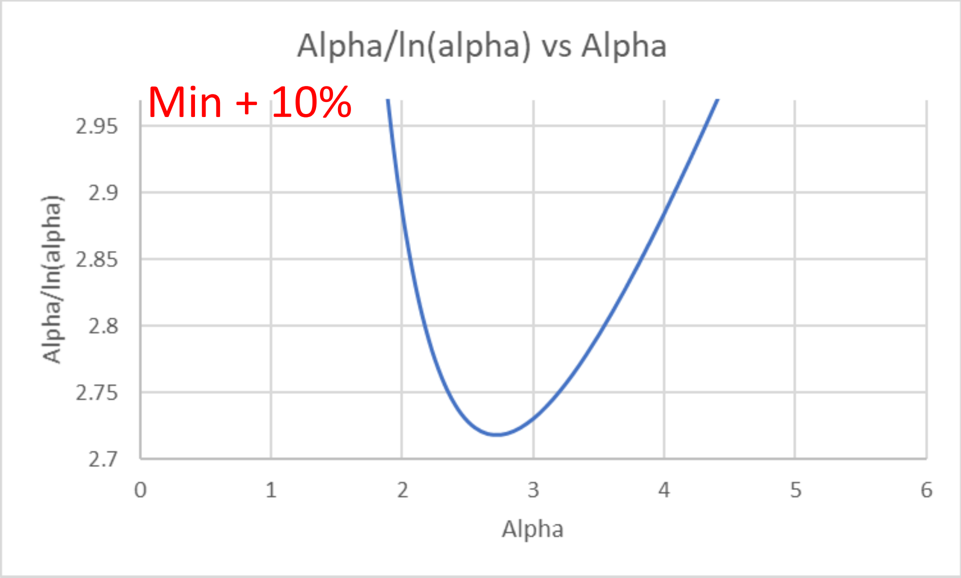
- Driving large loads
  - Assume the delay of a minimum inverter driving another minimum inverter is τ
  - We expect the delay of an inverter driving an inverter α times the first to be $\alpha\tau$
  - The delay of N stages of progressively growing inverters would be $N\alpha\tau$

  - The input capacitance for the inverters it C_G
  - Driving a large capacitance C_L
    - $Y = C_L / C_G = \alpha^N$
    - Bigger α → smaller N, …
    - $\ln(Y) = N\ln(\alpha)$
  - $N\alpha\tau = [\ln(Y)/\ln(\alpha)]\ \alpha\ \tau = \ln(Y)\ \tau\ [\alpha / \ln(\alpha)]$

CMOS Inverter

- Driving large loads
  - $N\alpha\tau = [\ln(Y)/\ln(\alpha)]\ \alpha\ \tau = \ln(Y)\ \tau\ [\alpha / \ln(\alpha)]$
  - Minimizing by taking the derivative → $\alpha = e = 2.71$
  - Plotting wrt α





CMOS Inverter

- Driving large loads
  - Typically scale by 2.7x – 4x
  - 2.7x → minimum delay
  - 4x → <10% delay penalty + area savings

    - $Y = C_L / C_G = \alpha^N = 256$
    - $\alpha = 2.7$: $N = \ln(Y)/\ln(\alpha) = 5.54$
    - 1A + 2.7A + 7.29A + 19.68A + 53.14 + 77.47* = 161.28A
    - $\alpha = 4$: $N = \ln(Y)/\ln(\alpha) = 4$
    - 1A + 4A + 16A + 64A = 85A