Gain Stages

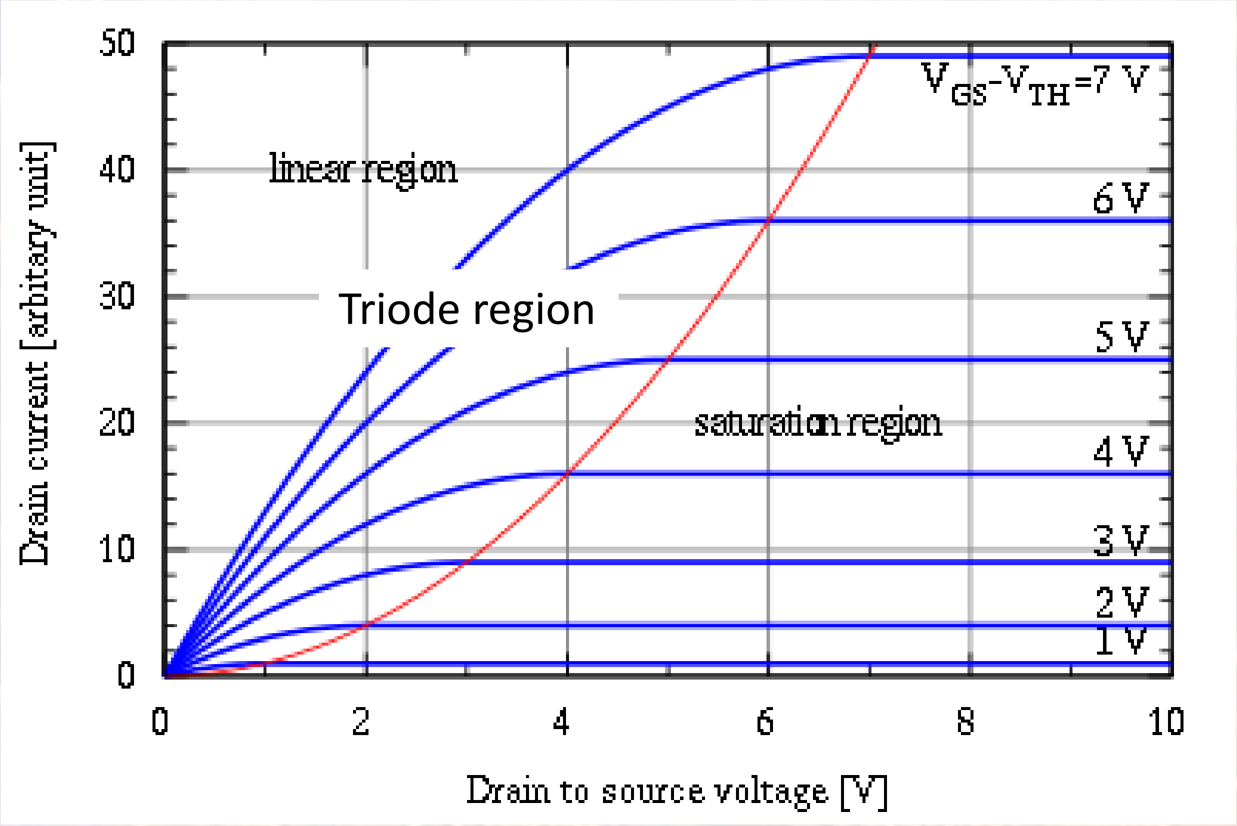
Last updated 4/7/19

Gain Stages

- Threshold Voltage
  - Gate voltage V_{GS} that first allows conduction from source to drain
  - Function of Silicon processing

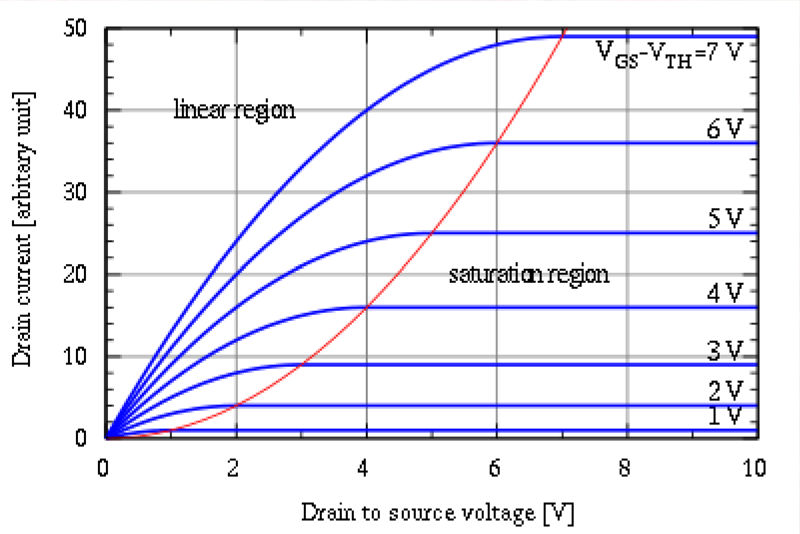
Gain Stages

- Large Signal Analysis
  - $V_{GS} - V_{TH}$: over voltage



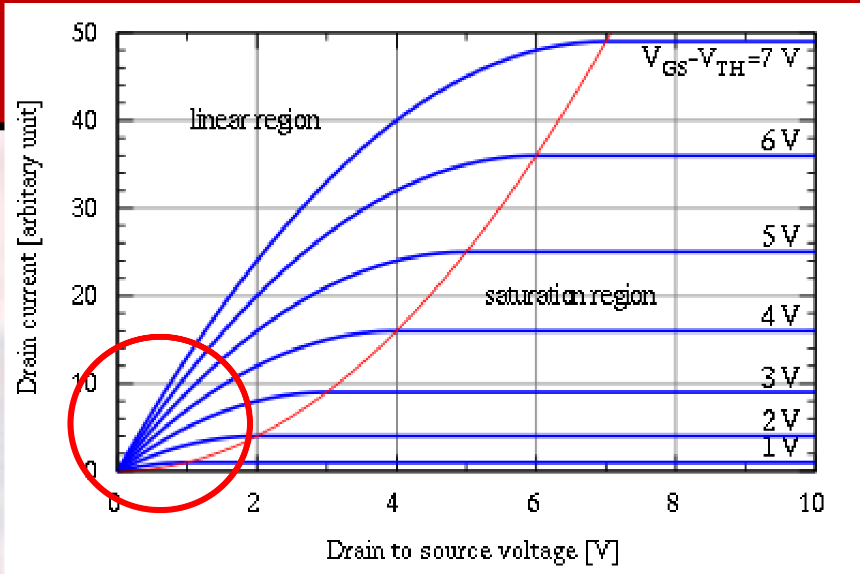
Gain Stages

- Large Signal Analysis
  - Linear (Triode) Region
  - $V_{GS} > V_{TH}$
  - $V_{DS} < V_{GS} - V_{TH}$



$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - {V_{DS}}^2 \big/ 2\right]$$

Gain Stages



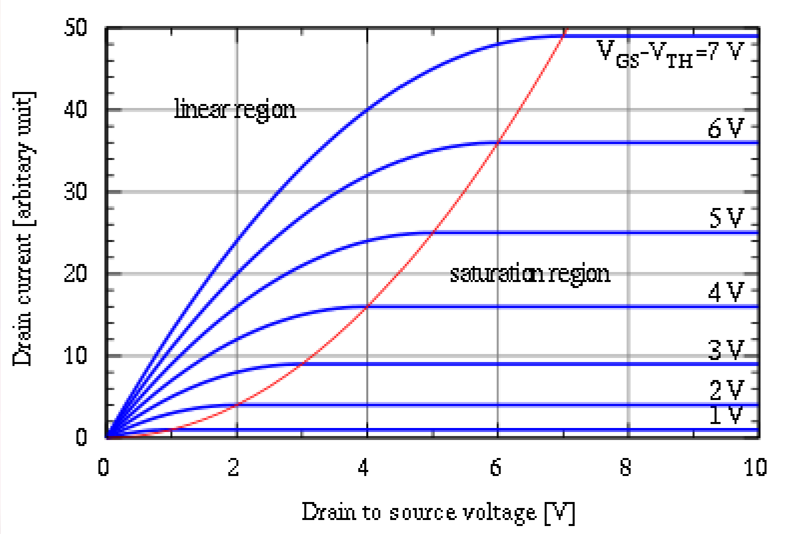
- Large Signal Analysis
  - Linear (Triode) Region
  - $V_{DS} << V_{GS} - V_{TH}$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{TH}\right)V_{DS}\right]$$

$$R_{EQ} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

Gain Stages

- Large Signal Analysis
  - Onset of Saturation
  - $V_{DS} = V_{GS} - V_{TH}$



$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

Gain Stages

- MOS Transconductance
  - Transconductance

$$\frac{\partial I}{\partial V}$$

  - MOS Transconductance
    - In Saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

$$g_m = \frac{\partial_{ID}}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)$$

units
1/Ω

Gain Stages

- MOS Transconductance

$$g_m = \frac{\partial_{ID}}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)$$

- with substitutions

50uA/V^2(5/0.1)(300mV) = 750x10^{-6} /Ω

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$$

(2x112uA)/300mV = 750x10^{-6} /Ω

Gain Stages

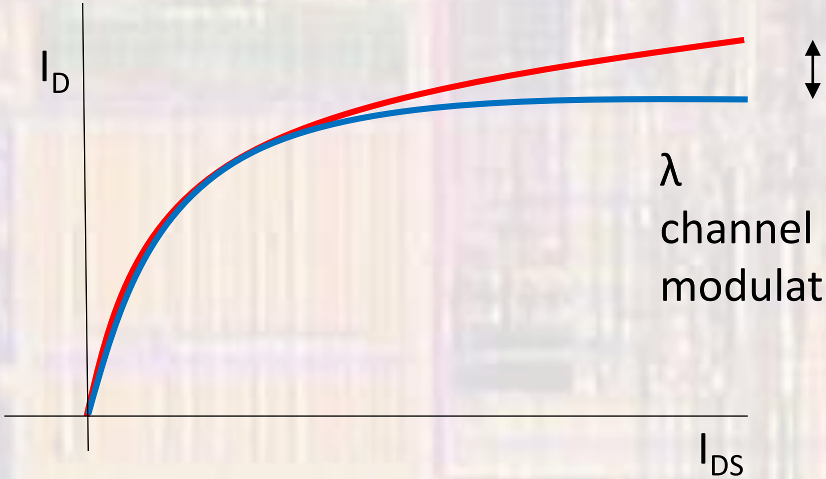
- Non-Ideal Effects
  - Body Effect

  - Assuming the body/s/d junctions remain reverse biased the device will continue to operate – but with different threshold voltage characteristics

  - $V_{TH} = V_{TH0} + \Upsilon(\ldots V_{BS} \ldots)$

Gain Stages

- Non-Ideal Effects
  - Channel Length Modulation



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda V_{DS}\right)$$

Gain Stages

- Non-Ideal Effects
  - Subthreshold Conduction
    - Current conduction with V_{GS} below V_{TH}
    - Called weak inversion

$$I_D = I_o \exp \frac{V_{GS}}{\xi V_T}$$

$$\xi > 1$$

Gain Stages

- Small Signal Model

$$I_D = g_m V_{GS}$$

$$r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\frac{\partial I_D}{\partial V_{GS}}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \bullet \lambda} = \frac{1}{\lambda I_D}$$

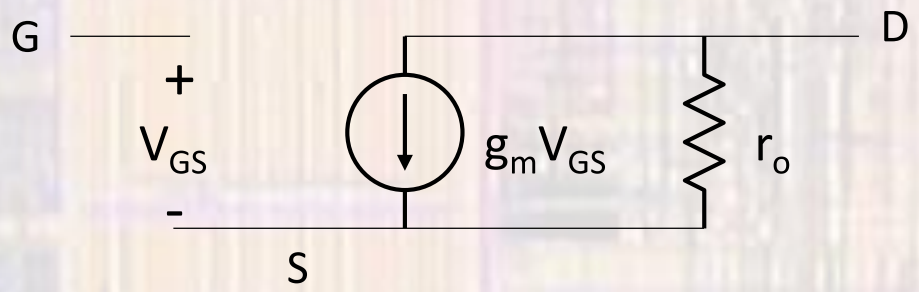
1/(0.1x112uA) = 89KΩ

typically $\frac{1}{g_m} << r_o$

1.3KΩ << 89KΩ

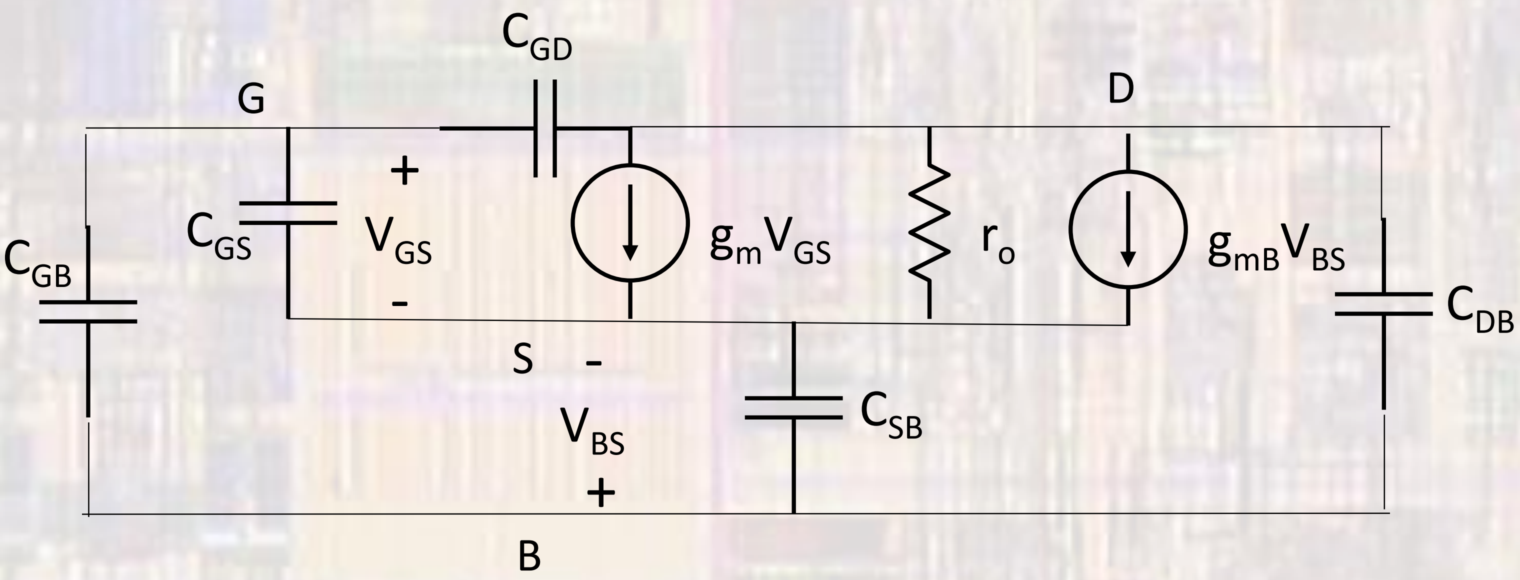
Gain Stages

- Small Signal Model



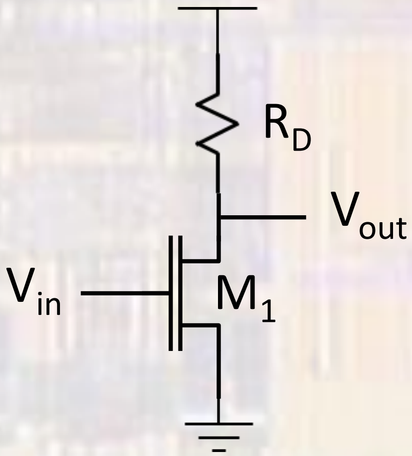
Gain Stages

- Small Signal Model



Gain Stages

- Common Source – Resistive Load



Linear Operation

$M_1 \rightarrow R_{eq}$

$$V_{out} = V_{DD}\frac{R_{eq}}{R_{eq} + R_D}$$

$$V_{out} = \frac{V_{DD}}{1 + R_D \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})}$$

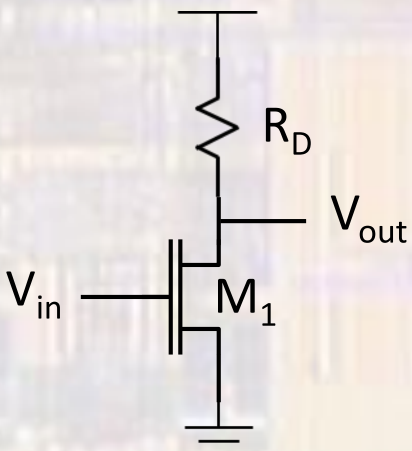
$$A_v = \frac{\partial Vout}{\partial Vin}$$

$$A_v = -R_D \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})$$

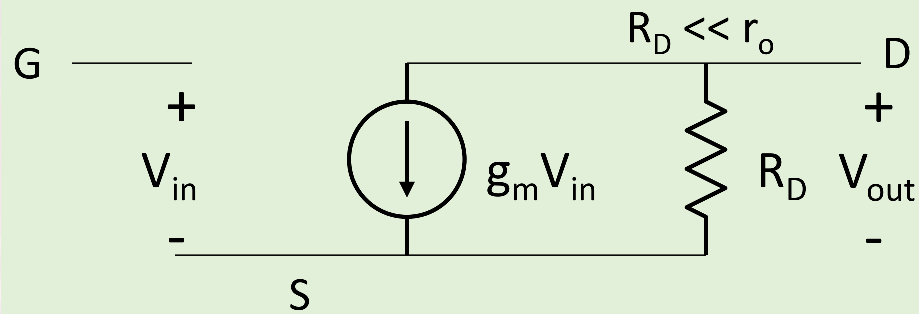
$$A_v = -g_m R_D$$

Gain Stages

- Common Source – Resistive Load



Saturation
Small signal model



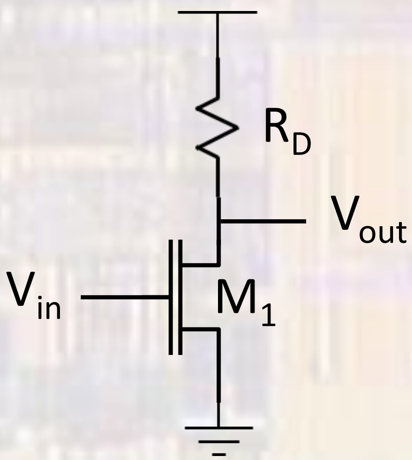
$$A_v = \frac{\partial Vout}{\partial Vin}$$

$$A_v = -g_m R_D$$

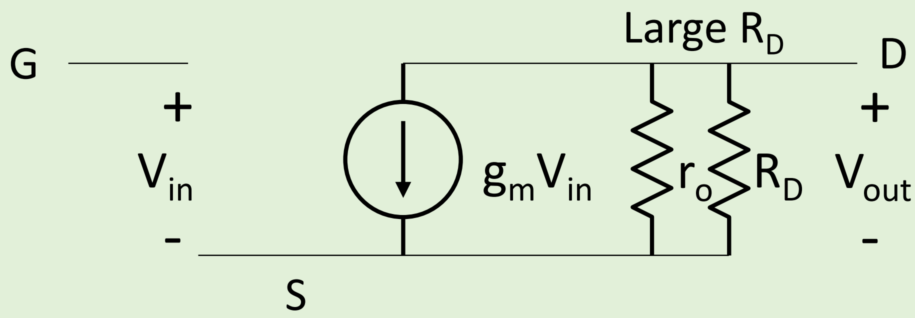
$Av = -(750 \times 10^{-6}/\Omega) \times 10K\Omega = -7.5$

Gain Stages

- Common Source – Resistive Load



Saturation
Small signal model



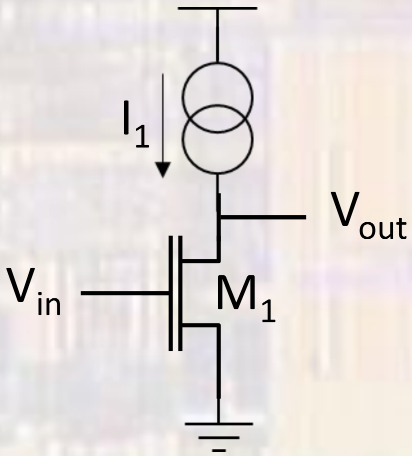
$$A_v = \frac{\partial Vout}{\partial Vin}$$

$$A_v = -g_m \frac{r_o R_D}{r_o + R_D}$$

Av = -(750x10^{-6}/Ω)x(10KΩ|| 90KΩ) = -6.75

Gain Stages

- Common Source – Current Source Load
  - Saturation



$$A_v = -g_m \frac{r_o R_D}{r_o + R_D}$$

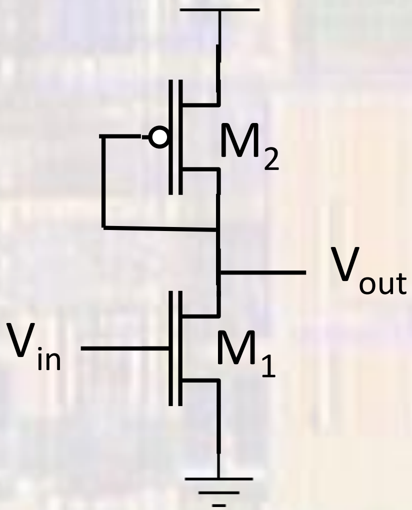
$$R_D \to \infty$$

$$A_v = -g_m r_o$$

Av = -(750x10^{-6}/Ω)x90KΩ = -67.5

Gain Stages

- Common Source – Diode Connected Load



$$I_{D_{M1}} = \frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}\left(V_{in} - V_{TH_n}\right)^2 =$$

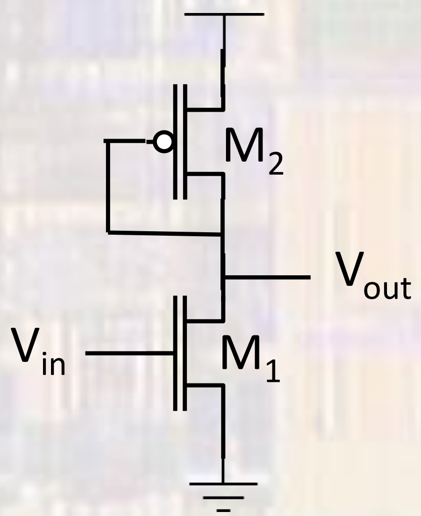
$$I_{D_{M2}} = -\frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}\left(V_{out} - V_{DD} - V_{TH_p}\right)^2$$

$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} = \frac{\left|V_{GS_2} - V_{TH_2}\right|}{V_{GS_1} - V_{TH_1}}$$

Vdd = 1.2V, vout = Vdd/2, vin = 0.5V
Av = |-0.6+0.3|/(0.5 – 0.3) = -1.5

Gain Stages

- Common Source – Diode Connected Load



$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} = \frac{\left|V_{GS_2} - V_{TH_2}\right|}{V_{GS_1} - V_{TH_1}}$$

for a gain of 5

$\mu_n = 2\ \mu_p$

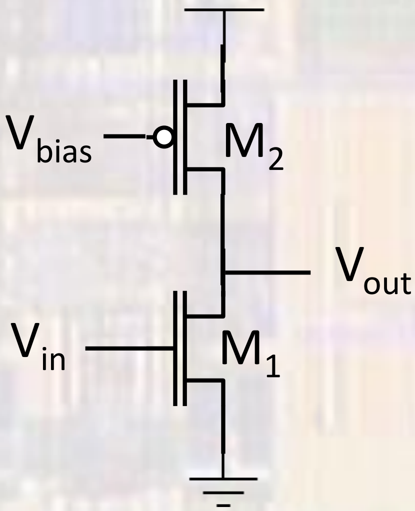
→ $(W/L)_n = 12.5(W/L)_p$

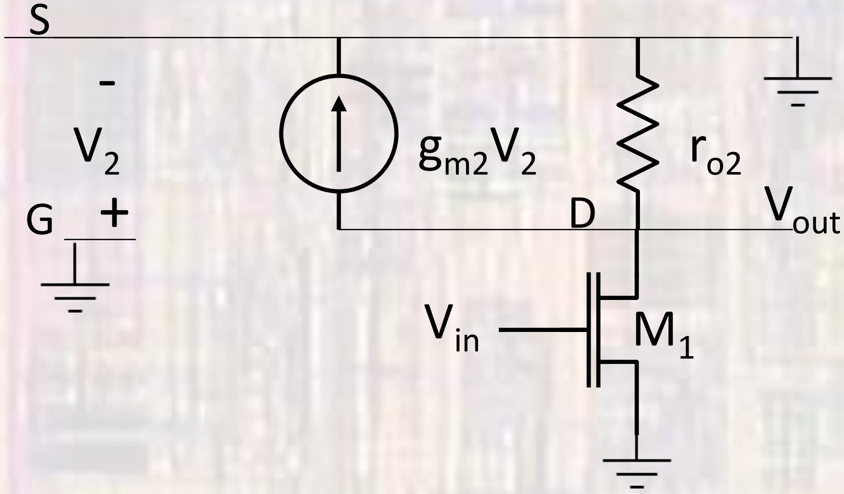
and

$$\left|V_{GS_2} - V_{TH_2}\right| = 5 \times (V_{GS_1} - V_{TH_1})$$

Gain Stages

- Common Source – Current Source Load



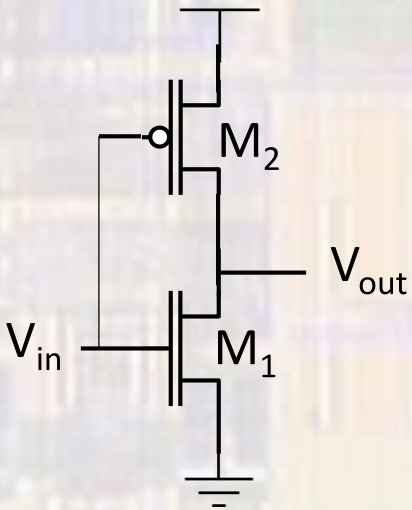


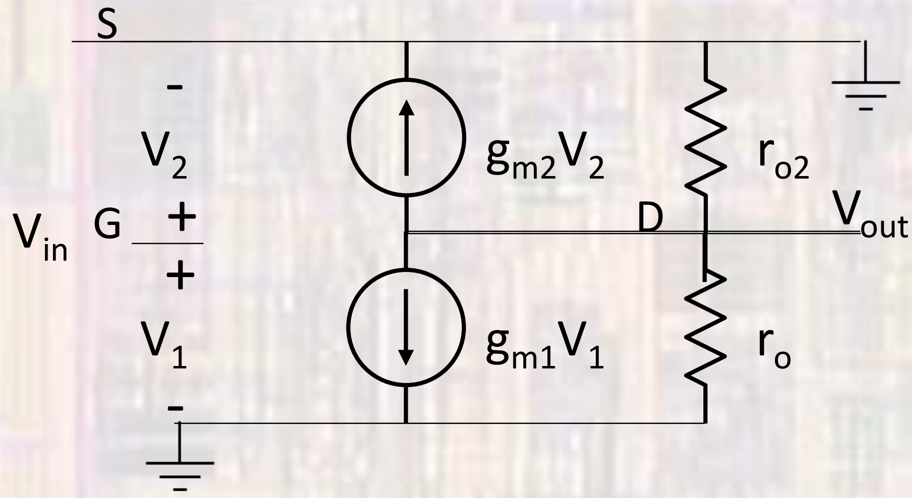
$$A_v = -g_{m1}(r_{o1} \| r_{o2})$$

Av = -(750x10^{-6}/Ω)x(90KΩ||90KΩ) = -33.7

Gain Stages

- Common Source – Active Load



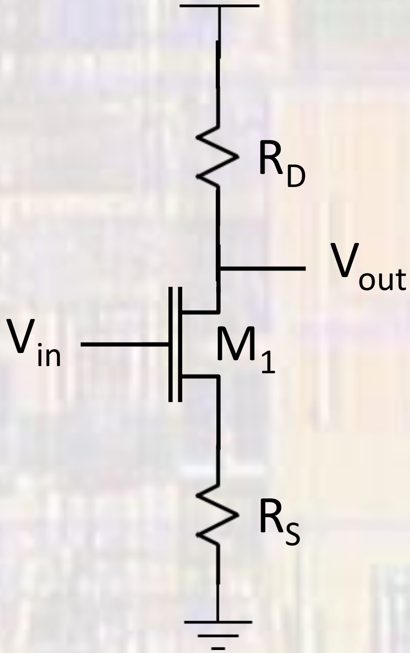


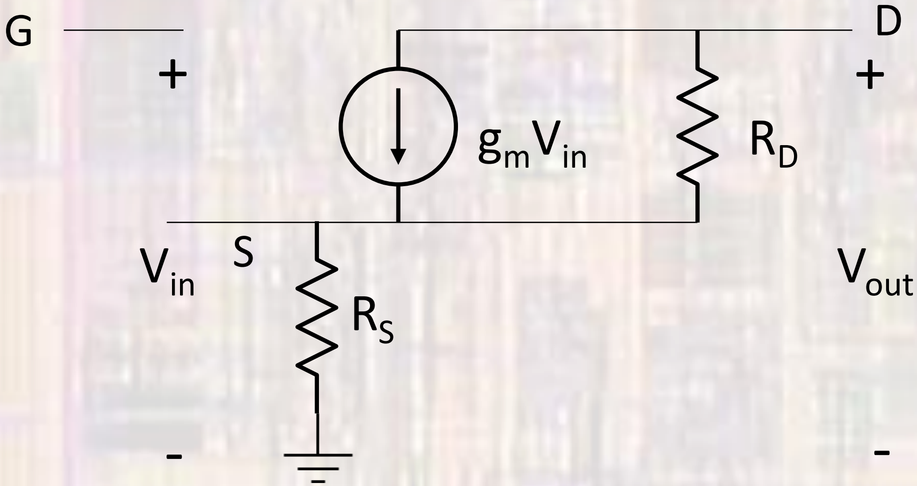
$$A_v = -(g_{m1} + g_{m2})(r_{o1} \| r_{o2})$$

Av = -(750x10^{-6}/Ω+ 375x10^{-6}/Ω)x(90KΩ||90KΩ) = -50.6

Gain Stages

- Common Source – Source Degeneration



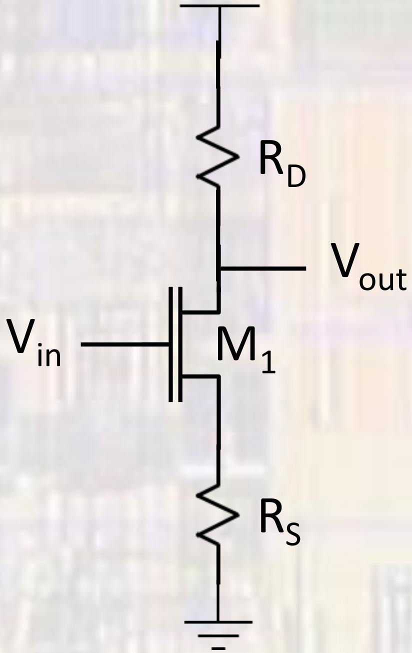


$$A_v = \frac{-g_m R_D}{1 + g_m R_S}$$

Av = -(750x10^{-6}/Ω)x10KΩ/(1 + (750x10^{-6}/Ω)x500Ω) = -5.4

Gain Stages

- Common Source – Source Degeneration
  - Increase in effective transistor output resistance
    - R_S is seen through the transistor

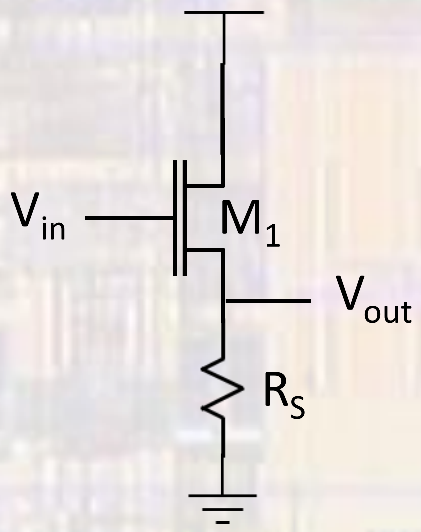


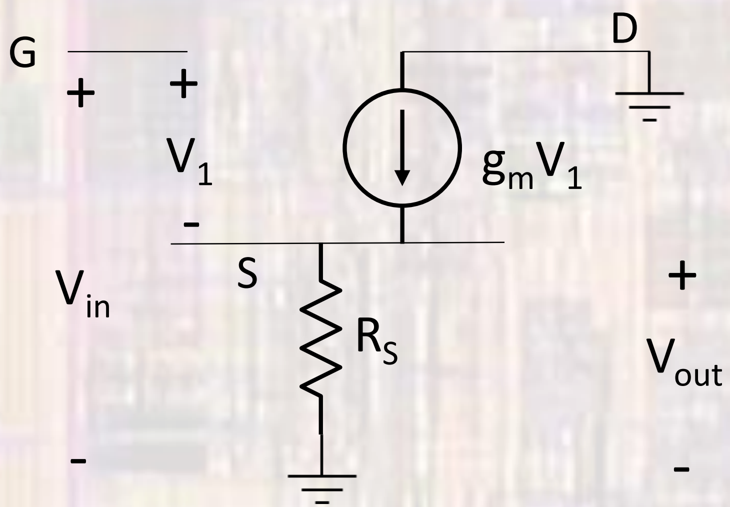
$$r_{out} = [1 + g_m R_S] r_o$$

r_{out} = [1 + 750x10^{-6}/Ωx500Ω]x90KΩ) = 124KΩ

Gain Stages

- Source Follower



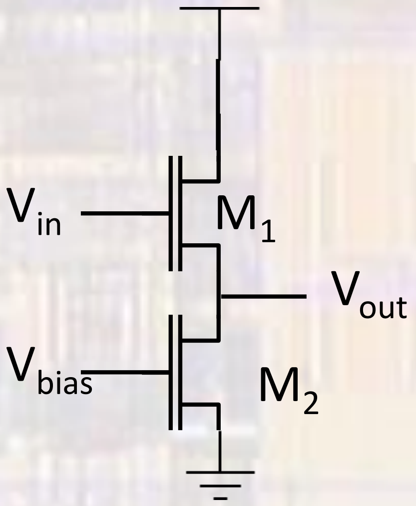


$$A_v = \frac{g_m R_S}{1 + g_m R_S}$$

Av = $(750 \times 10^{-6}/\Omega) \times (10K\Omega)/(1 + (750 \times 10^{-6}/\Omega) \times (10K\Omega)) = 0.88$

Gain Stages

- Source Follower – active load

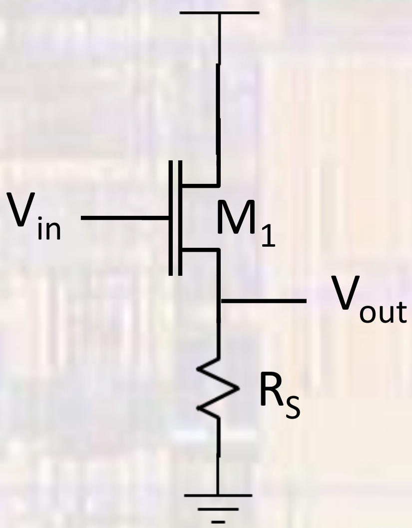


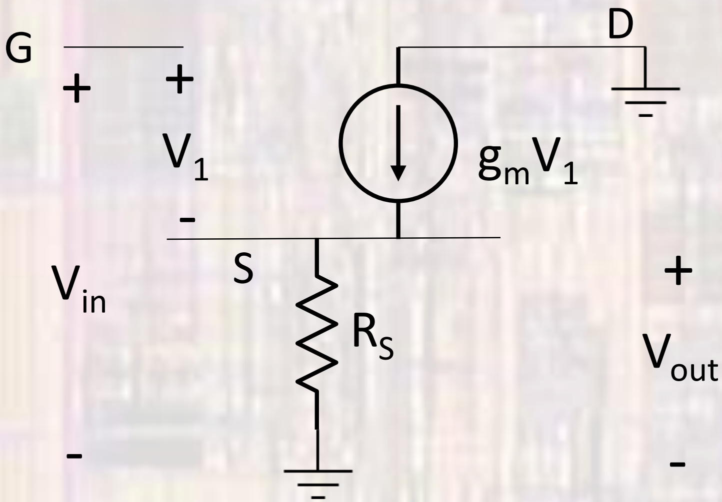
$$A_v = \frac{g_m R_{eq}}{1 + g_m R_{eq}}$$

$$R_{eq} = \frac{1}{g_{mB}} \parallel r_{o1} \parallel r_{o2}$$

Gain Stages

- Source Follower
  - Relatively low output impedance



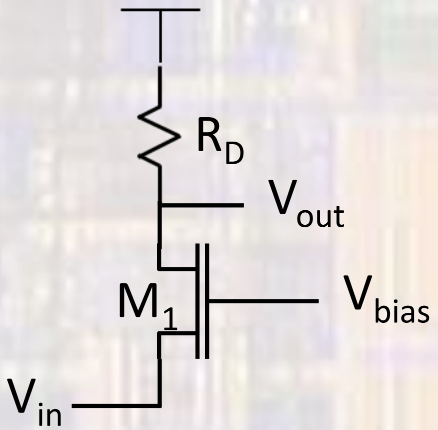


$r_o = 1/g_m$

$ro = 1/(750x10^{-6}/\Omega) = 1.33K\ \Omega$

Gain Stages

- Common Gate Stage



$$I_{D_{M1}} = \frac{1}{2}\mu_n C_{ox} \frac{W_n}{L_n}\left(V_{Bias} - V_{in} - V_{TH_n}\right)^2$$

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox} \frac{W_n}{L_n}\left(V_{Bias} - V_{in} - V_{TH_n}\right)^2 R_D$$

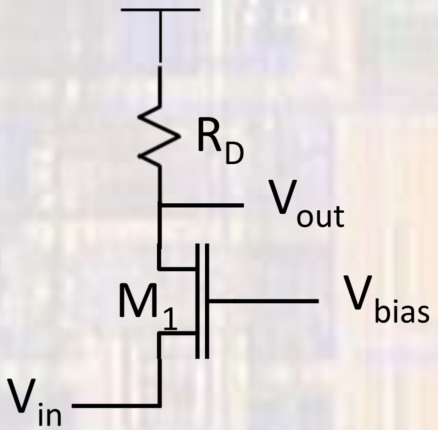
$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox} \frac{W_n}{L_n}\left(V_{Bias} - V_{in} - V_{TH_n}\right)^2 \left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right) R_D$$

$$\frac{\partial V_{out}}{\partial V_{in}} = g_m (1+\eta) R_D$$

positive

Gain Stages

- Common Gate Stage

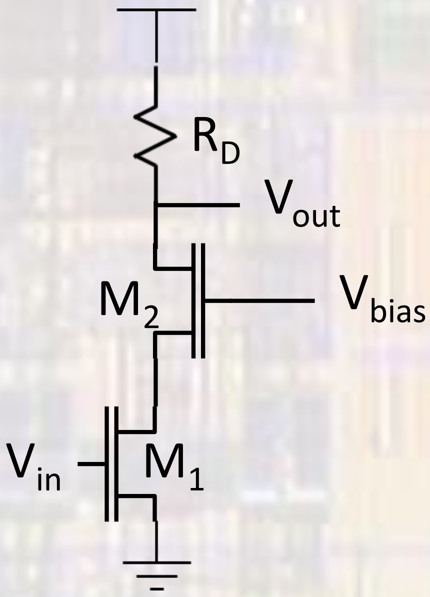


$$R_{in} = \frac{1}{\frac{1}{r_o} + g_m + g_{mb}}$$

$R_{in} = 1/(750\text{x}10^{-6}/\Omega + 400\text{x}10^{-6}/\ \Omega\ \ + 1/90\text{K}\Omega\ ) = 861\Omega$

Gain Stages

- Cascode Stage



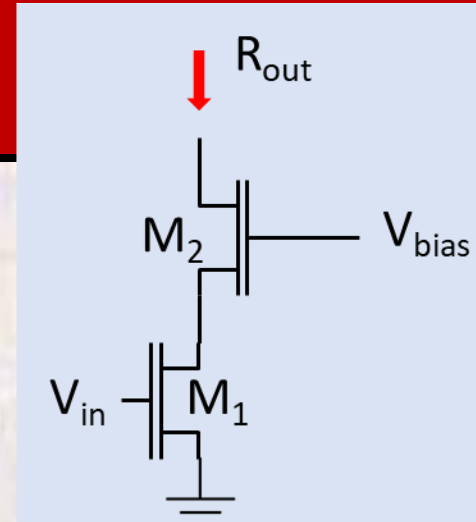
$$A_v = -g_m R_D$$

M2 passes the current through

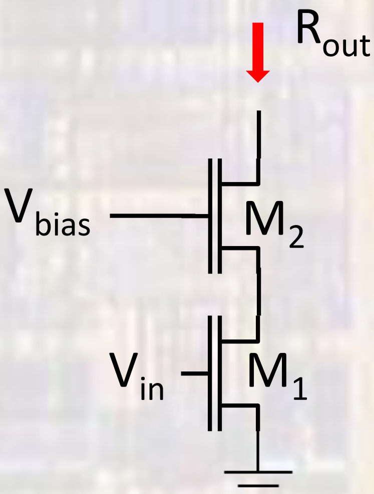
$$R_{out} = [1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o1} + r_{o2}$$

looks like common source with r_{o2} degeneration

Gain Stages



- Cascode Stage



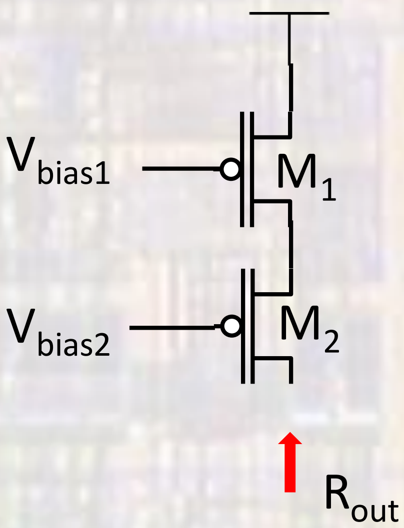
$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1} + r_{o2}$$

looks like common source with r_{o2} degeneration

R_{out} = [1+(750x10^{-6}/Ω + 400x10^{-6}/ Ω)90KΩ] 90KΩ + 90KΩ = 9.5MΩ

Gain Stages

- Cascode Load

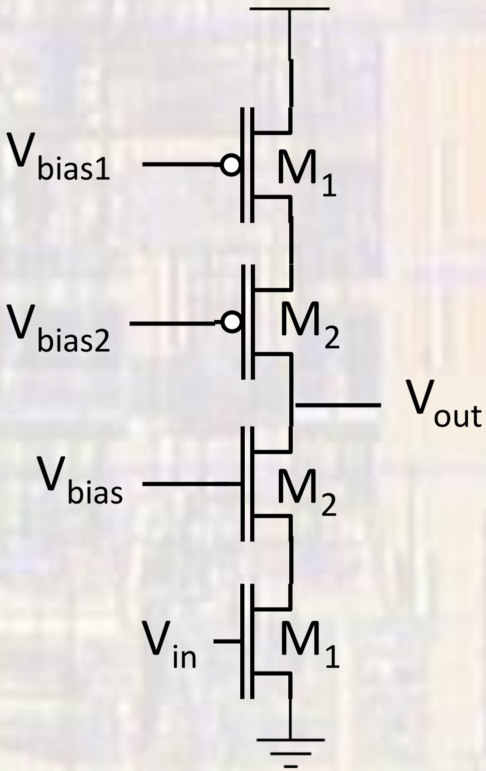


$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1} + r_{o2}$$

looks like common source with r_{o2} degeneration

Gain Stages

- Cascode Amplifier

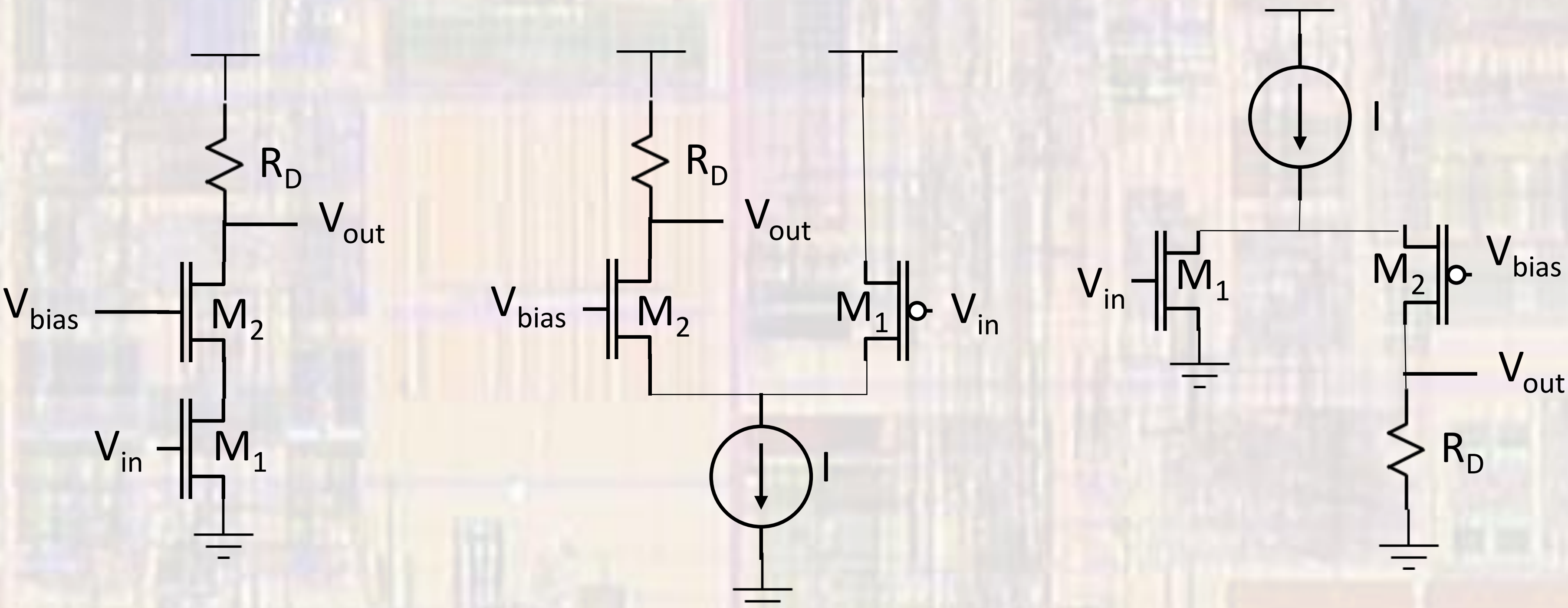


$$A_v = -g_{m1}[(g_{m2}r_{o2}r_{o1}) \| (g_{m3}r_{o3}r_{o4})]$$

A_v = -750x10^{-6}/Ω [(750x10^{-6}/Ωx90KΩx90KΩ)||(400x10^{-6}/Ωx90KΩx90KΩ)]
= 1587

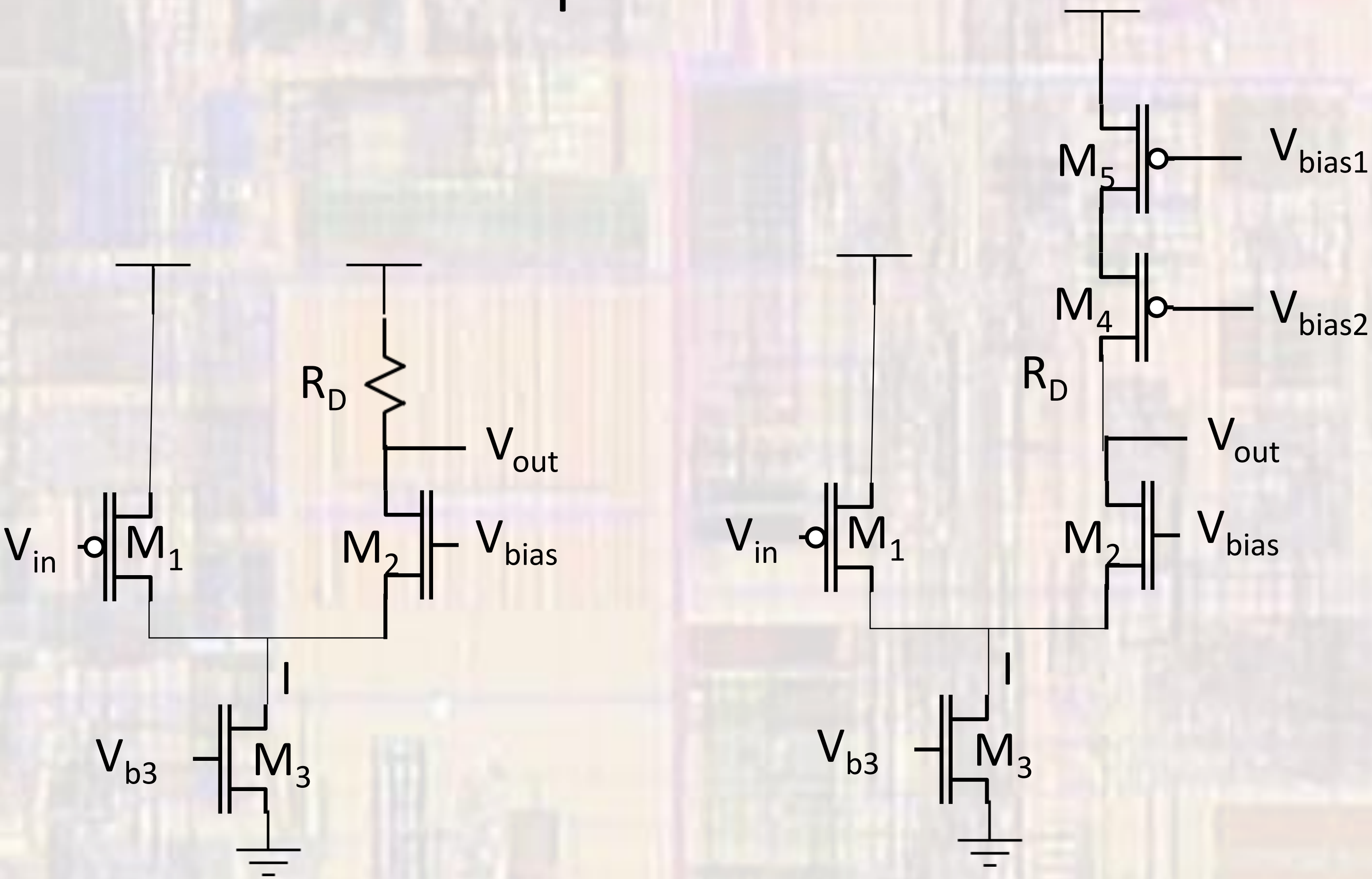
Gain Stages

- Folded Cascode Amplifier



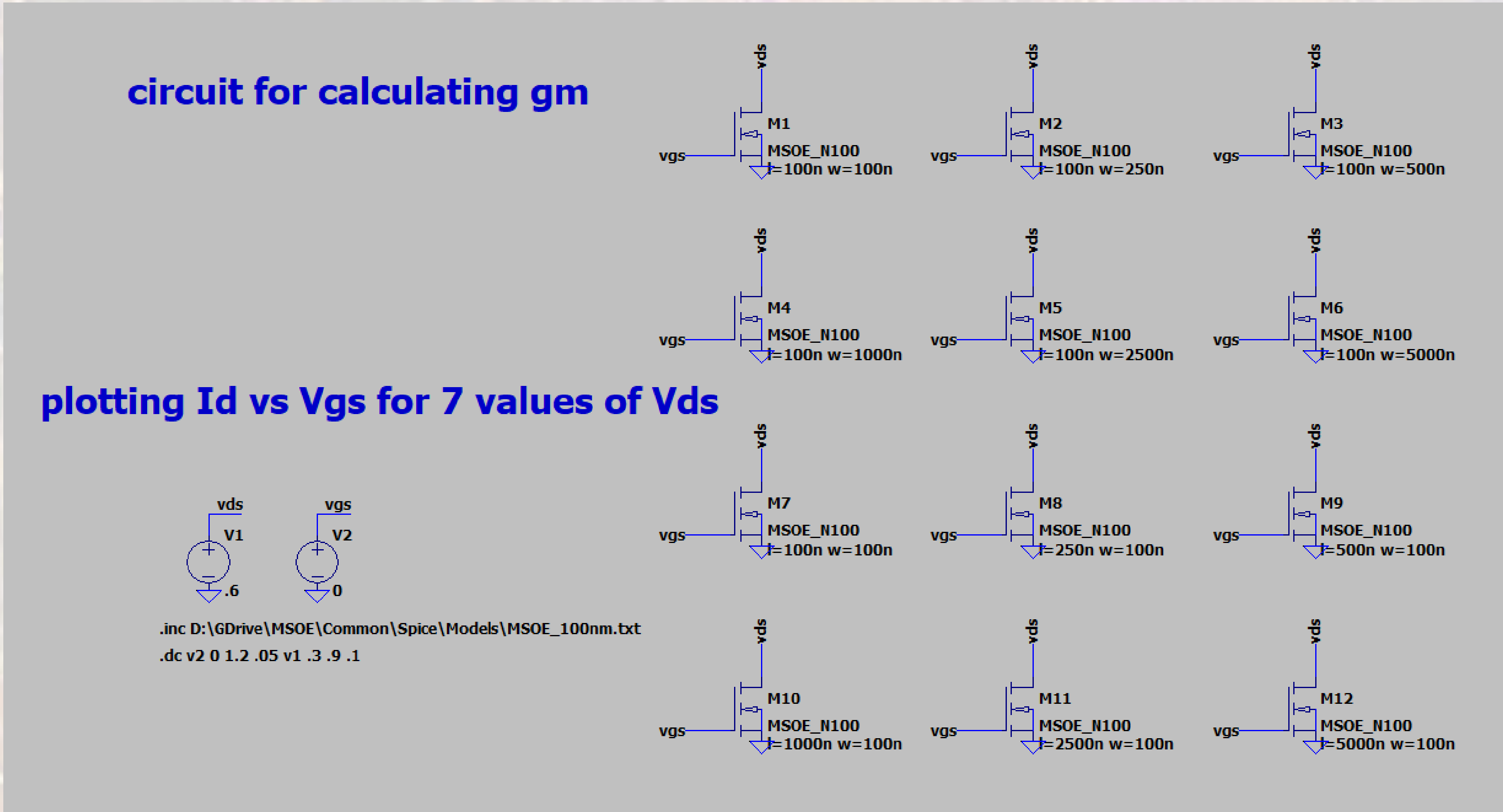
Gain Stages

- Folded Cascode Amplifier



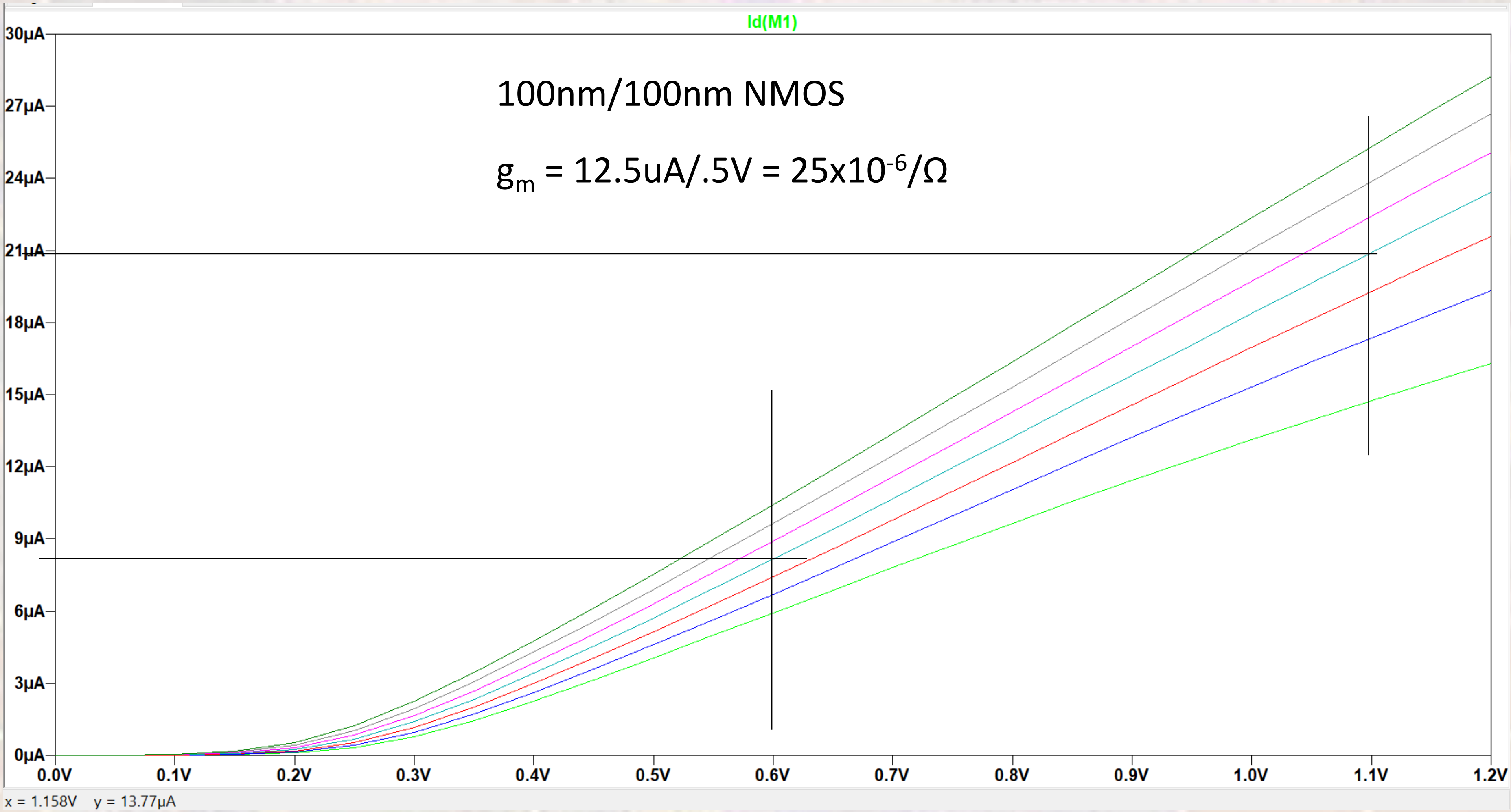
Gain Stages

- Simulating g_m

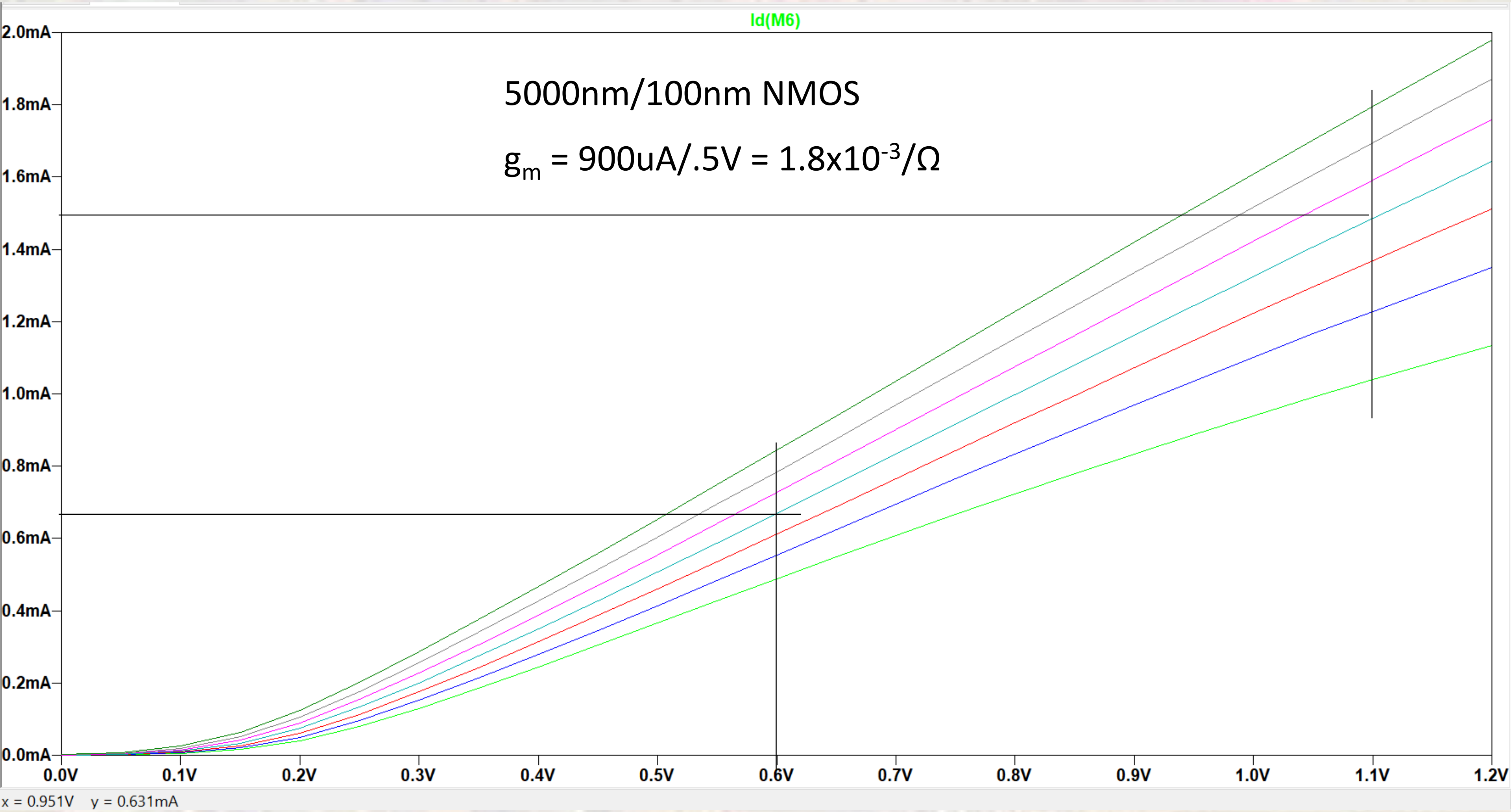


Gain Stages

- Simulating g_m



Gain Stages



Id(M6)
5000nm/100nm NMOS
g_m = 900uA/.5V = 1.8x10^{-3}/Ω
2.0mA
1.8mA
1.6mA
1.4mA
1.2mA
1.0mA
0.8mA
0.6mA
0.4mA
0.2mA
0.0mA
0.0V
0.1V
0.2V
0.3V
0.4V
0.5V
0.6V
0.7V
0.8V
0.9V
1.0V
1.1V
1.2V
x = 0.951V y = 0.631mA

Gain Stages

- Simulating g_m