EE4981 - Lab W4: Inverter Delay Characteristics

1 week total

Goals:

1. Validate simple inverter electrical characteristics
2. Use schematic design hierarchy
3. Drive a large capacitive load

Assignment Description:

Overview:

Optimize an inverter design for the MSOE_100 technology node

Part 1: Design a minimum delay inverter with a fanout of 4

Min L for both N and P channel devices is 100nm

Min W for both N and P channel devices is 250nm

Optimize for minimum switching speed with symmetrical rise and fall delays

Part 2: Design a ring oscillator (no need to create output circuitry

Use your inverter from part 1

Minimum number of inverters is 99

Determine the maximum frequency of operation

Part 3: Design an inverter chain to drive a large capacitive load

The load is equivalent to 1024 inverters from part 1

Optimize your design for switching delay

Determine the switching delay

Deliverables:

Schematics

Simulation plots

Table of results

Hardcopy – no need to put into a PowerPoint or pdf, just print/label/staple

Due: Lab week 5