EE4981 - Lab W5: Layouts

1 week total

Goals:

1. Create some small gate layouts
2. Use the Micro Magic tool
3. Plot from GDSPlot

Assignment Description:

Overview:

Develop the beginning of a cell library in MicroMagic

Part 1: Design a minimum sized inverter cell

Note: you will need to live with the cell height for parts 2 and 3

Inputs and outputs on metal 2 – no other metal 2

Part 2: Design a minimum inverter cell with matched rise and fall times

Part 3: Design either a 4 input nand gate or 4 input nor gate

Deliverables:

Layout plots (8-1/2 x 11) ok – color (available in the library)

Picture of the DRC rule run (clean)

Due: Lab week 6