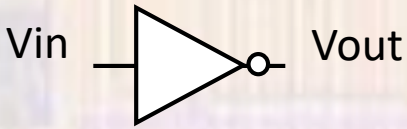
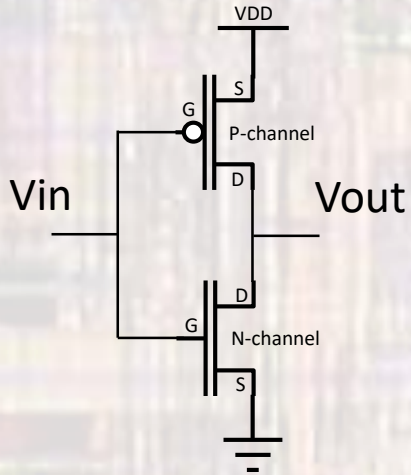
CMOS Logic Gates

Last updated 3/25/19

Logic Gates

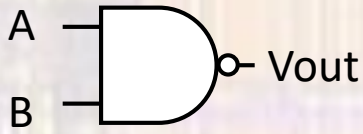
- Inverter Circuit

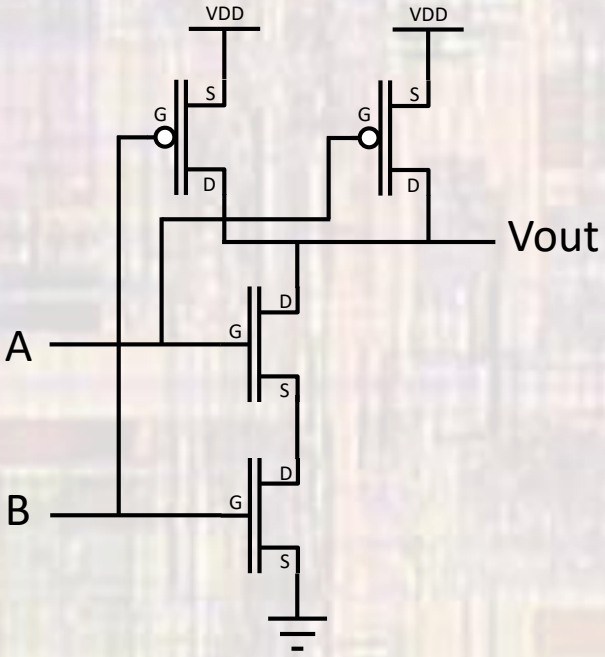




Logic Gates

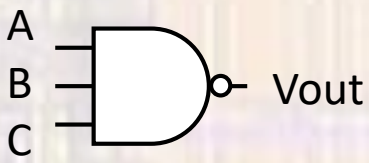
- Nand Gate

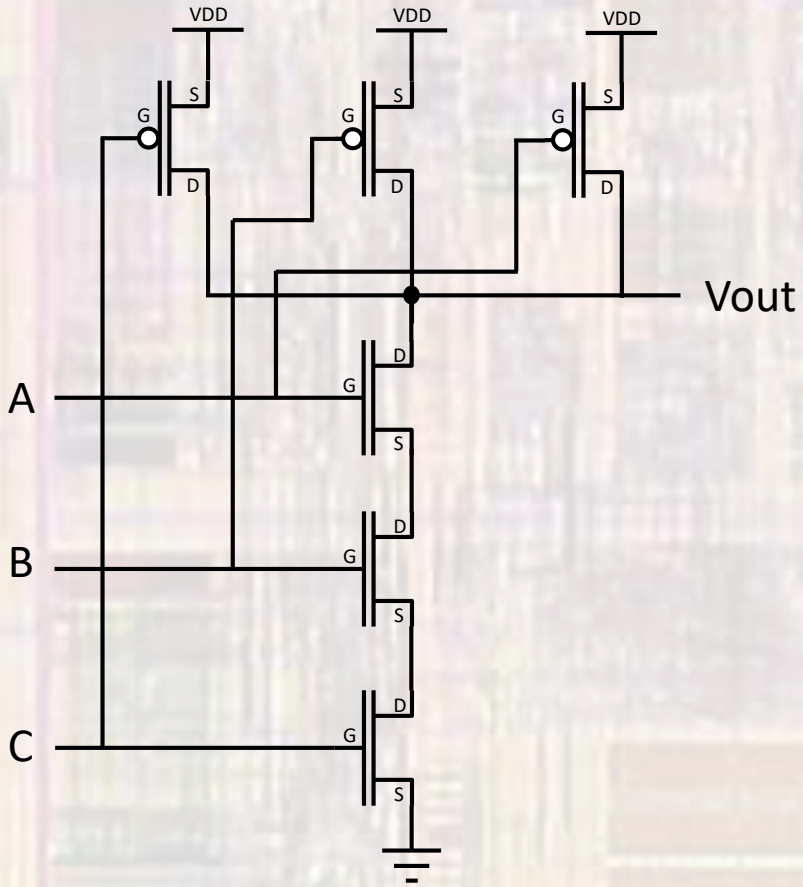




Logic Gates

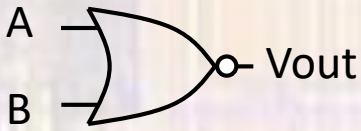
- Nand Gate

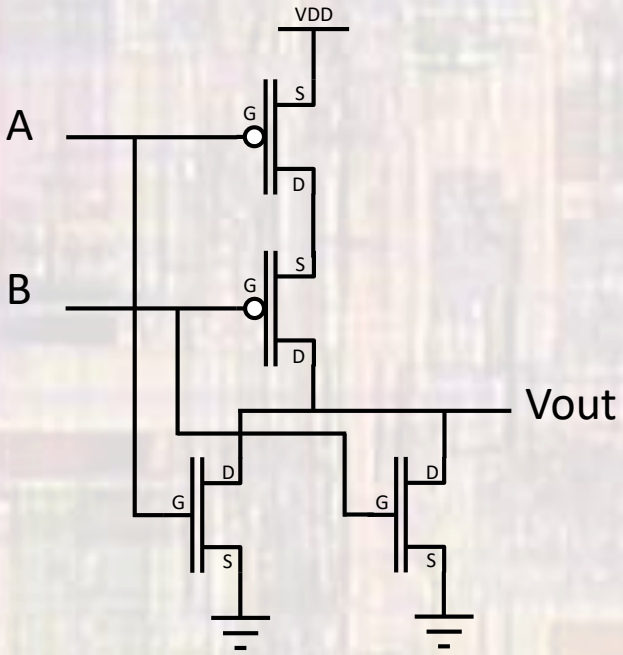




Logic Gates

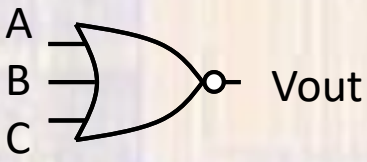
- Nor Gate

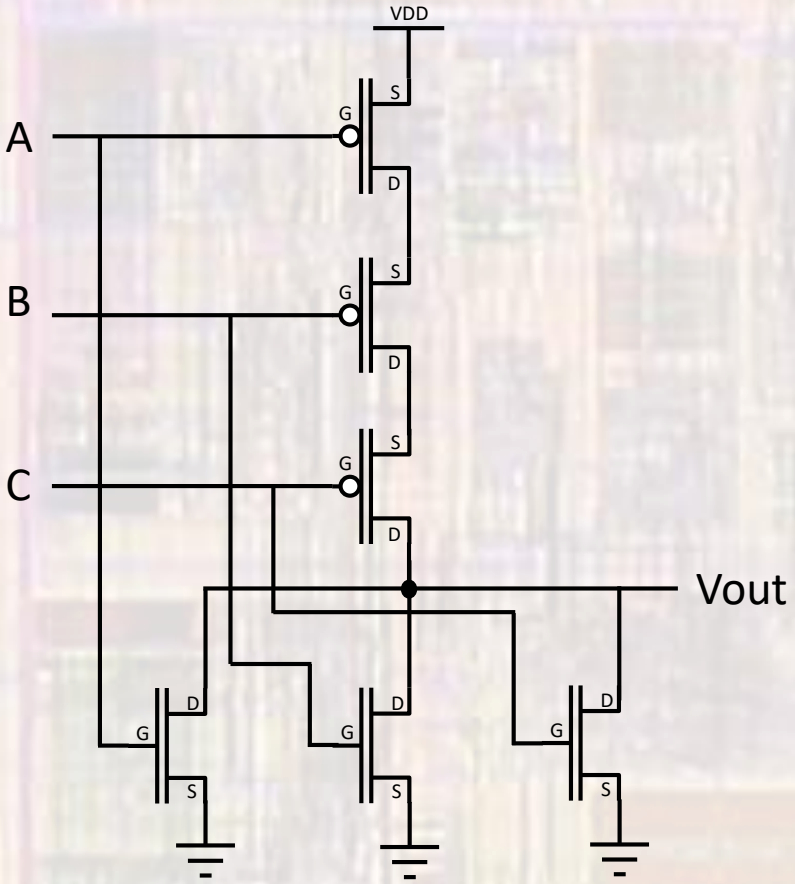




Logic Gates

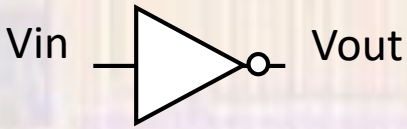
- Nor Gate

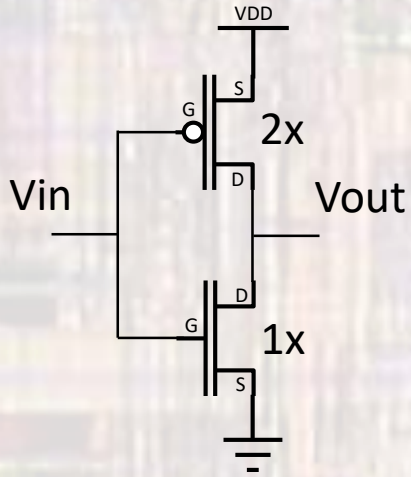




Logic Gates

- Inverter Circuit

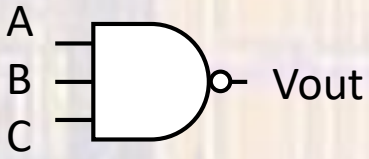


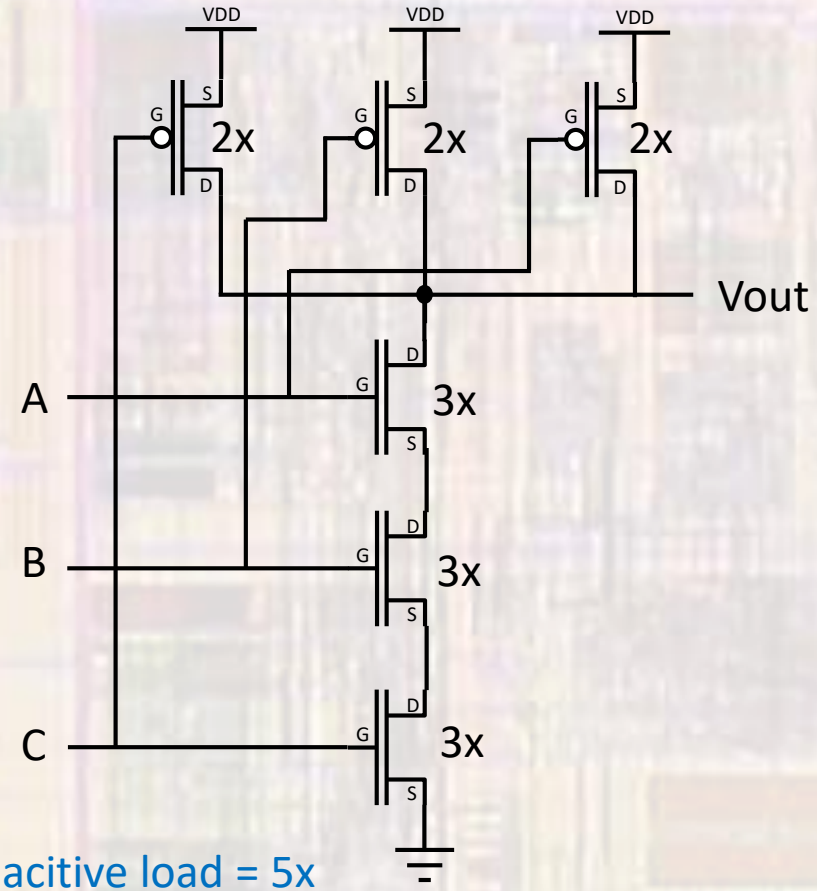


Input capacitive load = 3x

Logic Gates

- Nand Gate

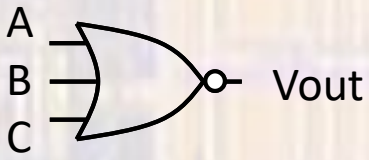


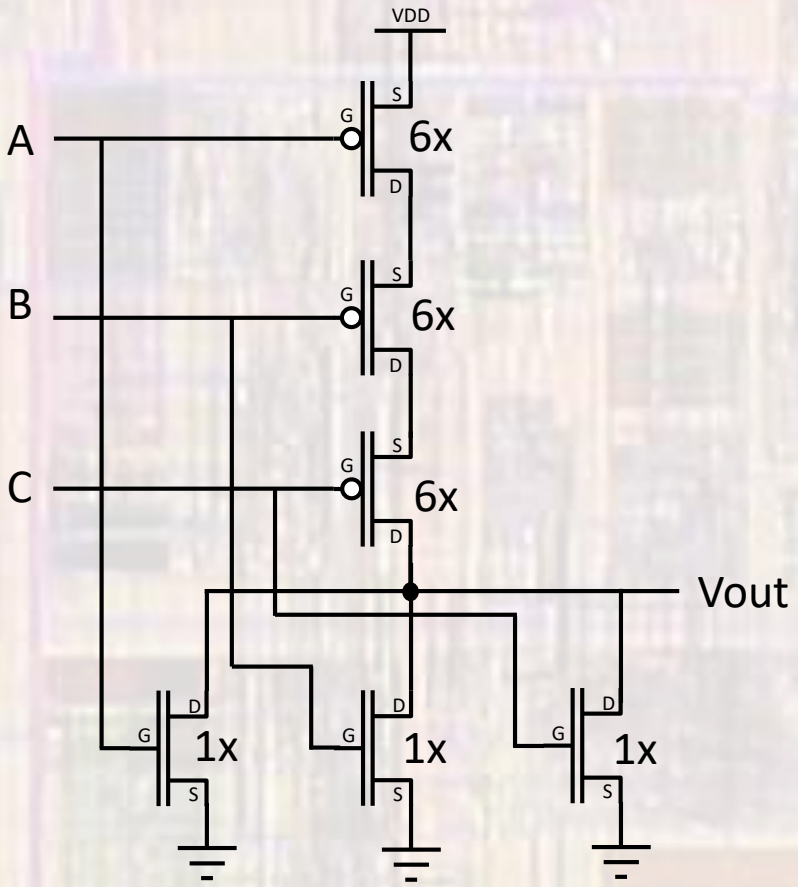


Input capacitive load = 5x

Logic Gates

- Nor Gate





Input capacitive load = 7x

Logic Gates

- Input loading

Effective input Load

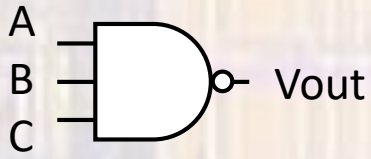
Gate Type	1 input	2 input	3 input	4 input
Inv	3x			
Nand		4x	5x	6x
Nor		5x	7x	9x

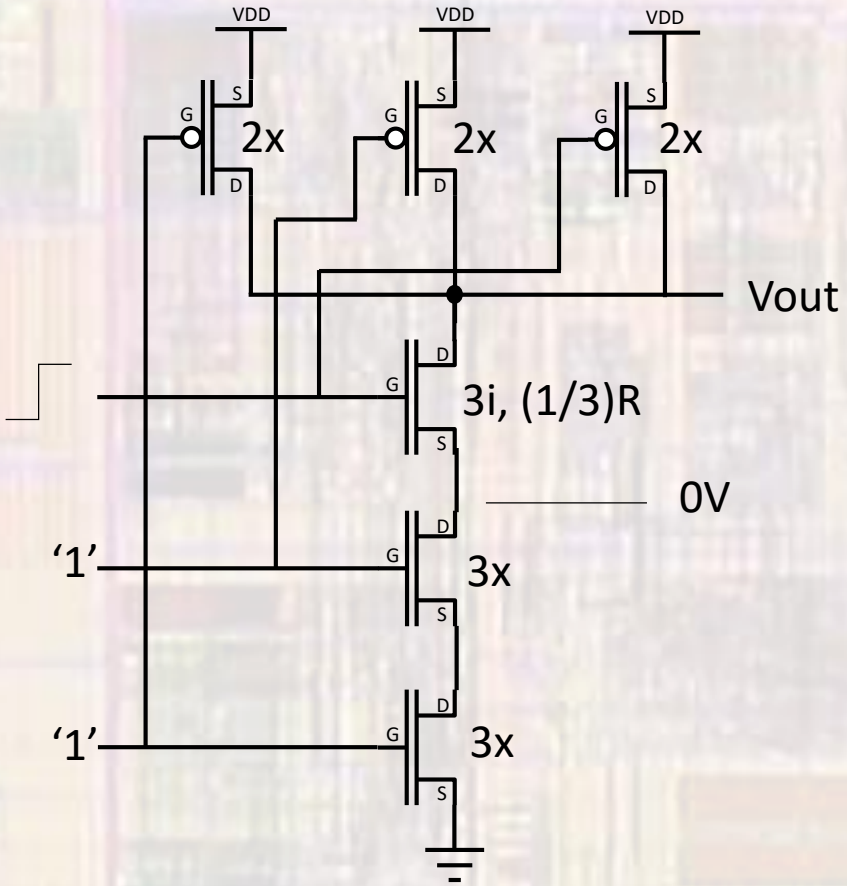
Normalized Effective input Load

Gate Type	1 input	2 input	3 input	4 input
Inv	0.75x			
Nand		1x	1.25x	1.5x
Nor		1.25x	1.75x	2.25x

Logic Gates

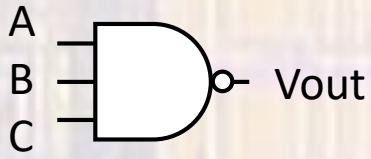
- Nand Gate Transient

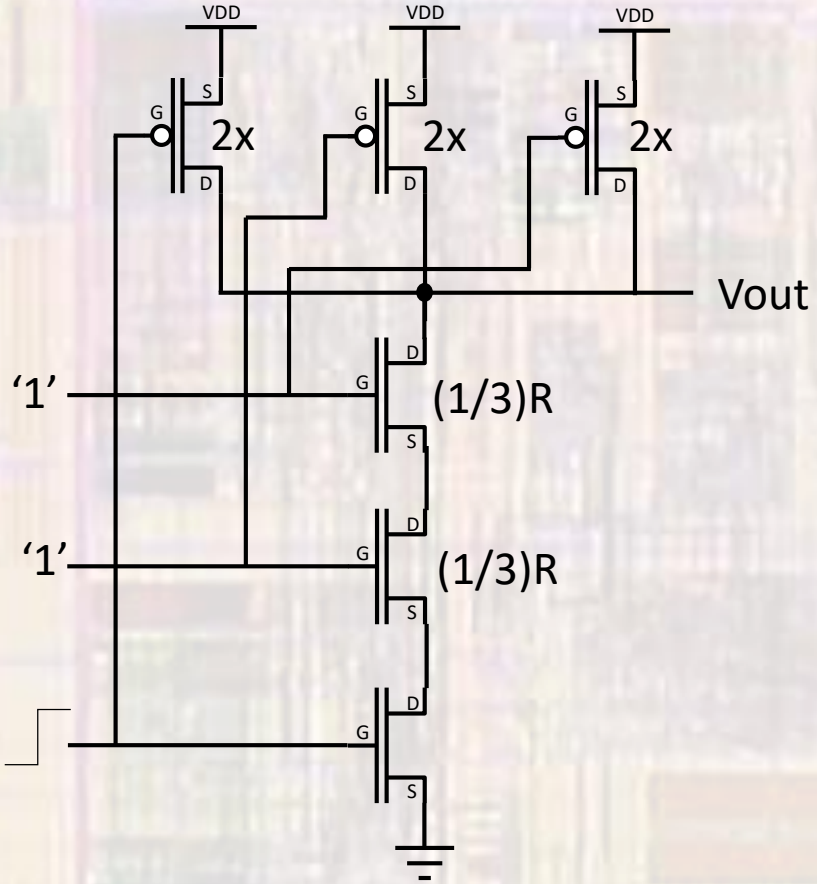




Logic Gates

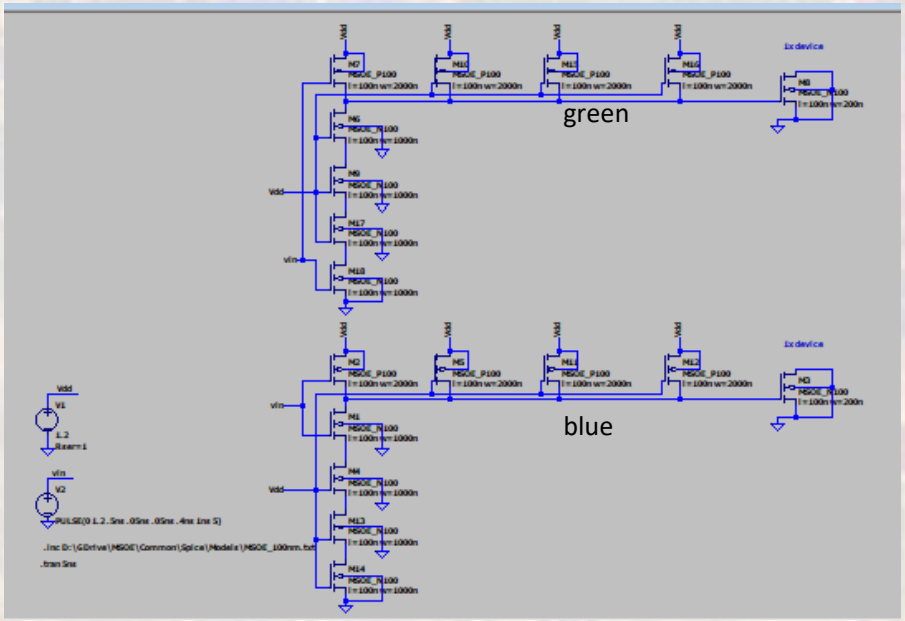
- Nand Gate Transient

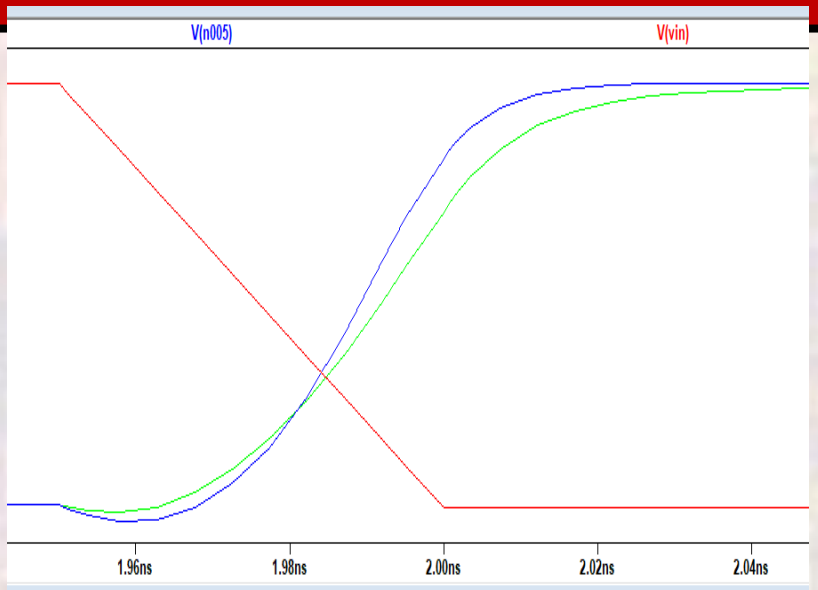


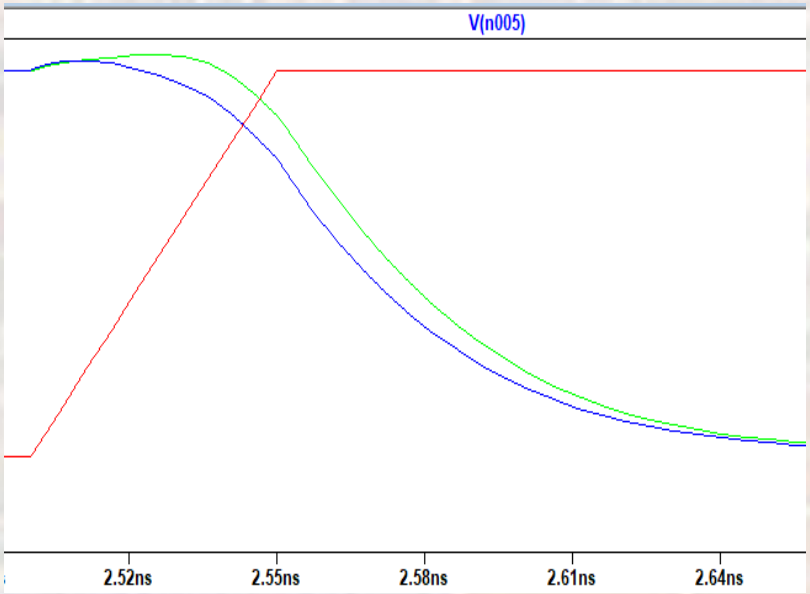


Logic Gates

- Nand Gate Transient

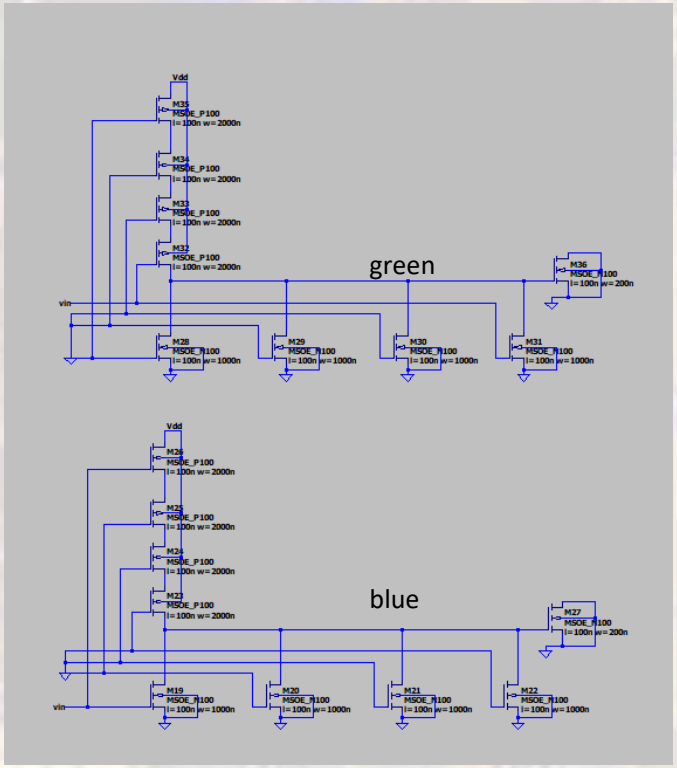


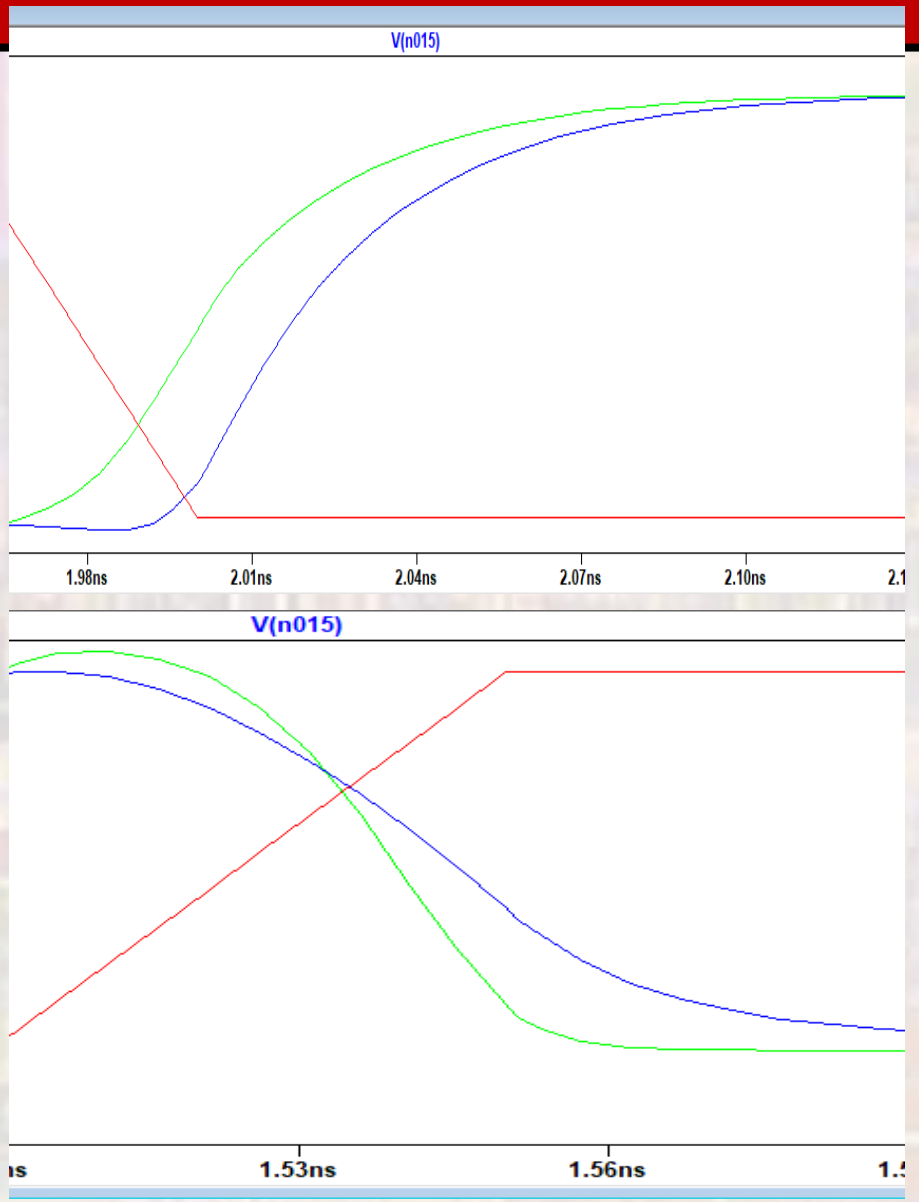




Logic Gates

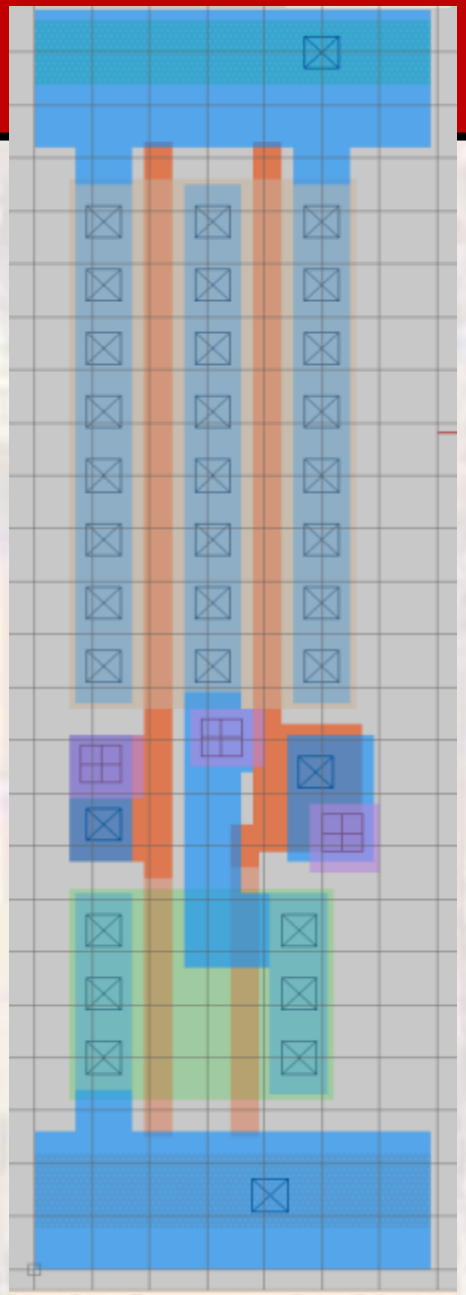
- Nor Gate Transient





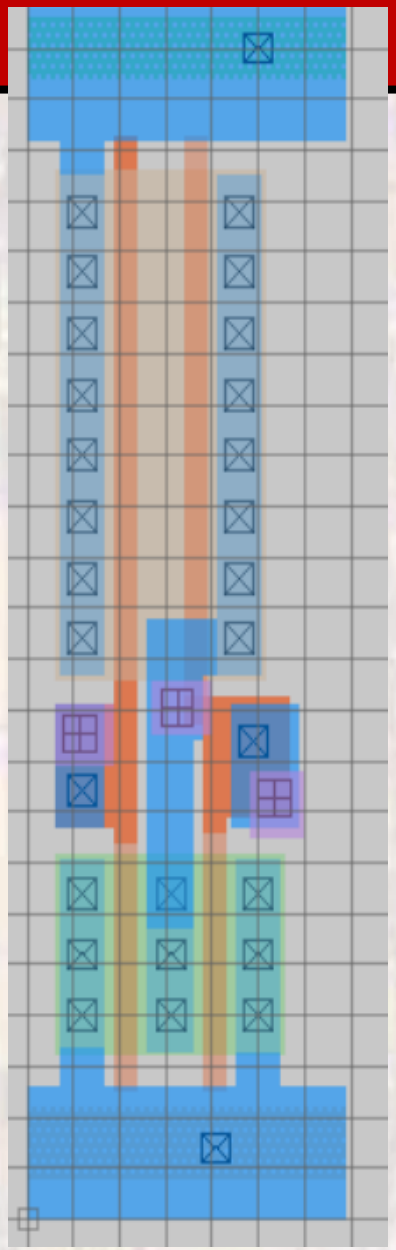
Logic Gates

- Nand 2 Layout



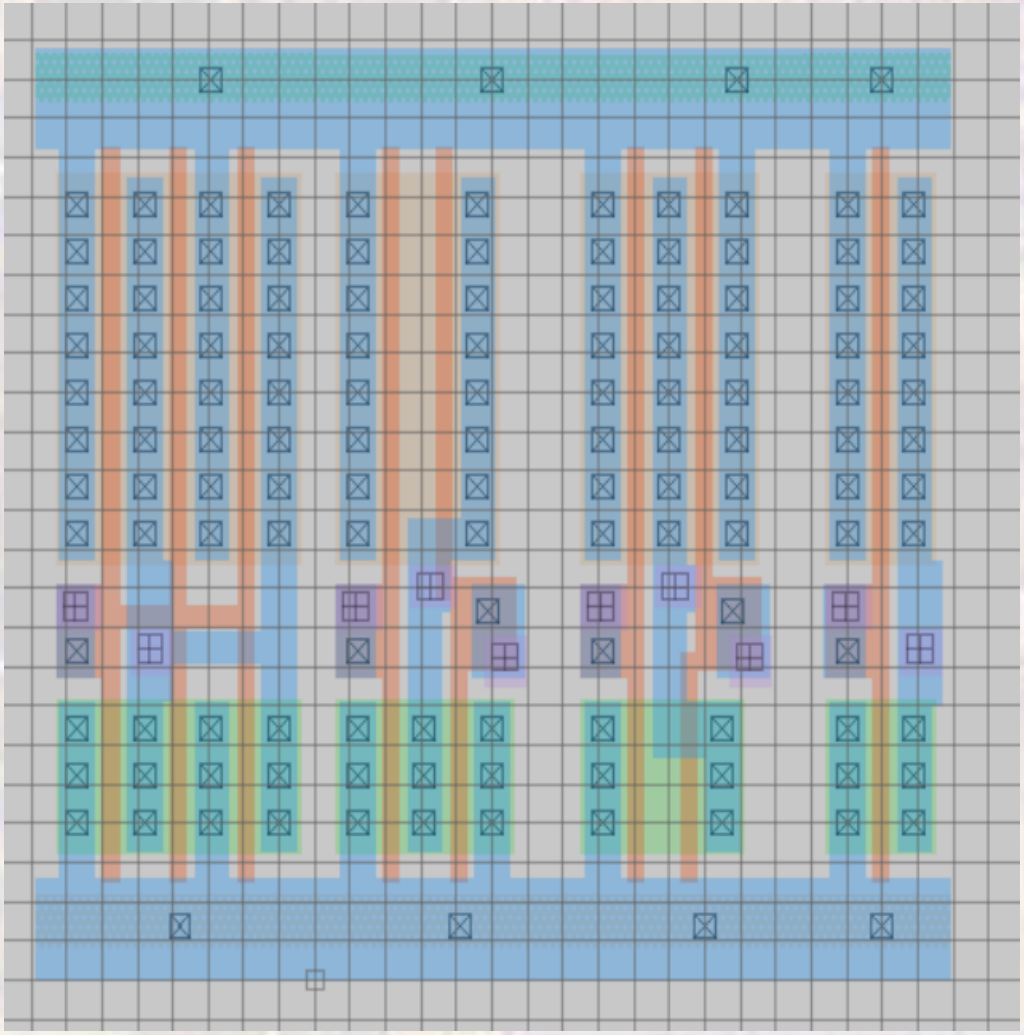
Logic Gates

- Nor 2 Layout



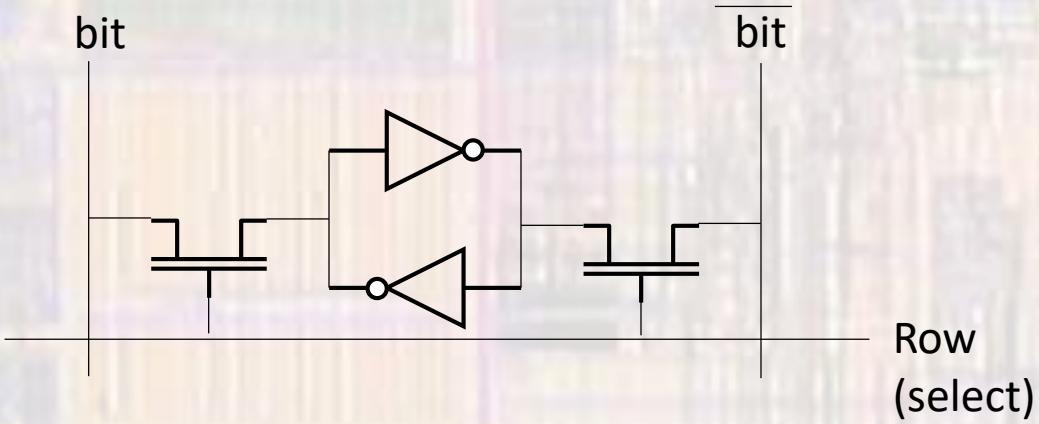
Logic Gates

- Logic Row Layout



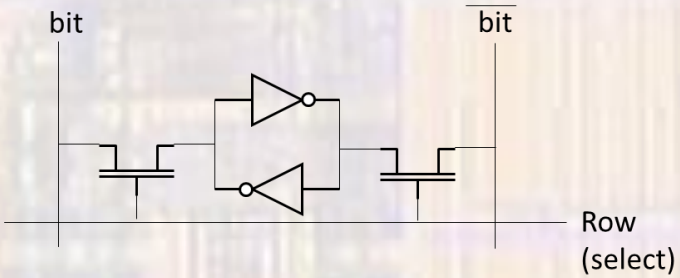
Logic Gates

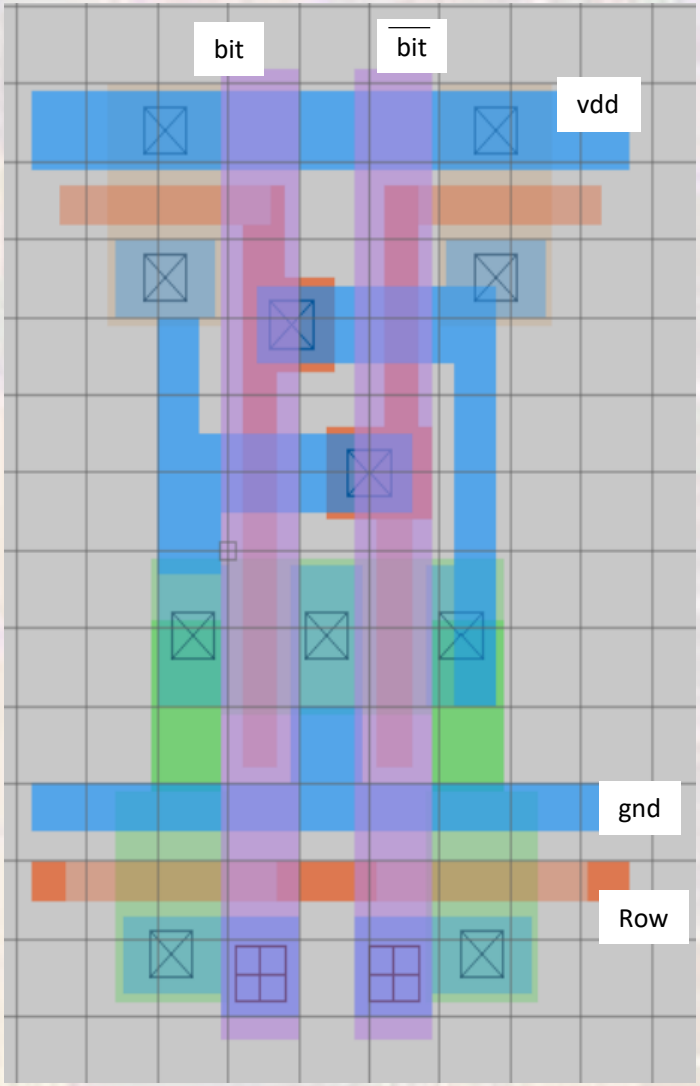
- SRAM bit



Logic Gates

- SRAM bit





Logic Gates

- SRAM bit