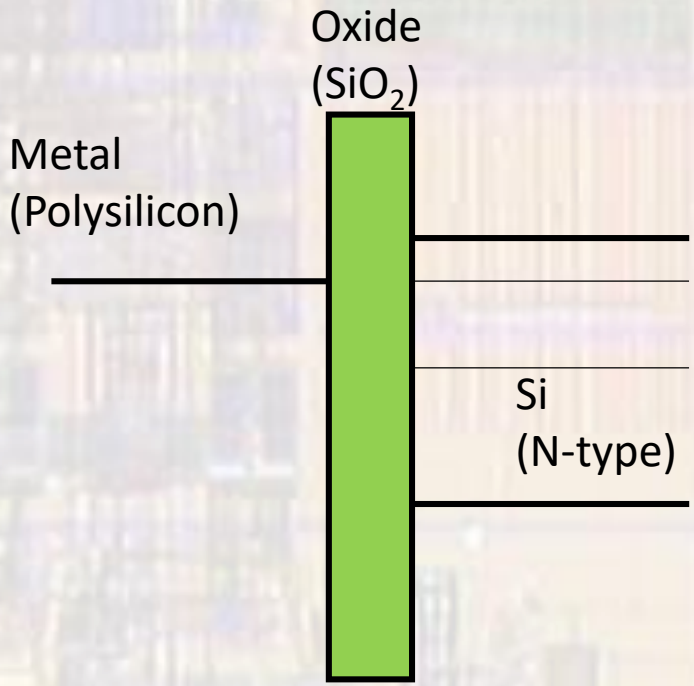
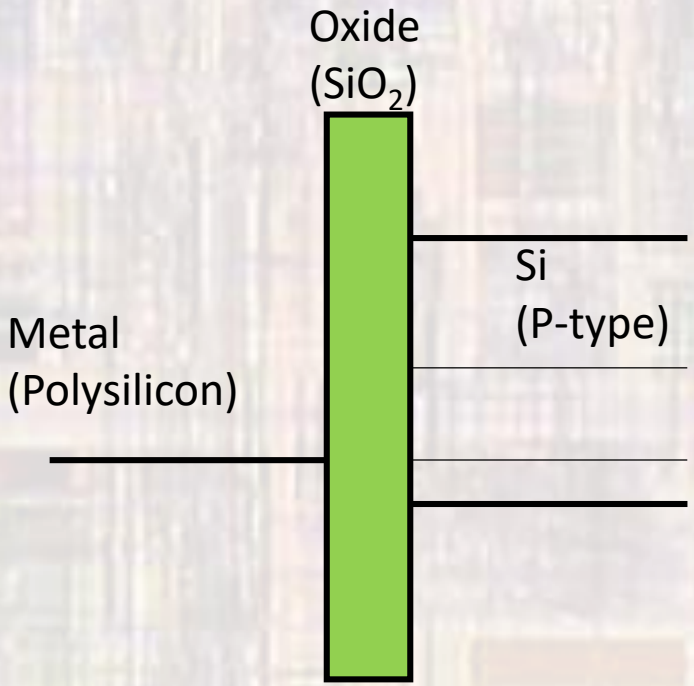
MOSFET

Last updated 3/17/19

MOSFET

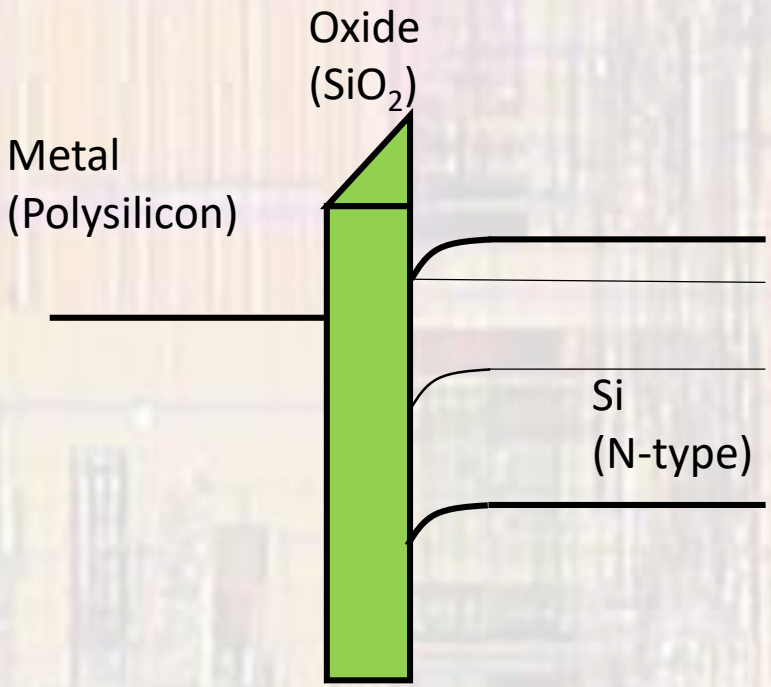
- MOS Capacitor
  - No bias





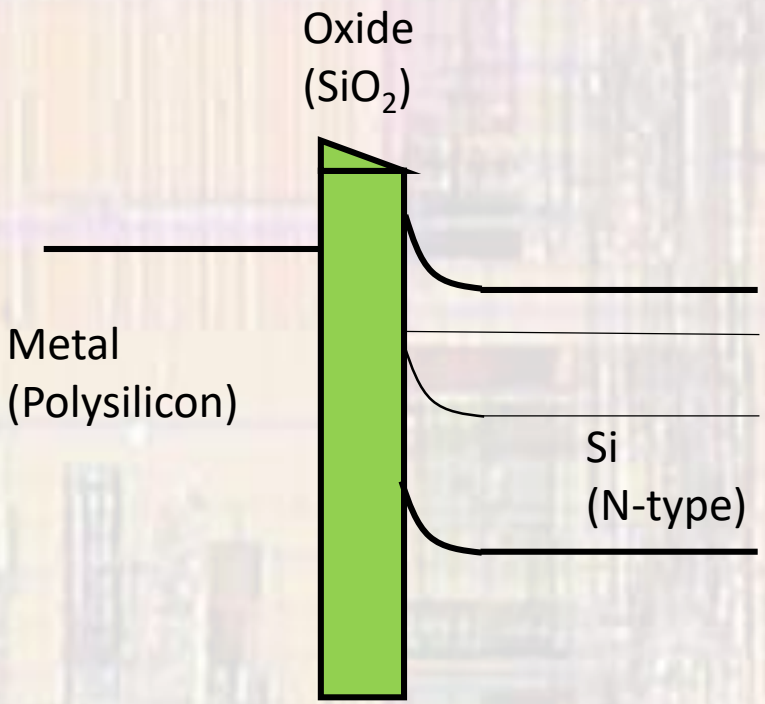
MOSFET

- MOS Capacitor: N-Type
  - Accumulation
  - $V_G > 0$
  - Excess e^- at the Si interface



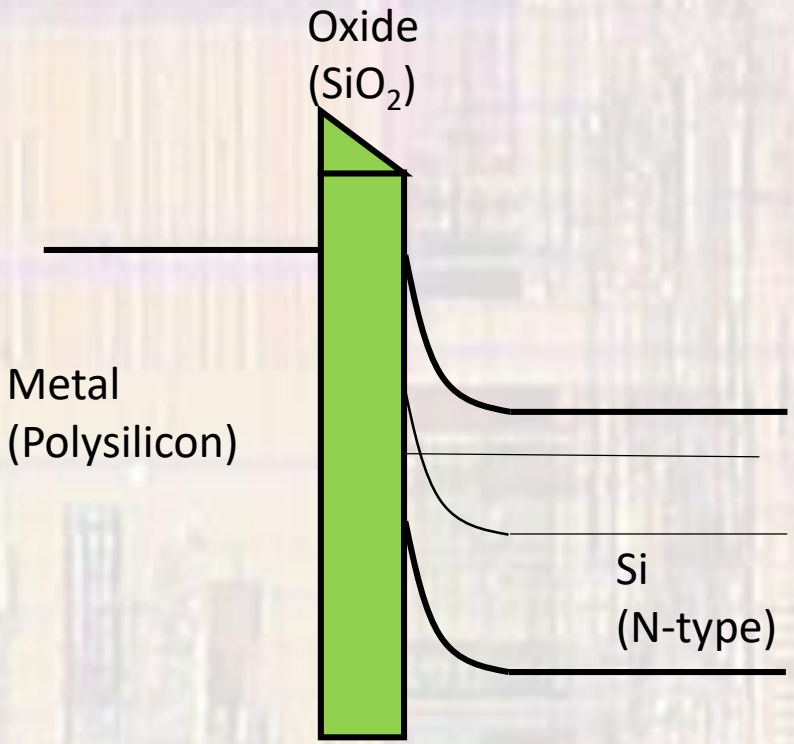
MOSFET

- MOS Capacitor: N-Type
  - Depletion
  - $V_G < 0$ (small)
  - No carriers at the Si interface



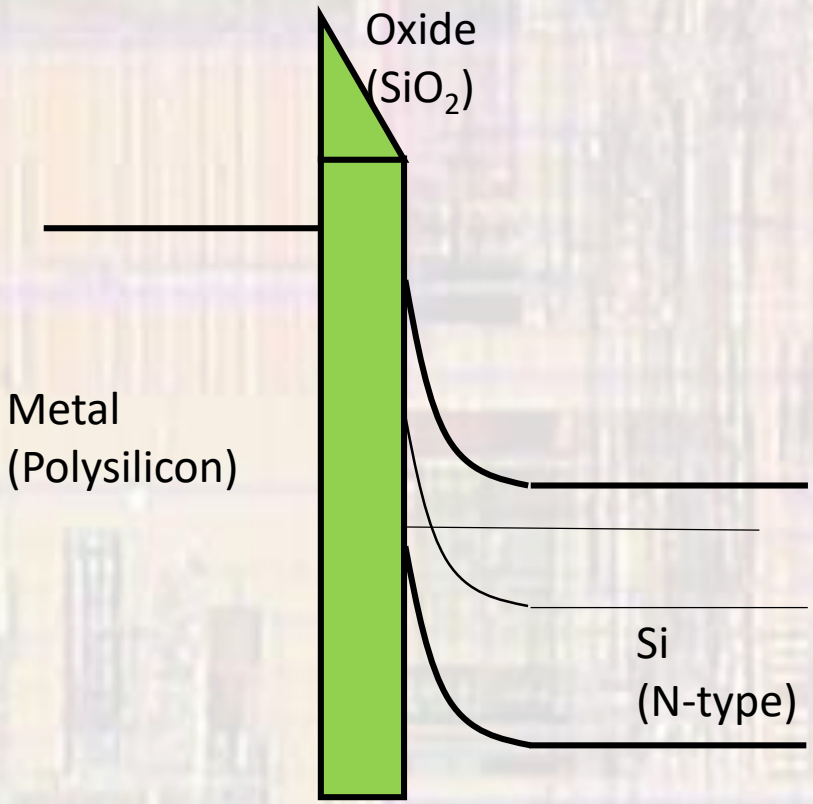
MOSFET

- MOS Capacitor: N-Type
  - Onset of Inversion
  - $V_G = V_T$
  - Some excess holes at the Si interface



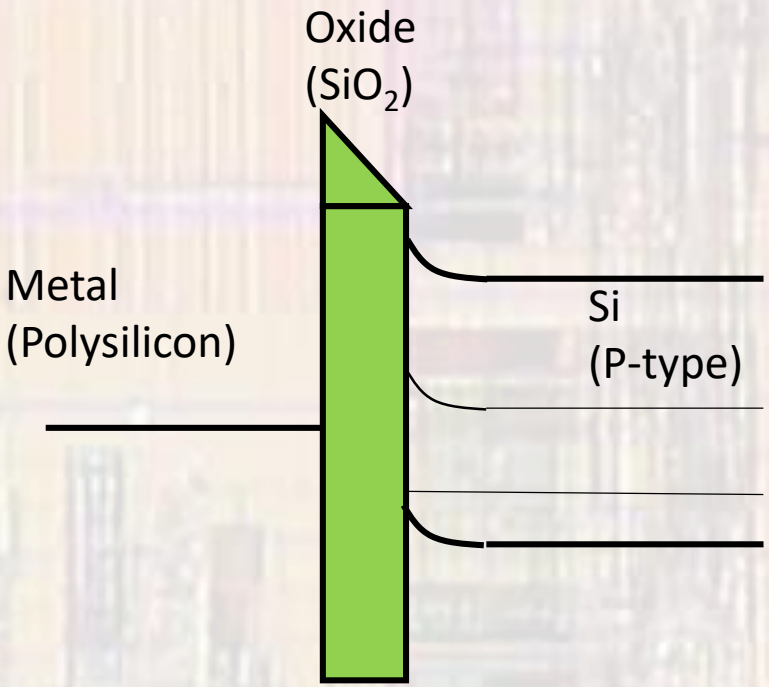
MOSFET

- MOS Capacitor: N-Type
  - Inversion
  - $V_G < V_T$
  - Excess holes at the Si interface



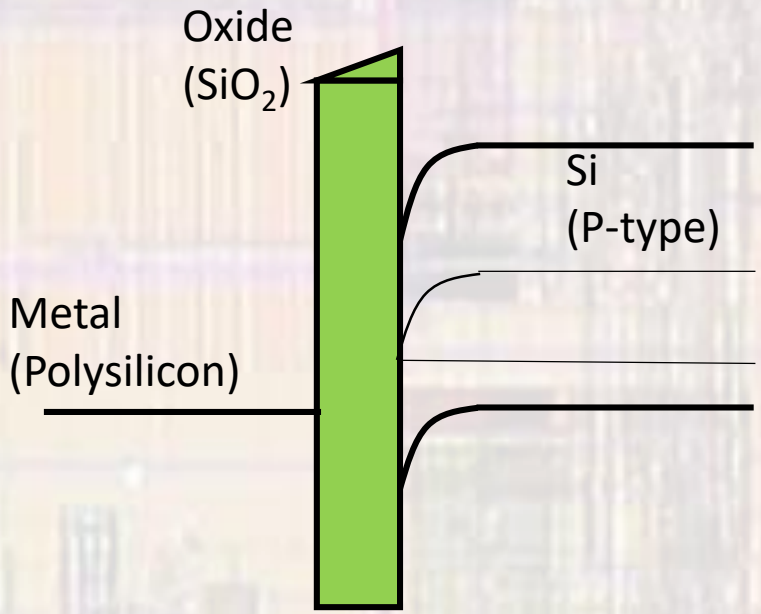
MOSFET

- MOS Capacitor: P-Type
  - Accumulation
  - $V_G < 0$
  - Excess holes at the Si interface



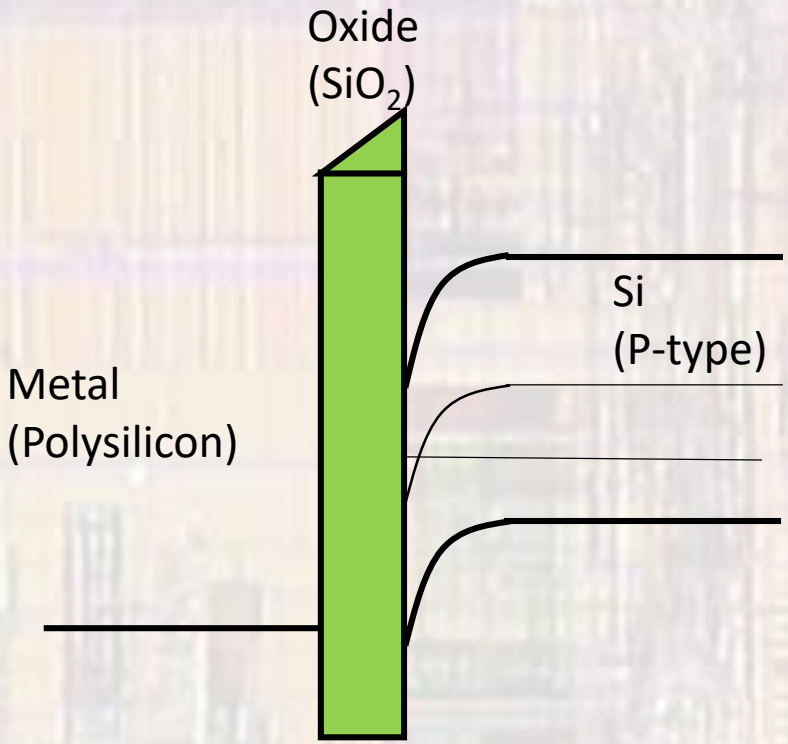
MOSFET

- MOS Capacitor: P-Type
  - Depletion
  - $V_G > 0$ (small)
  - No carriers at the Si interface



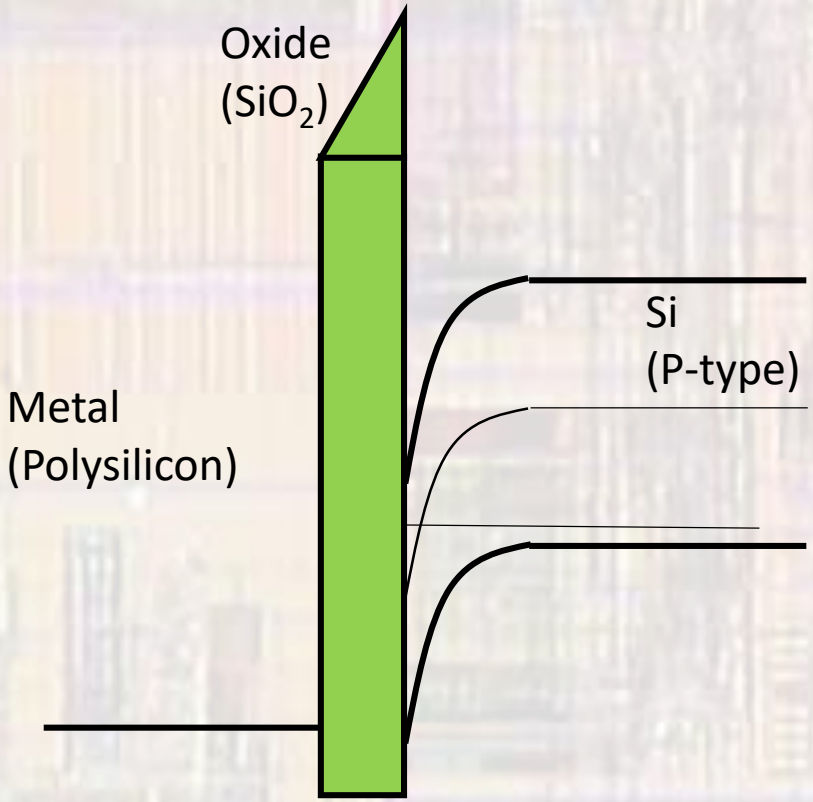
MOSFET

- MOS Capacitor: P-Type
  - Onset of Inversion
  - $V_G = V_T$
  - Some excess electrons at the Si interface



MOSFET

- MOS Capacitor: P-Type
  - Inversion
  - $V_G > V_T$
  - Excess electrons at the Si interface



MOSFET

- N-Channel
  - V_{GS} = 0V

MOSFET

- N-Channel
  - $V_{GS} = V_T$

MOSFET

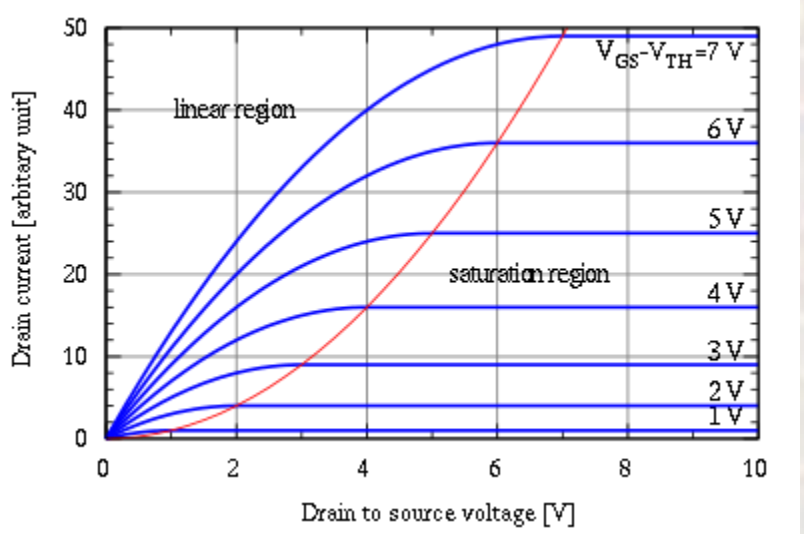
- N-Channel
  - $V_{GS} > V_T$

MOSFET

- N-Channel
  - $V_D > V_{Dsat}$

MOSFET

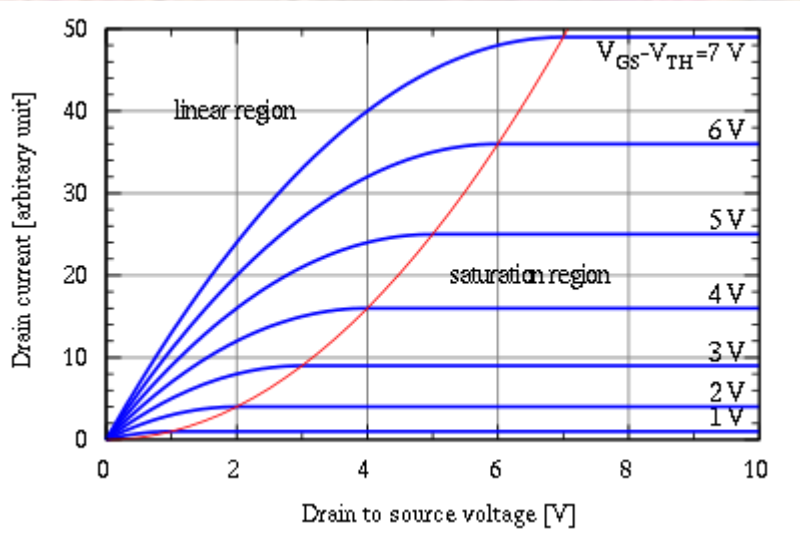
- N-Channel
  - $V_G > V_T$
  - $0 < V_D < V_{Dsat}$
  - Linear Region



$$I_D = \frac{Z\mu_0 C_0}{L}\left[(V_G - V_T)V_D - {V_D}^2/2\right]$$

MOSFET

- N-Channel
  - $V_G - V_T = V_{Dsat}$
  - Saturation



$$I_{Dsat} = \frac{Z\mu_0 C_0}{2L}\left(V_G - V_T\right)^2$$

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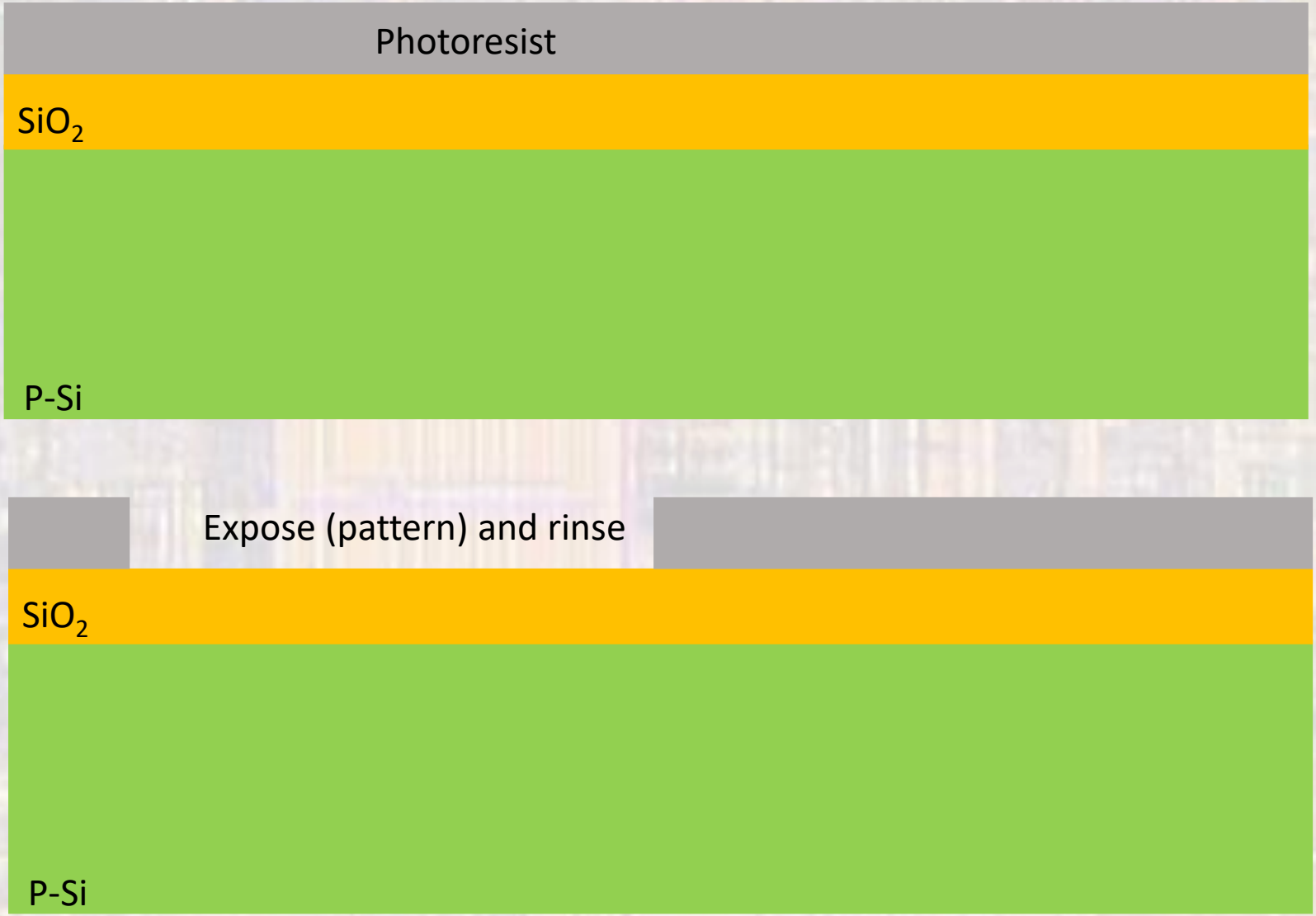


MOSFET

N type implant/diffusion and drive

Pattern – Etch – Grow thin oxide

MOSFET

Deposit Poly and Pattern

Implant P+ : self aligned gate

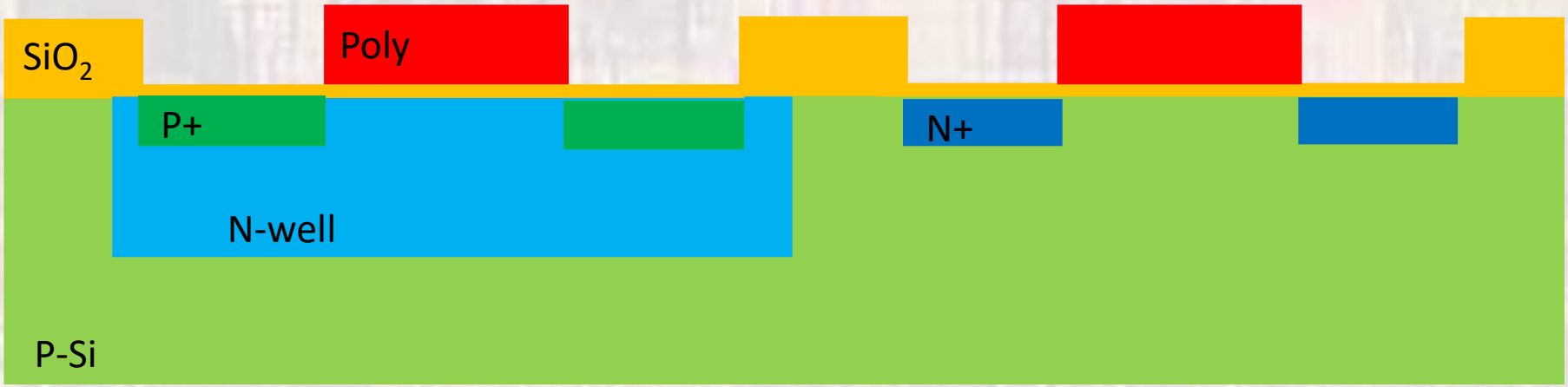
MOSFET

Pattern – Etch – Grow thin oxide

Deposit Poly - Pattern

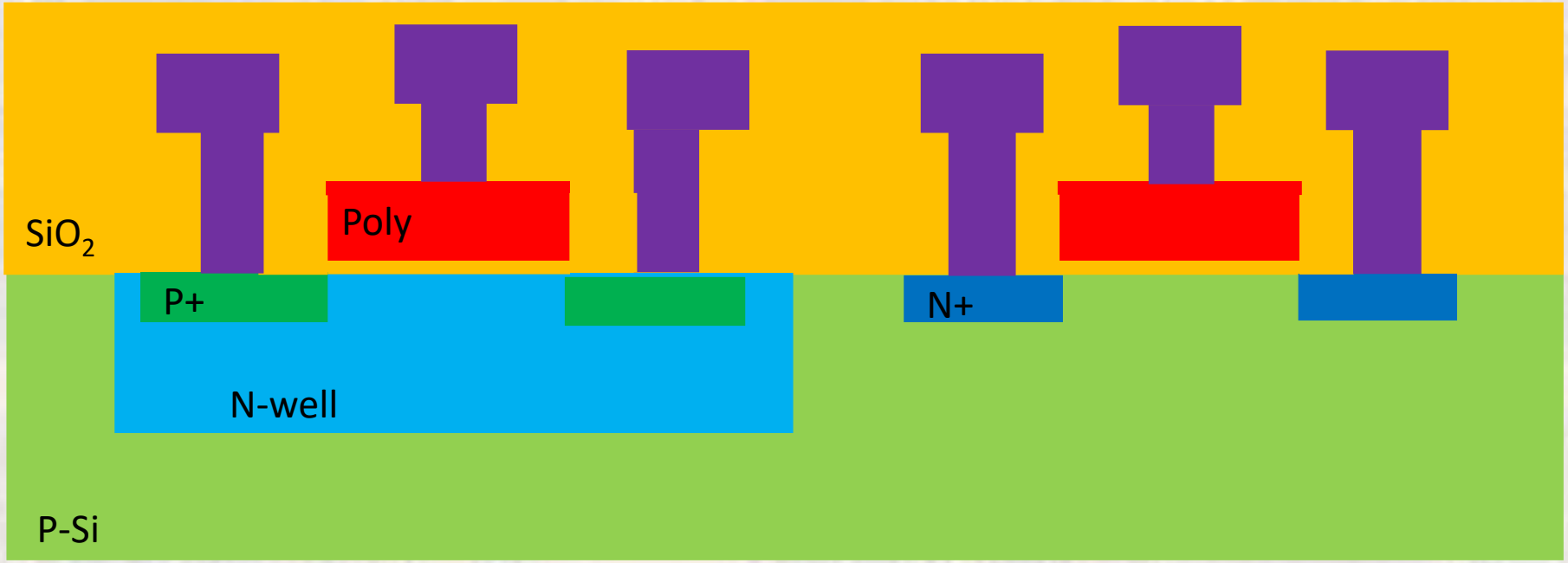
MOSFET

Ion Implant N+ : self aligned gate



MOSFET

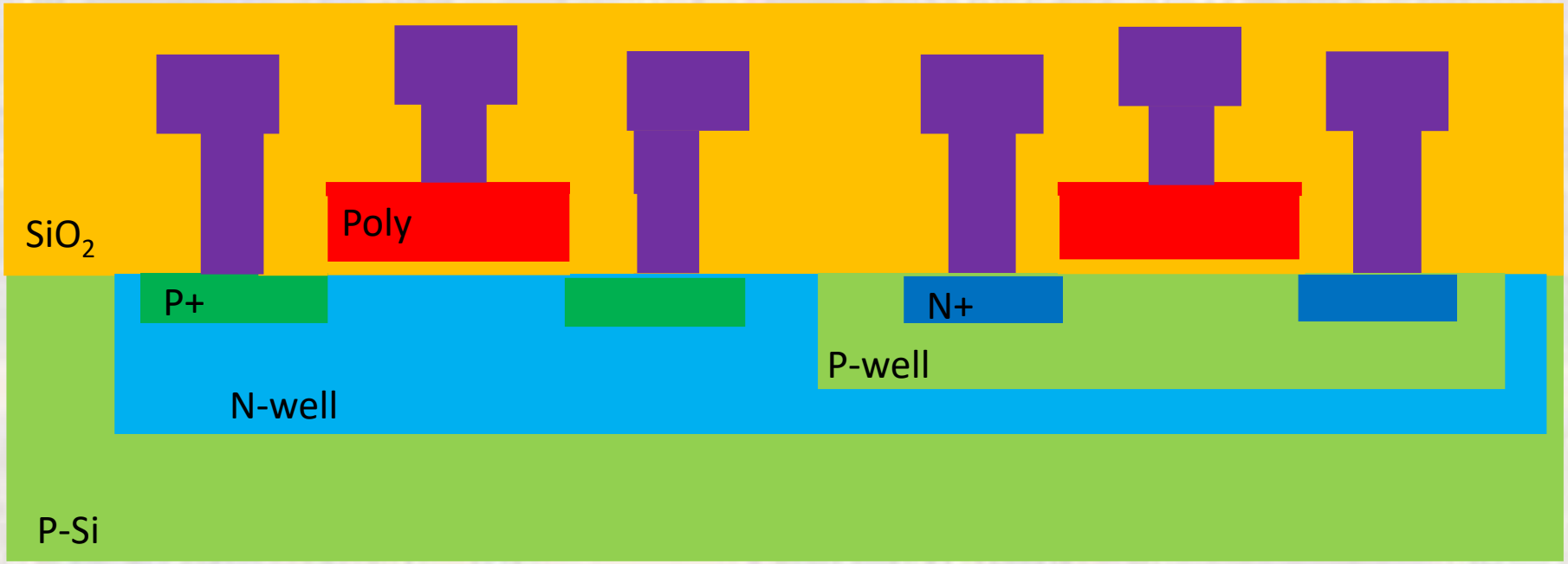
Contacts and metallization



Note: N-channel body (P-Si) must be tied to V-

MOSFET

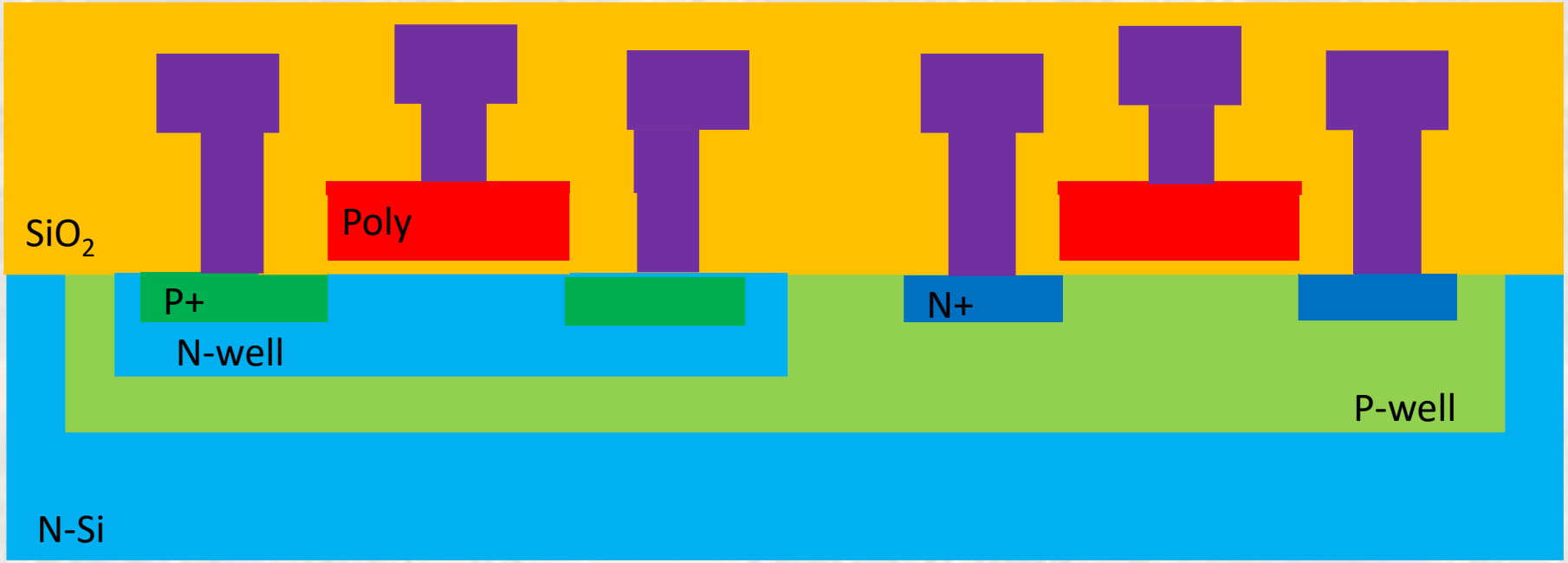
Dual Well Process



Note: P-Si must be tied to V-

MOSFET

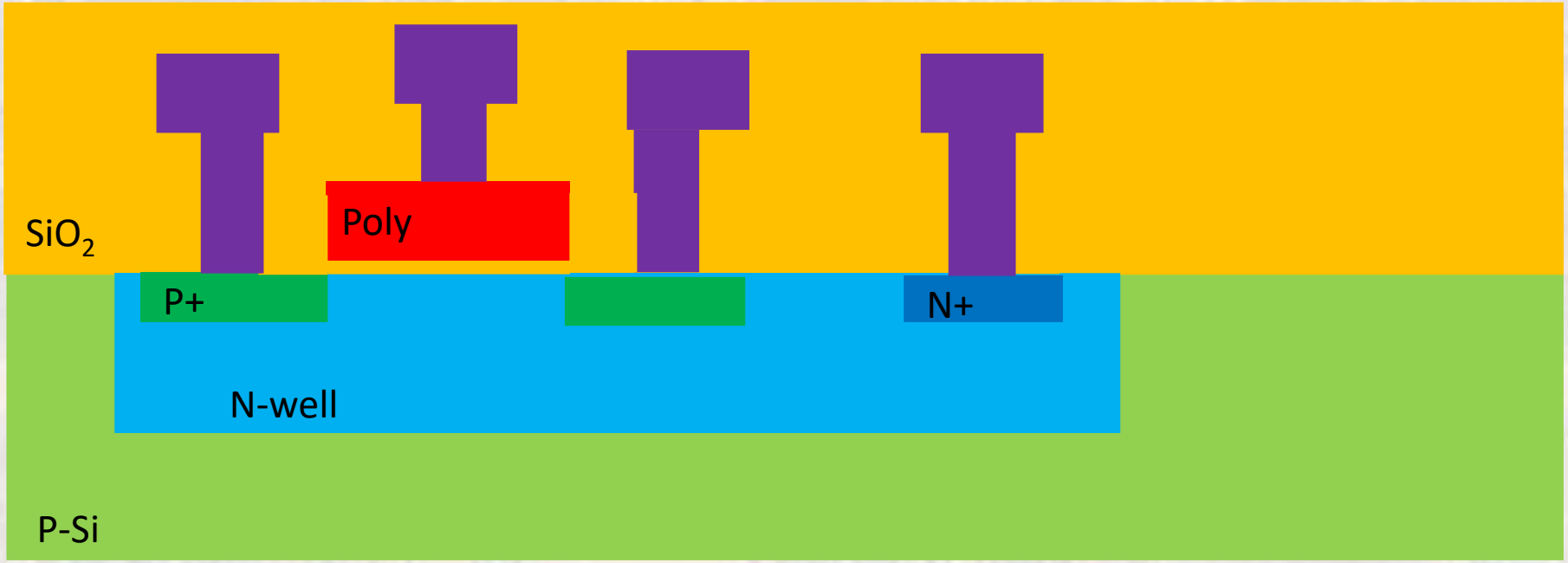
Dual Well Process



Note: N-Si must be tied to V+

MOSFET

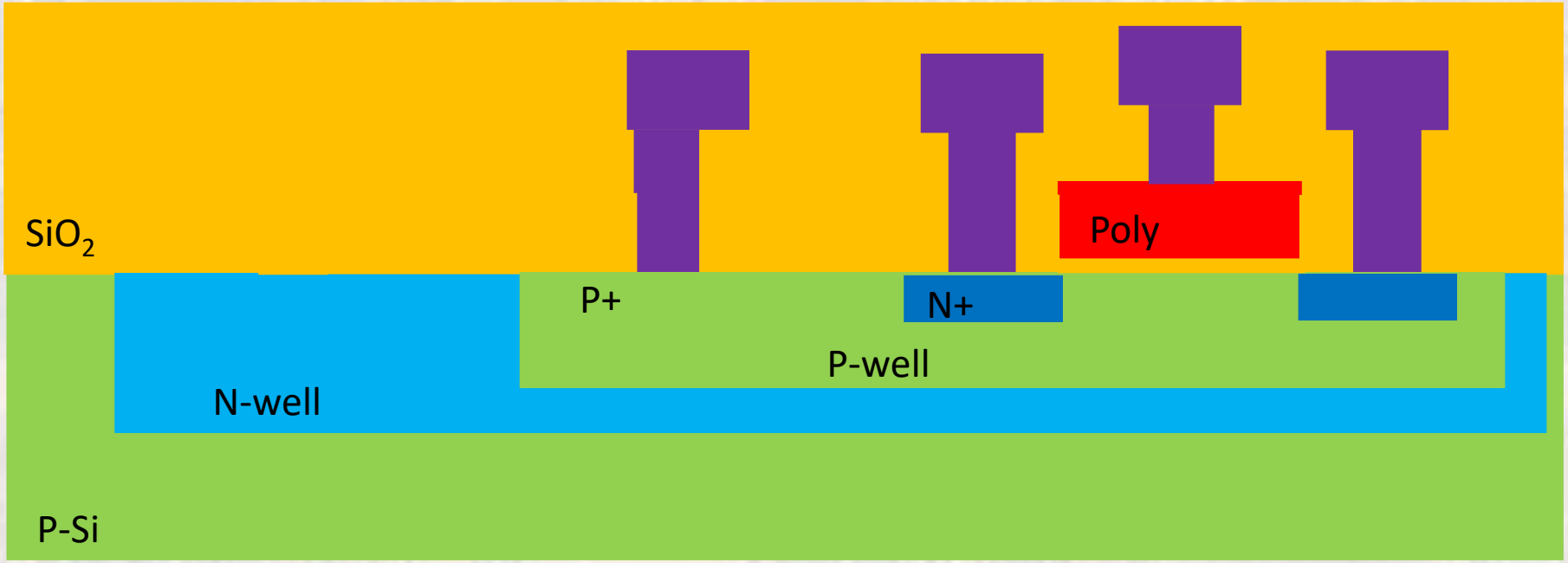
Dual Well Process



N-Well body contact

MOSFET

Dual Well Process



P-Well body contact

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