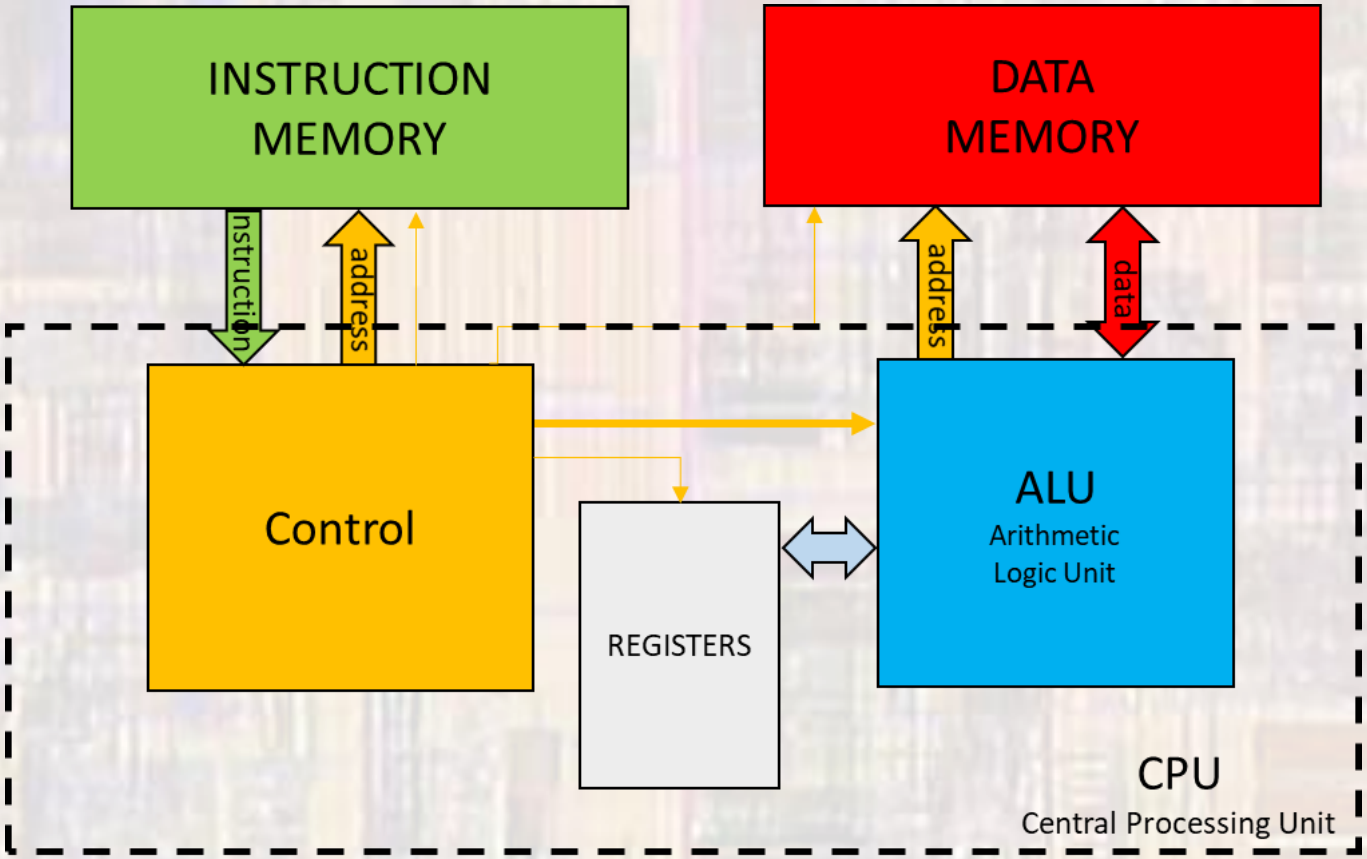
Embedded Systems Architecture

Last updated 7/25/24

These slides introduce the architecture of embedded computer systems

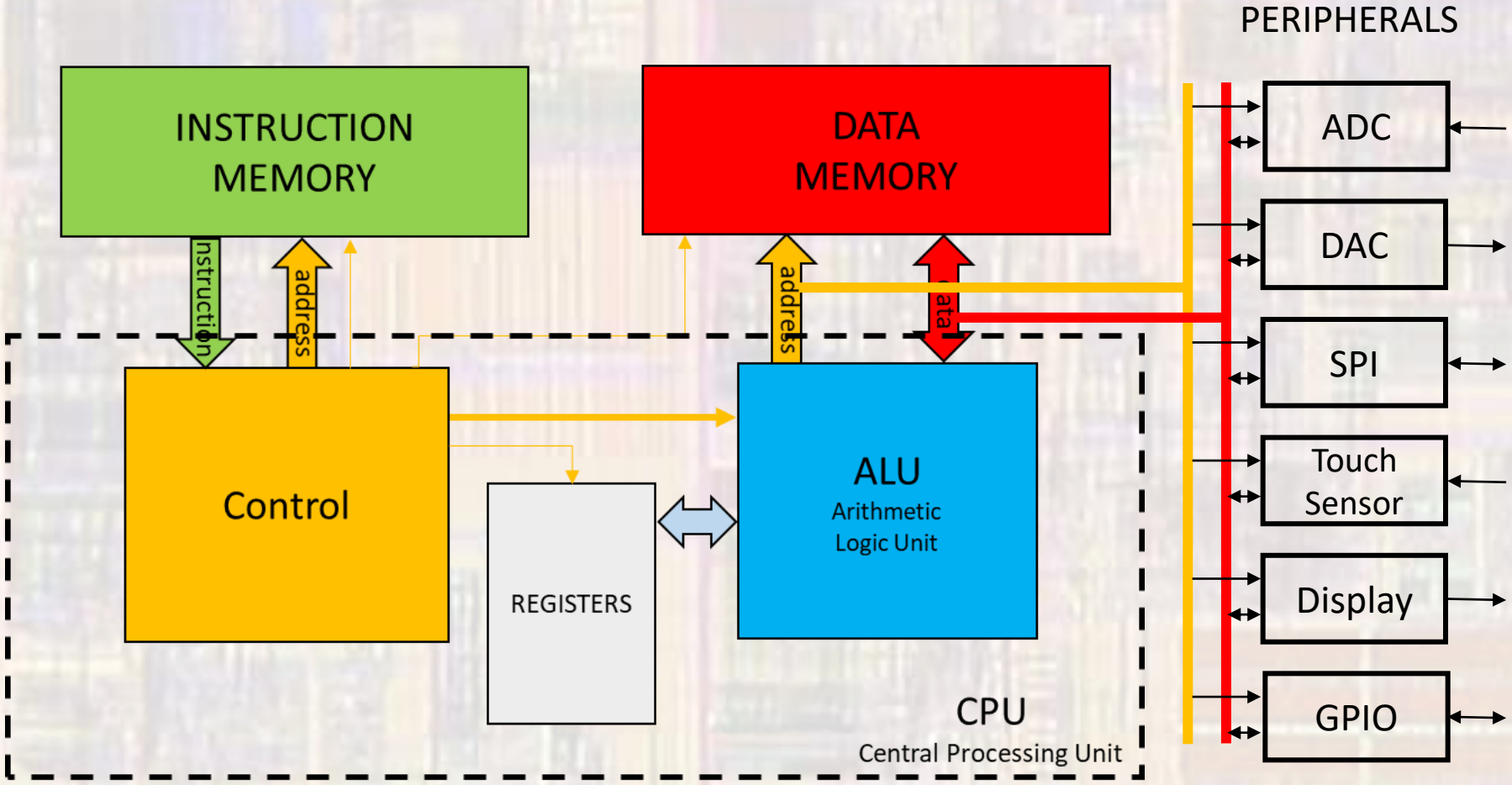
Embedded Systems Architecture

- Components (Harvard Architecture)



Embedded Systems Architecture

- Embedded System Components
  - Peripherals are system dependent

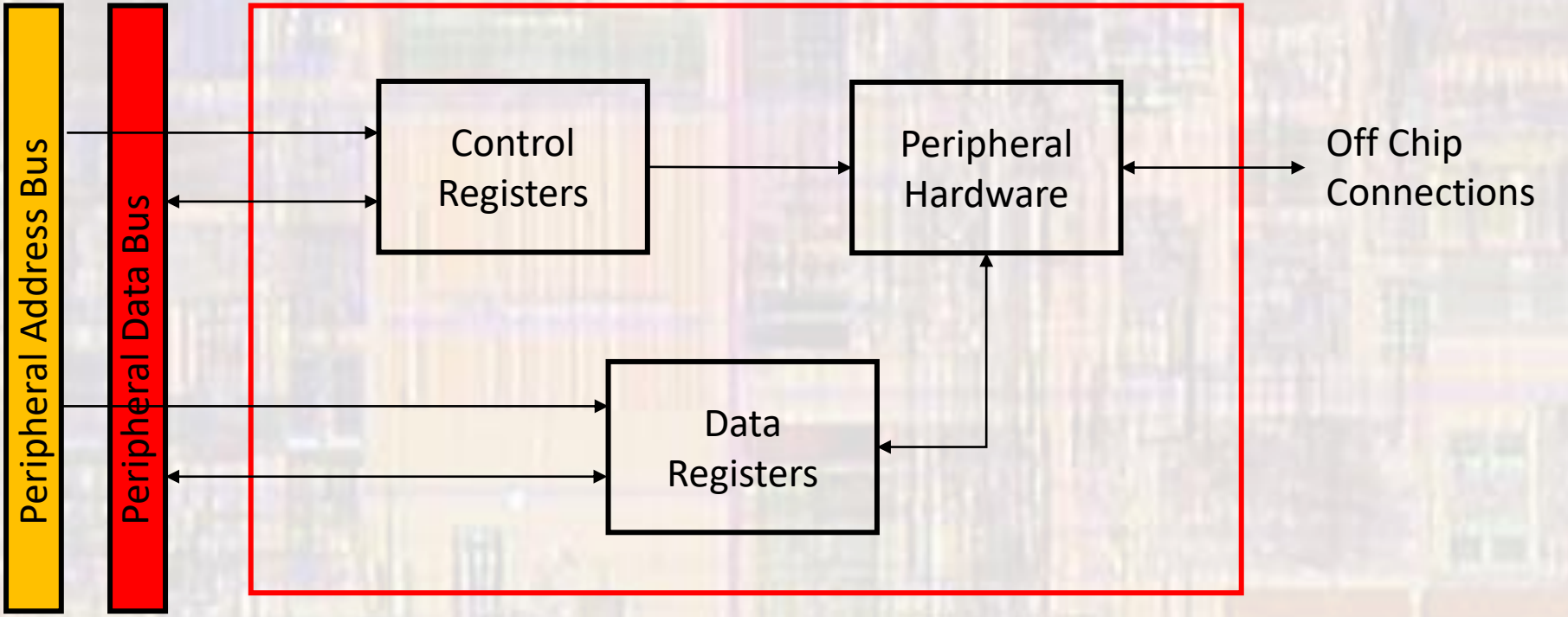


Embedded Systems Architecture

- Peripherals
  - Dedicated blocks used to perform specific functions
    - ADC – convert analog signals to digital signals
    - SPI – communicate to other processor systems or external components
    - GPIO – general purpose I/O
      - Used to read/write to individual wires
        - Turn on an LED
        - Read the value on a switch
    - Many variations

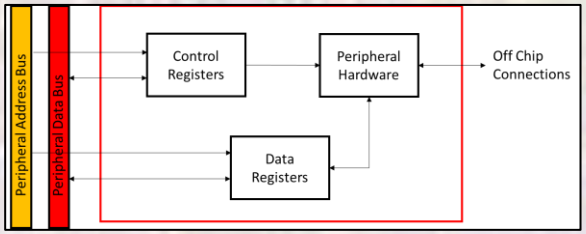
Embedded Systems Architecture

- Peripheral structure (typical)



Embedded Systems Architecture

- Control Registers
  - Collection of 1/2/4 byte words
  - Selected via the peripheral address bus
  - R/W via the peripheral data bus
  - Store control information
  - Can be written to select various modes of operation
  - Can be read to determine current mode
  - Can be read to find status



Each peripheral has a base address assigned during design (0x2f00)

The base address is outside the normal data memory range

Individual registers are accessed using the base address + offset

Mode = base + 0x0C

Status 2	0x2F14
Status 1	0x2F10
Mode	0x2F0C
Control 3	0x2F08
Control 2	0x2F04
Control 1	0x2F00

Embedded Systems Architecture

- Control Registers – cont'd
  - Collection of 1/2/4 byte words
  - Each word may be made up of a collection of independent bits or groups of bits

Table 318. ADC register map and reset values for each ADC (offset = 0x00 for master ADC, 0x100 for slave ADC)

Offset	Register name reset value	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ADC_ISR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LDORDY	Res.	Res.	AWD3	AWD2	AWD1	JEOS	JEOC	OVR	EOS	EOC	EOSMP	ADRDY
	Reset value																																
0x04	ADC_IER	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	Reset value																																
0x08	ADC_CR	ADCAL	Res.	DEEPPWD	ADVREGEN	CALINDEX[3:0]				Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADCALIN	Res.	Res.														
	Reset value	0		0	0	0	0	0	0								0																
0xDC	ADC_CFGR1	Res.	AWD1CH[4:0]					JAUTO	JAWD1EN	AWD1EN	AWD1SGL	Res.	JDISCEN	DISCNUM [2:0]			DISCEN	Res.	AUTDLY															
	Reset value		0	0	0	0	0	0	0	0	0		0	0	0	0	0		0														
0x10	ADC_CFGR2	LSHIFT[3:0]				LSTRG	Res.	OSR[9:0]										SMPTRG	SWTRIG	BU			RO	TR	OVS						JO	RO	
	Reset value	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0				0	0
0x14	ADC_SMPR1	Res.	Res.	SMP9[2:0]			SMP8[2:0]			SMP7[2:0]			SMP6[2:0]			SMP5[2:0]			SMP4[2:0]			SMP3[2:0]			SMP2[2:0]			SMP1[2:0]			SMP0[2:0]		
	Reset value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	ADC_SMPR2	Res.	Res.	SMP19 [2:0]			SMP18 [2:0]			SMP17 [2:0]			SMP16 [2:0]			SMP15 [2:0]			SMP14 [2:0]			SMP13 [2:0]			SMP12 [2:0]			SMP11 [2:0]			SMP10 [2:0]		
	Reset value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

33.6.4 ADC configuration register (ADC_CFGR1)

Address offset: 0x0C

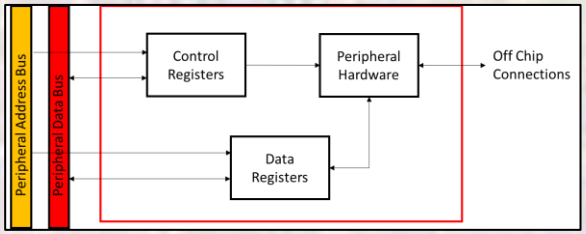
Reset value: 0x8000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	AWD1CH[4:0]					JAUTO	JAWD1EN	AWD1EN	AWD1SGL	Res.	JDISCEN	DISCNUM[2:0]			DISCEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	AUTDLY	CONT	OVRMOD	EXTEN[1:0]		EXTSEL[4:0]					Res.	RES[1:0]		DMNGT[1:0]	
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw

Embedded Systems Architecture

- Data Registers
  - Collection of 1/2/4 byte words
  - Selected via the peripheral address bus
  - R/W via the peripheral data bus
  - Store data to read/write from/to the peripheral hardware block
  - Data and Control registers are often combined



Each peripheral has a base address assigned during design (0x2f00)

The base address is outside the normal data memory range

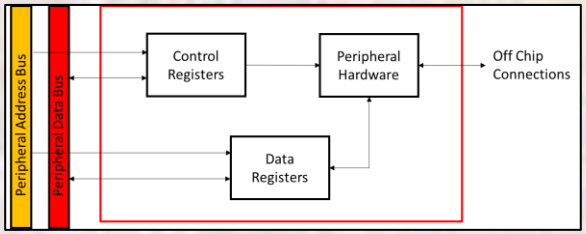
Individual registers are accessed using the base address + offset

Data In = base + 0x1C

Data In	0x2F1C
Data Out	0x2F18
Status 2	
Status 1	
Mode	

Embedded Systems Architecture

- Peripheral Hardware



  - Dedicated hardware to perform a specific task
  - Controlled via the control registers
  - Data read/written from/to the data registers
  - Has an interface to the external world

