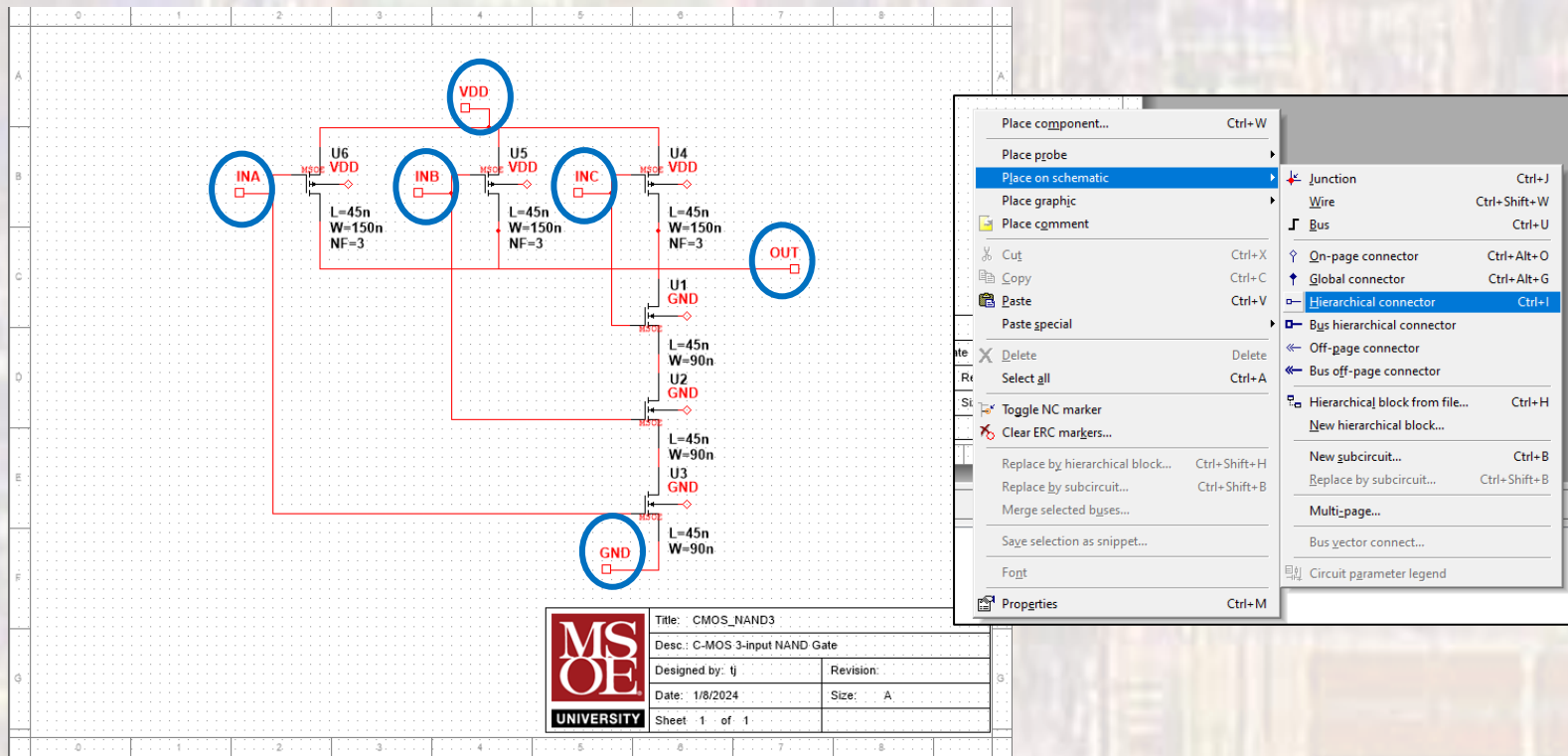


Hierarchical Design (MultiSim)

Last modified 1/8/24

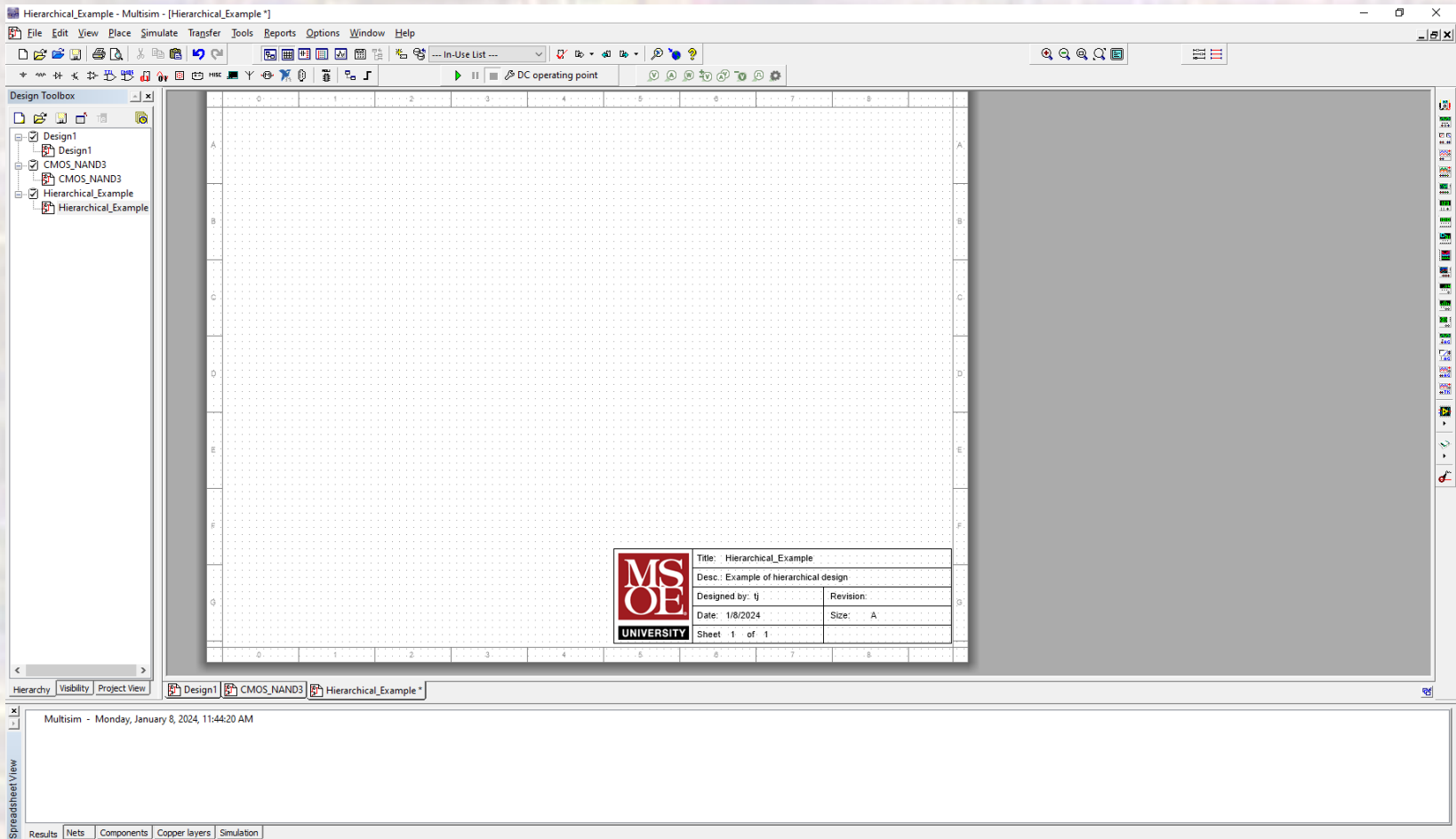
Hierarchical Design

- Create the design for the hierarchical block
 - Use hierarchical connectors for ALL pins
 - Place on schematic → Hierarchical connector



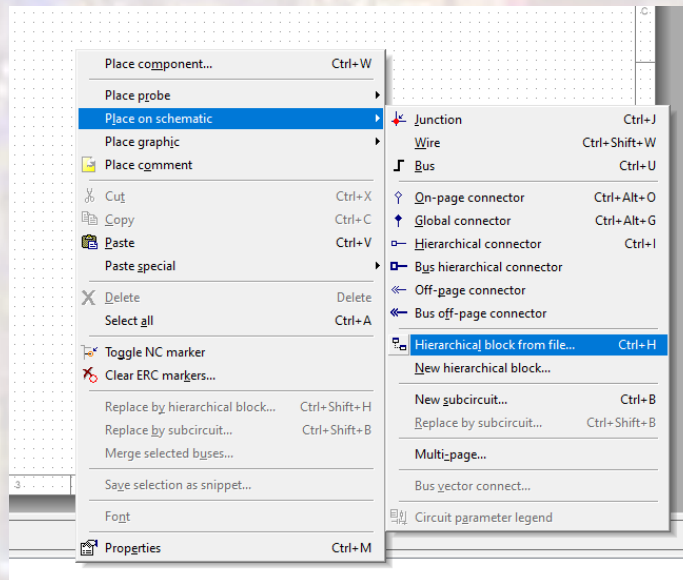
Hierarchical Design

- Open a new MSOE template schematic
 - Edit the description in the Title Block

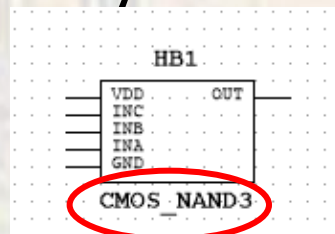


Hierarchical Design

- Rt-Click and select Place on schematic → Hierarchical block from file ...

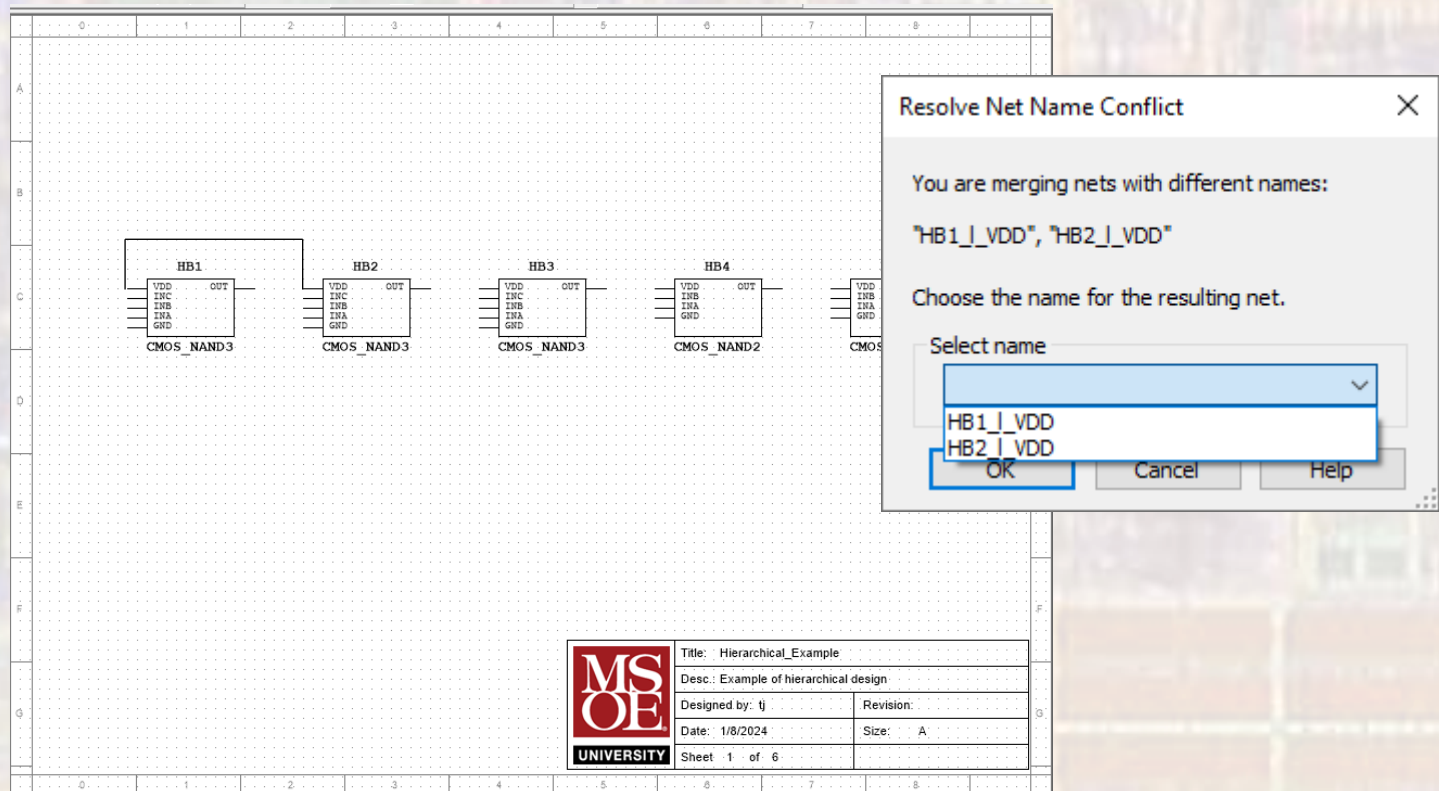


- Select the file you want to create a block for



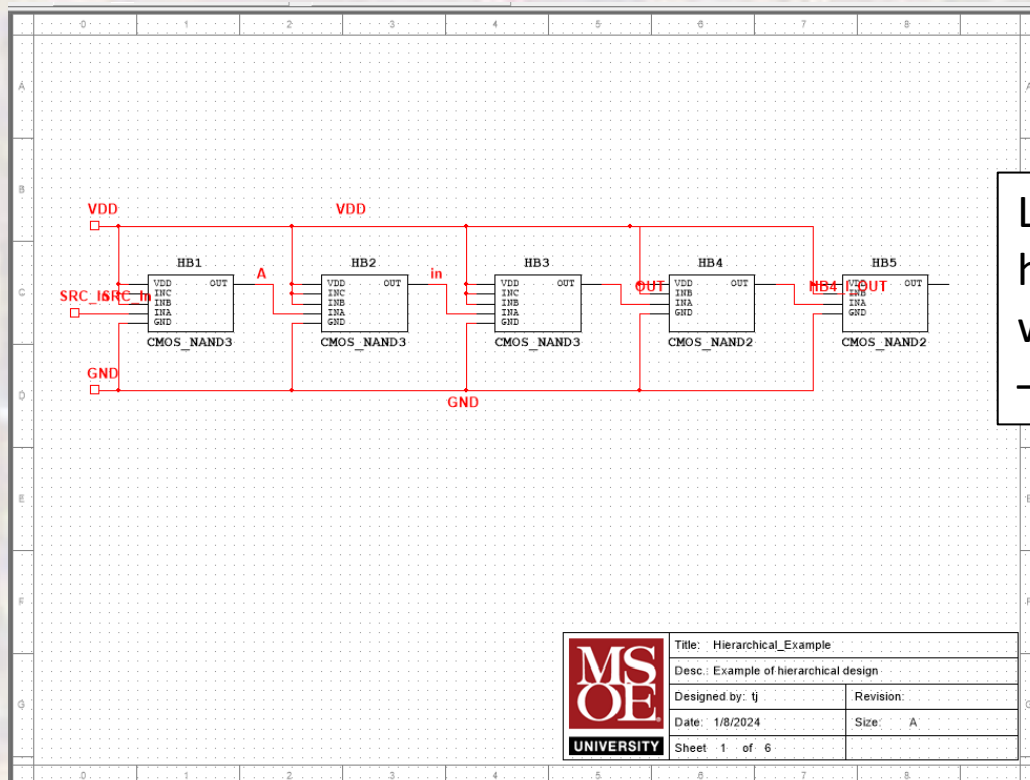
Hierarchical Design

- Repeat as necessary
- When you start wiring blocks – you will be asked to choose which net name you want to use – this is up to you



Hierarchical Design

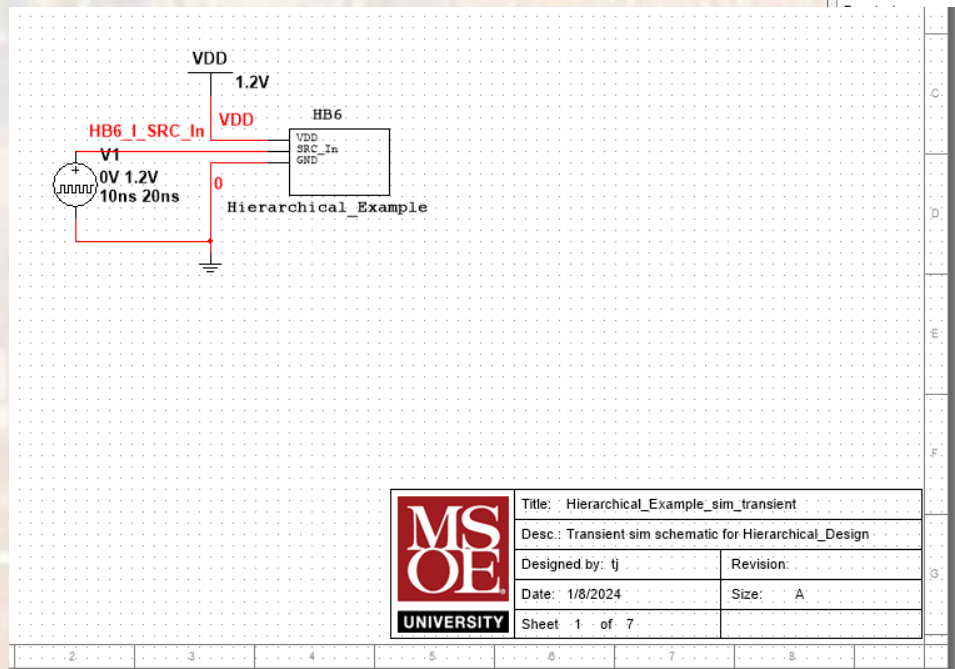
- Use hierarchical connectors for the external connections
- You can change the net names by double-clicking on them and changing the names



Labels are very hard to work with in MultiSim – do your best

Hierarchical Design

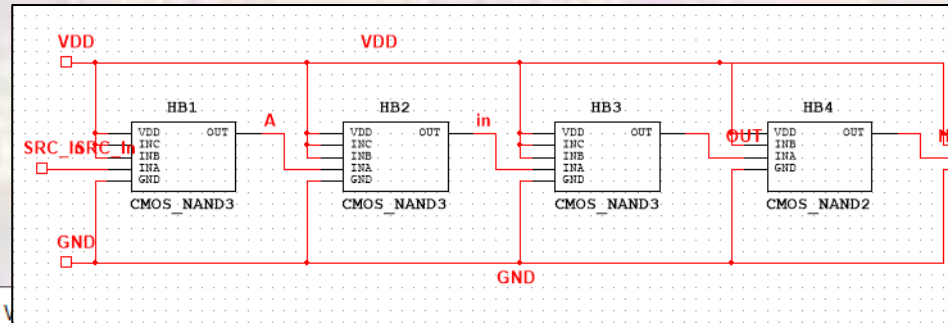
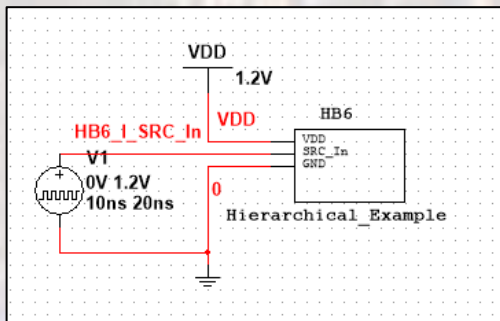
- Create simulation specific schematics as necessary
 - Placing your new hierarchical design in the simulation schematic
 - Note – simulation outputs are now referenced hierarchically



The screenshot shows the 'Analyses and Simulation' dialog box with the 'DC Operating Point' analysis selected. The 'Variables in circuit' list includes V(hb5_l_out) and V(vdd). The 'Selected variables for analysis' list includes V(hb6_l_a), V(hb6_l_in), V(hb6_l_out), and V(hb6_src_in), which are circled in red. The 'Show all device parameters at end of simulation in the audit trail' checkbox is checked.

Hierarchical Design

- Simulate



Analyses and Simulation

Active Analysis:

- Interactive Simulation
- DC Operating Point
- AC Sweep
- Transient
- DC Sweep
- Single Frequency AC
- Parameter Sweep
- Noise
- Monte Carlo
- Fourier
- Temperature Sweep
- Distortion
- Sensitivity
- Worst Case
- Noise Figure
- Pole Zero
- Transfer Function
- Trace Width
- Batched
- User-Defined

DC Operating Point

Output Analysis options Summary

Variables in circuit:

- All variables
- I(V1)
- I(VDD)
- P(V1)
- P(VDD)
- V(1)
- V(2)
- V(3)
- V(4)
- V(5)
- V(6)
- V(7)
- V(8)
- V(hb1_gnd)
- V(hb2_gnd)
- V(hb3_gnd)
- V(hb4_out)
- V(hb5_out)
- V(vdd)

Selected variables for analysis:

- All variables
- V(hb6_l_a)
- V(hb6_l_in)
- V(hb6_l_out)
- V(hb6_src_in)

More options

- Show all device parameters at end of simulation in the audit trail
- Select variables to save...

Run Save Cancel Help

