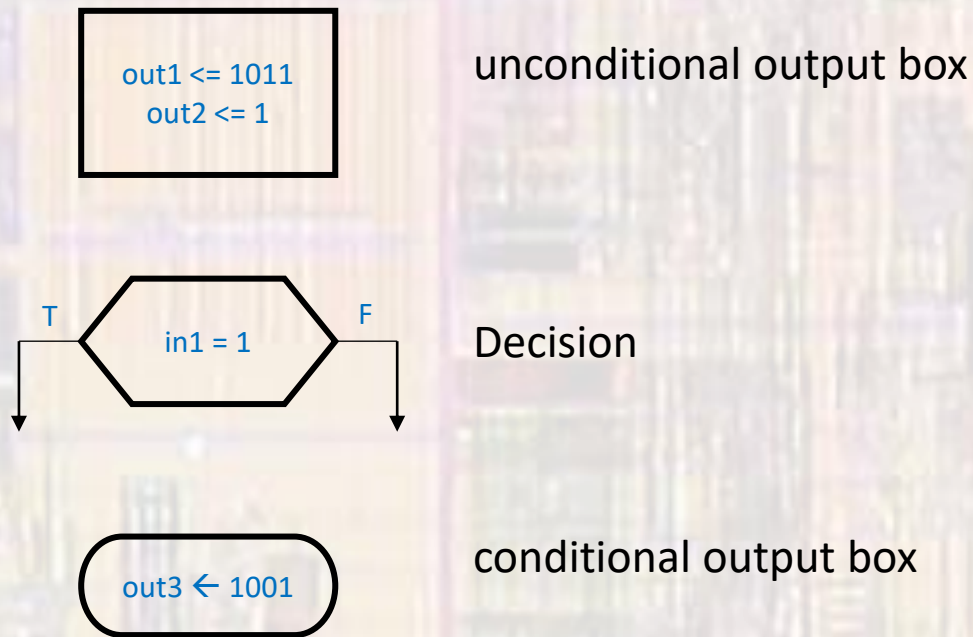# Algorithmic State Machine Charts

Last updated 7/18/23
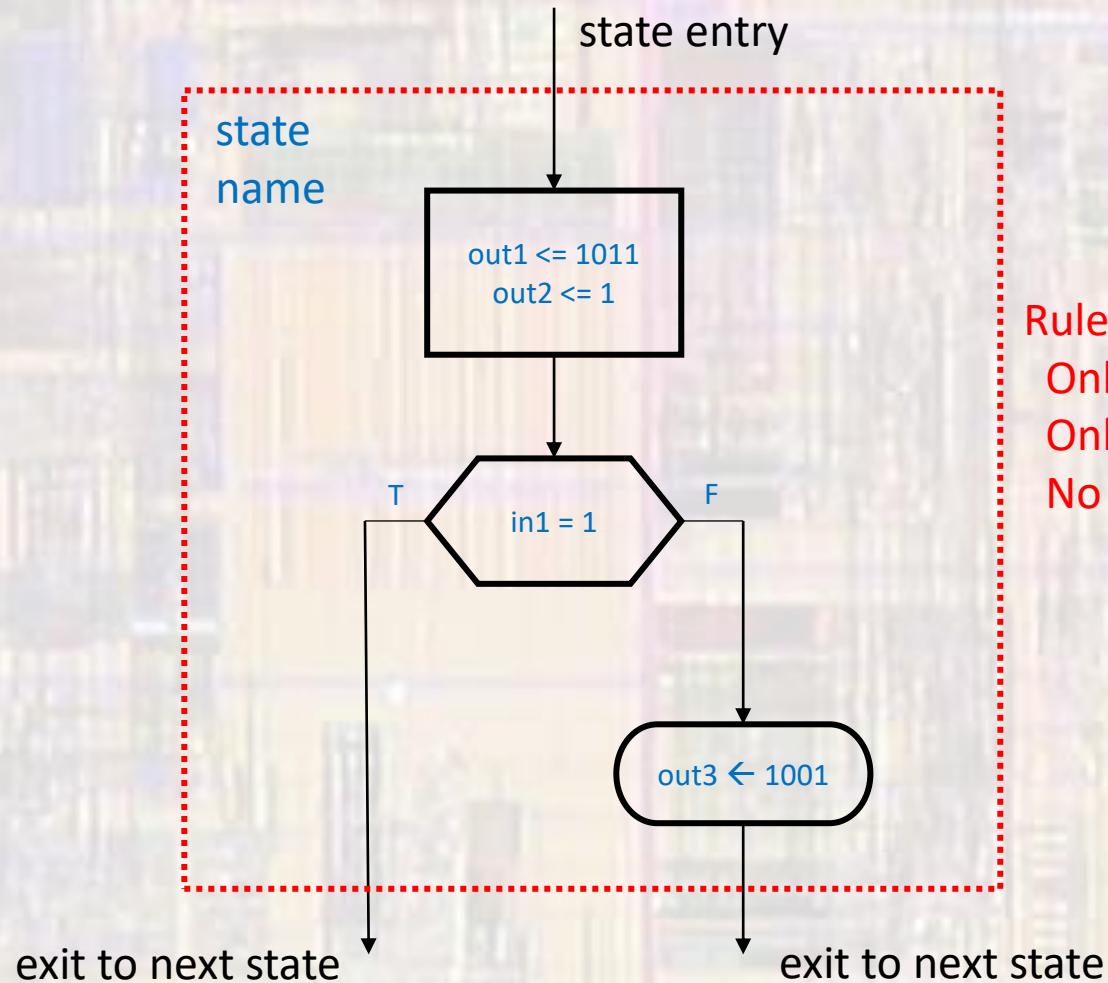
ASM Charts

- ## Algorithmic State Machine Chart (ASM)

  - ## Alternative representation to a State Diagram

out1 <= 1011
out2 <= 1

unconditional output box

T   in1 = 1   F

Decision

out3 ← 1001

conditional output box

ASM Charts

- Algorithmic State Machine Chart (ASM)

state entry

state
name

out1 <= 1011
out2 <= 1

T   in1 = 1   F

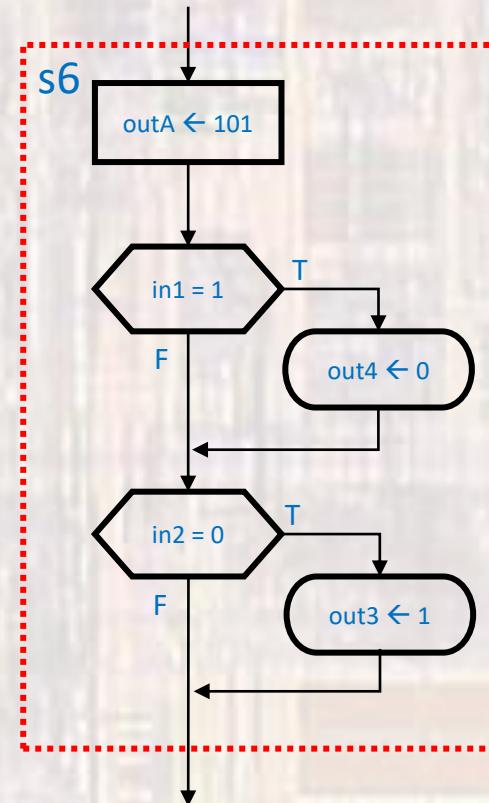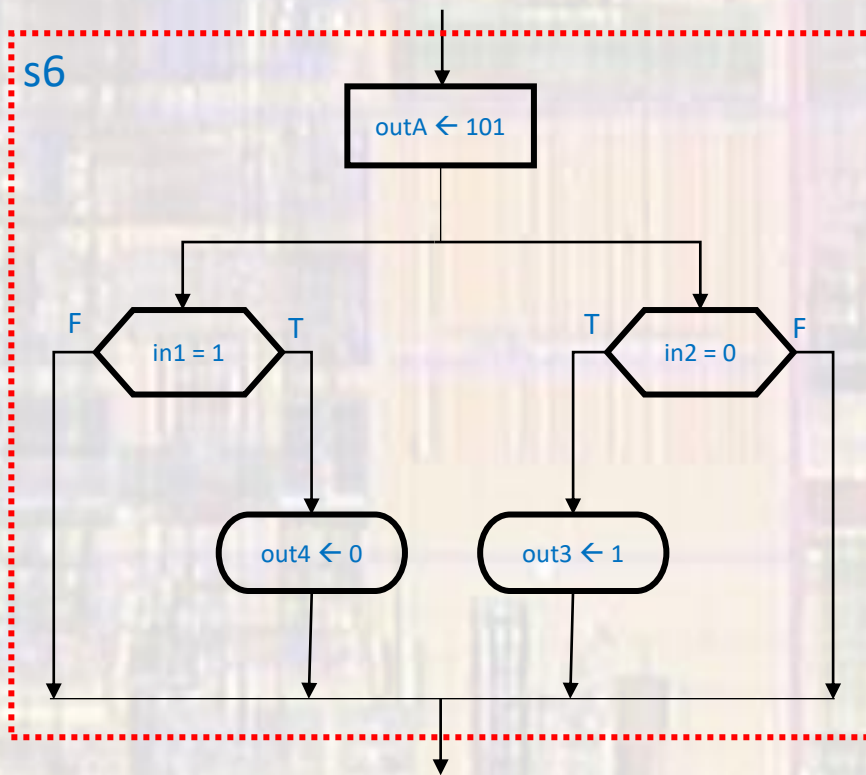out3 ← 1001

exit to next state   exit to next state

Rules:
Only one input path
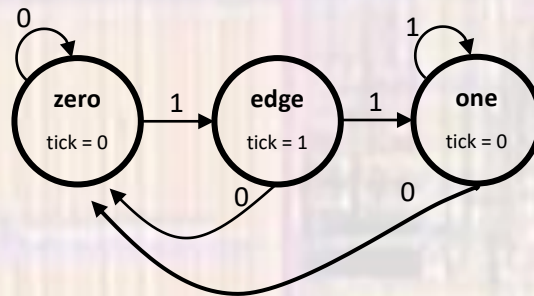Only one valid output path
No internal feedback

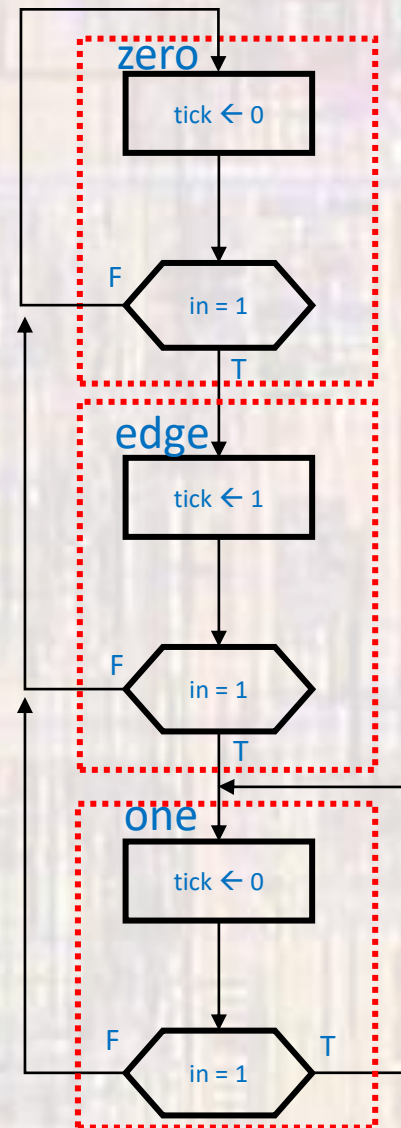# ASM Charts

- Algorithmic State Machine Chart (ASM)
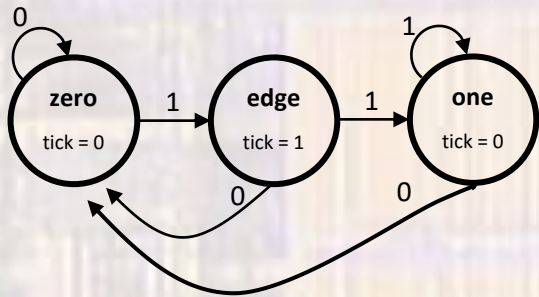
ASM Charts

- Edge Detector

  - Rising edge

5

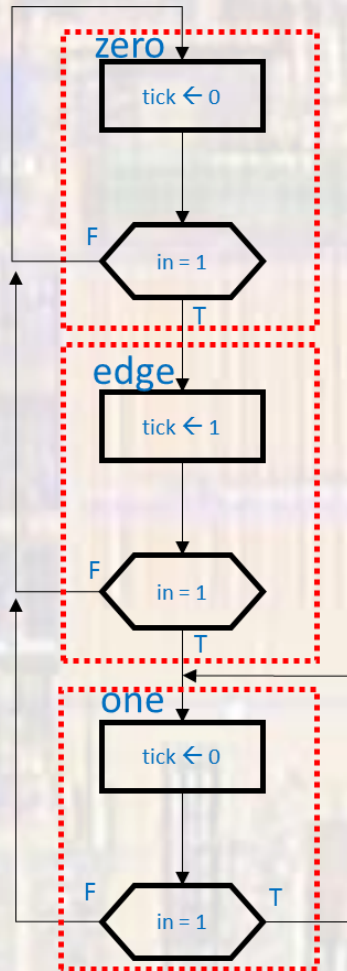# ASM Charts

- Edge Detector

© tj

ASM Charts
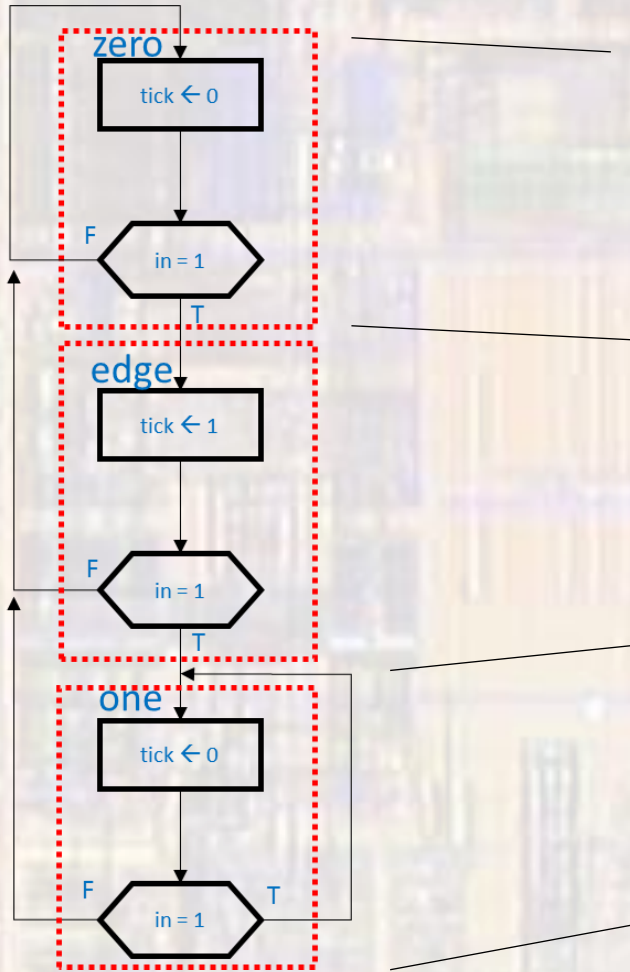
- Edge Detector


```
process(all)
begin
    case state is
        when zero =>
            tick <= '0';
            if in= '1' then
                state_next <= edge;
            else
                state_next <= zero;
            end if;
        when edge =>
            tick <= '1';
            if in= '1' then
                state_next <= one;
            else
                state_next <= zero;
            end if;
        when one =>
            tick <= '0';
            if in= '1' then
                state_next <= one;
            else
                state_next <= zero;
            end if;
    end case;
end case;
```

ASM Charts

- Edge Detector


```vhdl
-- Next state logic
process(all)
  begin
    case state is
      when zero =>
        if in= '1' then
          state_next <= edge;
        else
          state_next <= zero;
        end if;
      when edge =>
        if in= '1' then
          state_next <= one;
        else
          state_next <= zero;
        end if;
      when one =>
        if in= '1' then
          state_next <= one;
        else
          state_next <= zero;
        end if;
    end case;
```

```vhdl
-- Output logic

process(all)
  begin
    case state is
      when zero =>
        tick <= '0';
      when edge =>
        tick <= '1';
      when one =>
        tick <= '0';
    end case;
```