

Clocks and Clock Distribution

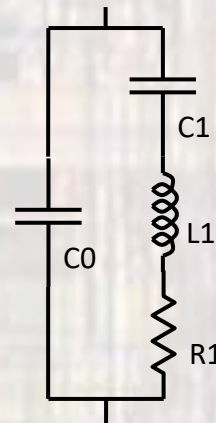
Last updated 8/23/23

Clock Generation

- Crystal Oscillator

- Piezoelectric Effect

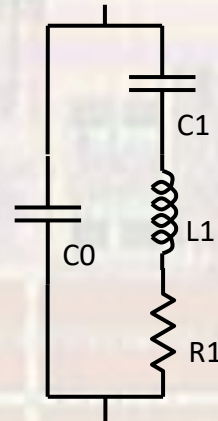
- Quartz is a piezoelectric material
 - When an electric field is placed upon it, a physical displacement occurs
 - Equivalent electrical circuit represents the mechanical properties of the crystal



Clock Generation

- Crystal Oscillator

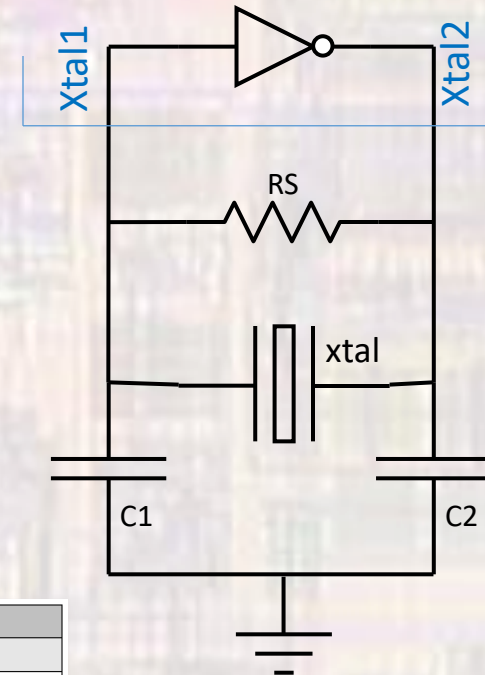
- C1 models the motional arm capacitance measured in Farads.
 - It represents the elasticity of the quartz, the area of the electrodes on the face, thickness and shape of the quartz wafer
 - Values of C1 range in femtofarads
- L1 represents motional arm inductance measured in Henrys.
 - It represents the vibrating mechanical mass of the quartz in motion
 - Low frequency crystals have thicker and larger quartz wafers and range in a few Henrys
 - High frequency crystals have thinner and smaller quartz wafers and range in a few millihenrys
- R1 represents resistance measured in Ohms.
 - It represents the real resistive losses within the crystal
 - Values of R1 range from 10Ω for 20 MHz crystals to $200K\Omega$ for 1 kHz crystals.
- C0 represents shunt capacitance measured in farads.
 - It is the sum of capacitance due to the electrodes on the crystal plate plus stray capacitances due to the crystal holder and enclosure
 - Values of C0 range from 3 to 7 pF



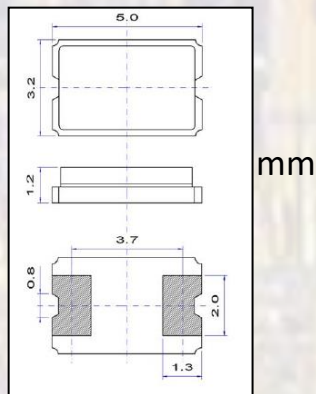
Clock Generation

• Pierce Oscillator

- R_s biases the inverter into its linear region
- Xtal – appears as a high Q inductor
- C_1 , Xtal, C_2 form a Pi network BPF \rightarrow 180° phase shift
- 180° from the Pi network + 180° from the inverter
 \rightarrow positive feedback
- positive feedback on the bias resistor causes the inverter to be unstable \rightarrow oscillation



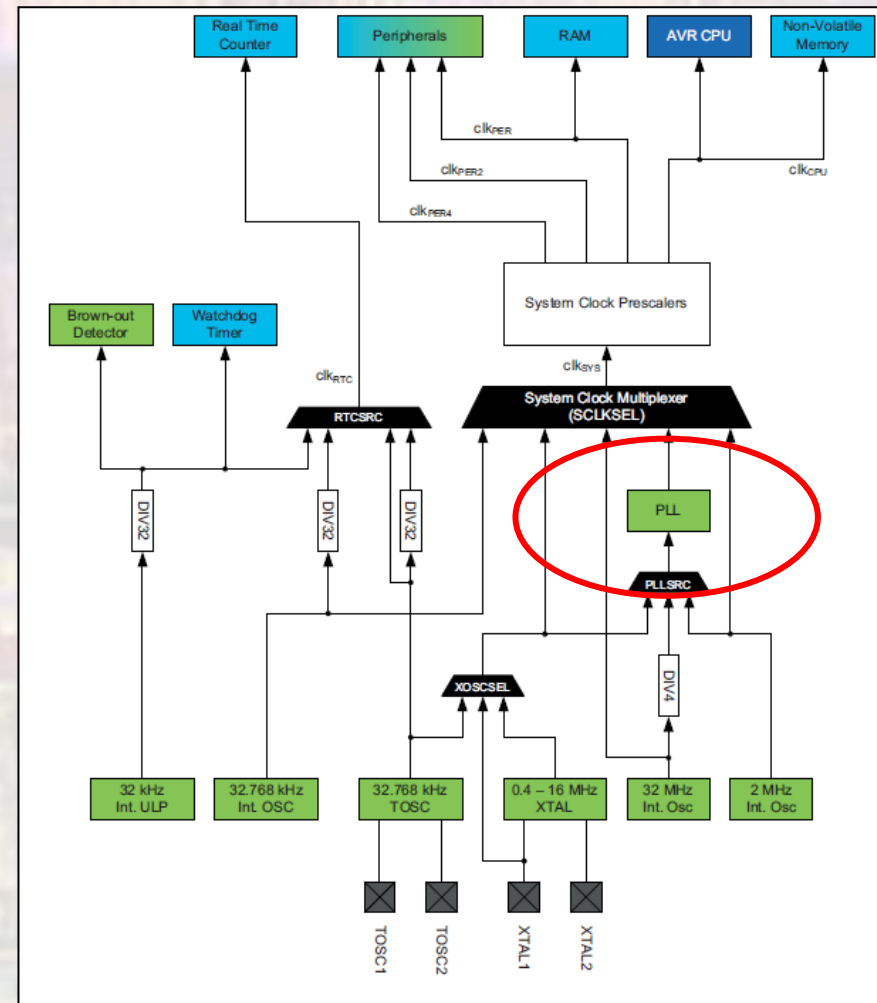
• Xtal Specifications



Parameter	Specification	
Frequency range	8 ~ 67 MHz	fundamental
Mode of oscillation	AT-cut	
Standard frequencies	8.00, 13.00, 16.00, 19.20, 20.00, 24.576, 25.00 & 32.00 MHz	
Frequency tolerance	$\pm 25 \sim \pm 50$ ppm	@ +25 °C
Frequency stability	$\pm 10 \sim \pm 50$ ppm	vs. operating temperature range
Aging	± 2 ppm	1 st year
Load capacitance	series or parallel resonance (CL = 8 ~ 32 pF)	
Equivalent series resistance (ESR)	< 12 Ω	@ 16 MHz
	< 10 Ω	@ 32 MHz
Drive level	10 ~ 100 μ W	
Operating temperature range	-20 ~ +70 °C	
	-40 ~ +85 °C	
	-40 ~ +125 °C	
Storage temperature range	-55 ~ +125 °C	
Packaging unit	tape & reel	1'000 or 2'000 pieces
Customer specifications on request		

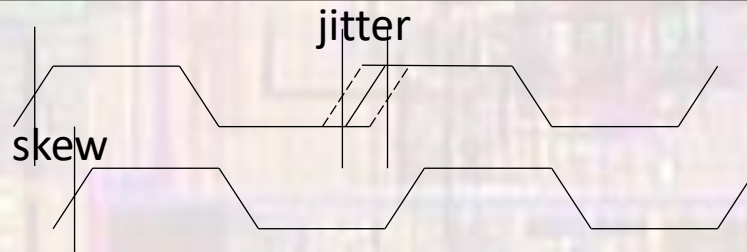
Clock Generation

- Advanced Clock Systems
 - Typical systems include a frequency synthesizer capability
 - Want to program the frequency based on a fixed input frequency
 - Xtal freq \rightarrow PLL \rightarrow desired clock
 - Some systems use an internal frequency generation circuit
 - Usually less accurate but cheap



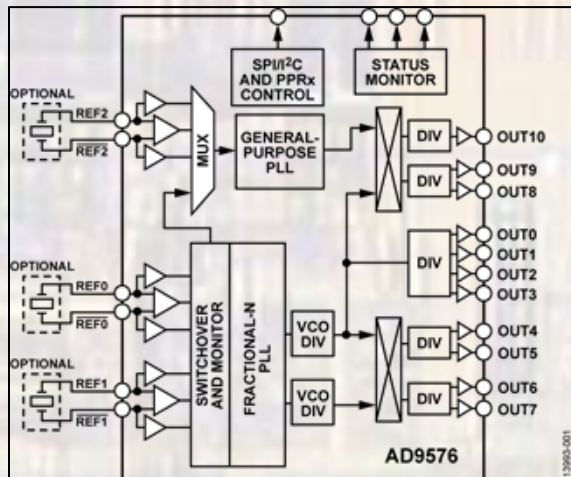
Clock Characteristics

- Frequency
- Duty Cycle
- Jitter
 - Small variations in the clock edge timing relative to the ideal clock edge
 - Impacts effective duty cycle
 - Creates a noise effect in timing circuits (esp. ADCs and high speed ports)
 - If bad enough – has same impact as Skew
- Skew
 - Difference between clock edge timing at different locations in the system
 - Can lead to missed logic transition capture in synchronous systems
 - Typically caused by
 - Differences in wire lengths
 - Differences in load impedances
 - Differences in driver output impedances when multiple drivers used



Clock Distribution

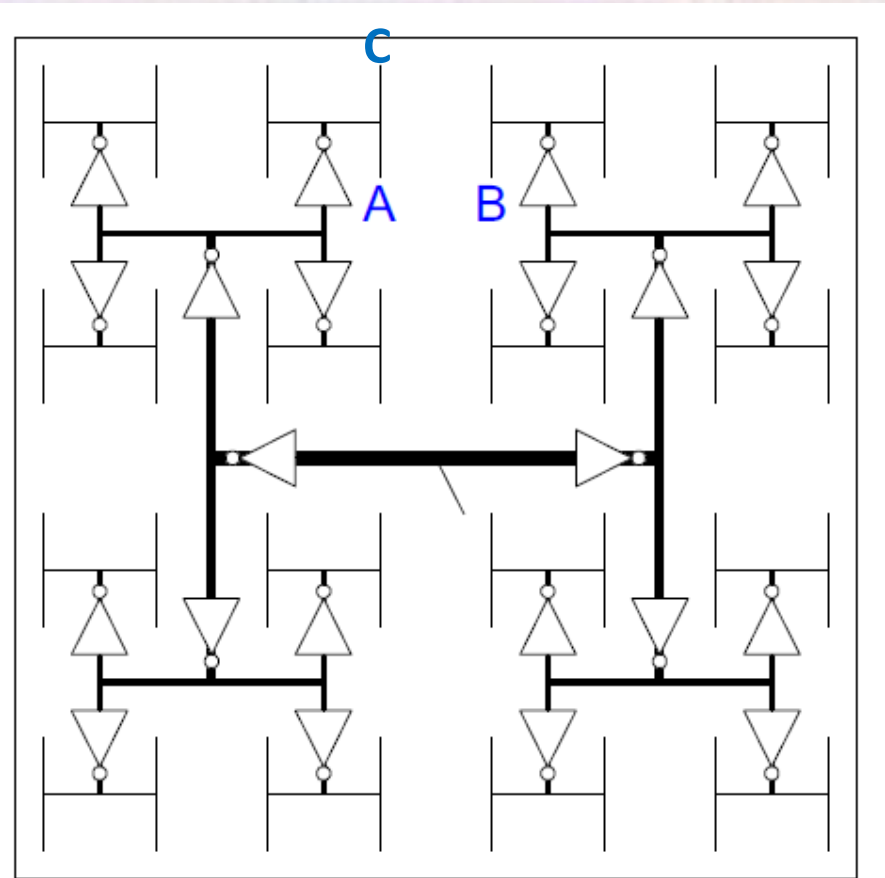
- Board Level / System Level
 - Partition the design so that clock synchronization (no skew) is not required between components or boards
 - If synchronization is required
 - Short, balanced traces may work – but very tricky due to input impedances shifting over temp, components, ...
 - Use a special clock generation/distribution part
 - PLL based chip solution
 - Still requires careful signal routing



- Single, low phase noise, fully integrated VCO/fractional-N PLL core
 - VCO range: 2375 MHz to 2725 MHz
 - Integrated loop filter (requires a single external capacitor)
 - 2 differential, XTAL, or single-ended reference inputs
 - Reference monitoring capability
 - Automatic redundant XTAL switchover
 - Minimal transient, smooth switching
 - Typical RMS jitter
 - <0.3 ps (12 kHz to 20 MHz), integer-N translations
 - <0.5 ps (12 kHz to 20 MHz), fractional-N translations
- Single, general-purpose, fully integrated VCO/integer-N PLL core
 - VCO range: 750 MHz to 825 MHz
 - Integrated loop filter
 - Independent, duplicate reference input or operation from the fractional-N PLL active reference input
 - Input frequency: 25 MHz
 - Preset frequency translations via pin strapping (PPRx)
 - 25 MHz, 33.33 MHz, 50 MHz, 66.67 MHz, 100 MHz, 133.33 MHz, 200 MHz, or 400 MHz
 - Up to 3 copies of reference clock output
 - 11 pairs of configurable differential outputs

Clock Distribution

- Chip Level (incl FPGA)
 - H-Tree
 - Fractal structure
 - Match line lengths
 - Match loads
 - Match # of buffer levels
 - A and C – very low skew
 - A and B – low skew



Clock Distribution

- Chip Level (incl FPGA)
 - Mesh
 - Grid
 - All clocks driven from a single signal
 - Requires careful matching of line impedances
 - A and C – very low skew
 - A and B – low skew
 - Hybrid
 - Combine H-Tree and Mesh

