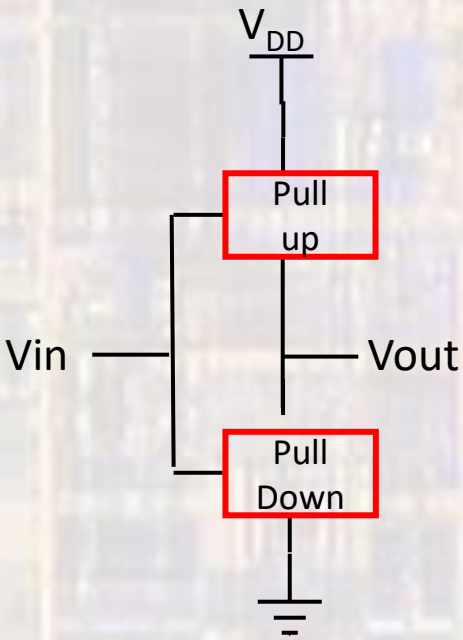
CMOS Area

Last updated 12/23/23

CMOS Area

- Gate Concepts



We can generalize our inverter results to account for more complex gates

Make the effective $(W/L)_{pull\text{-}up} = 3 \times (W/L)_{pull\text{-}down}$

Mid supply switching point

Equivalent rise and fall times

Remember the L of all devices is the same

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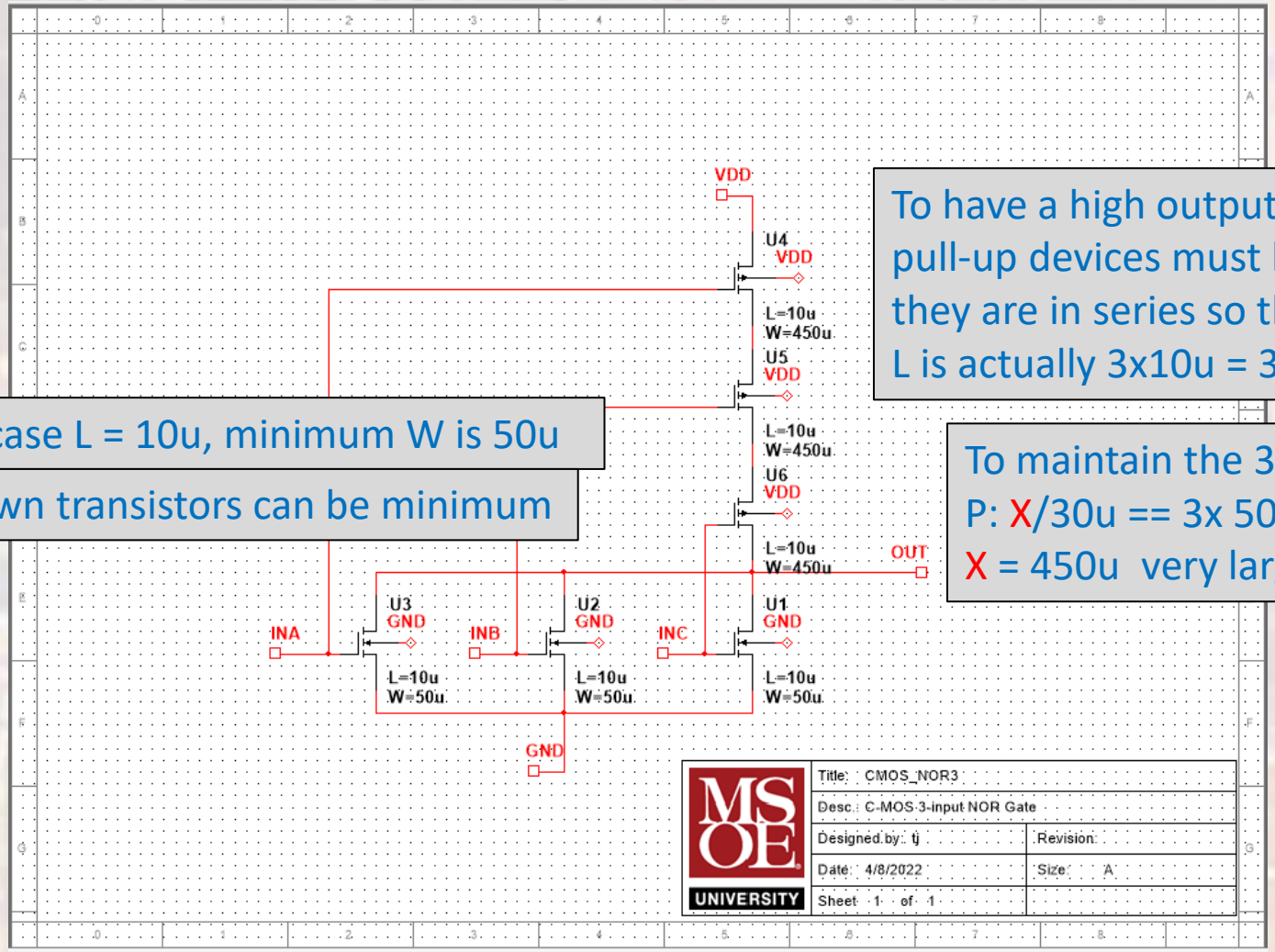
- NOR – Minimum with matched $T_R/T_F/V_{SW}$



To have a high output, all 3 pull-up devices must be on – but they are in series so the effective L is actually 3x10u = 30u

In this case L = 10u, minimum W is 50u

Pull-down transistors can be minimum

To maintain the 3x ratio
P: X/30u == 3x 50u/10u
X = 450u very large !

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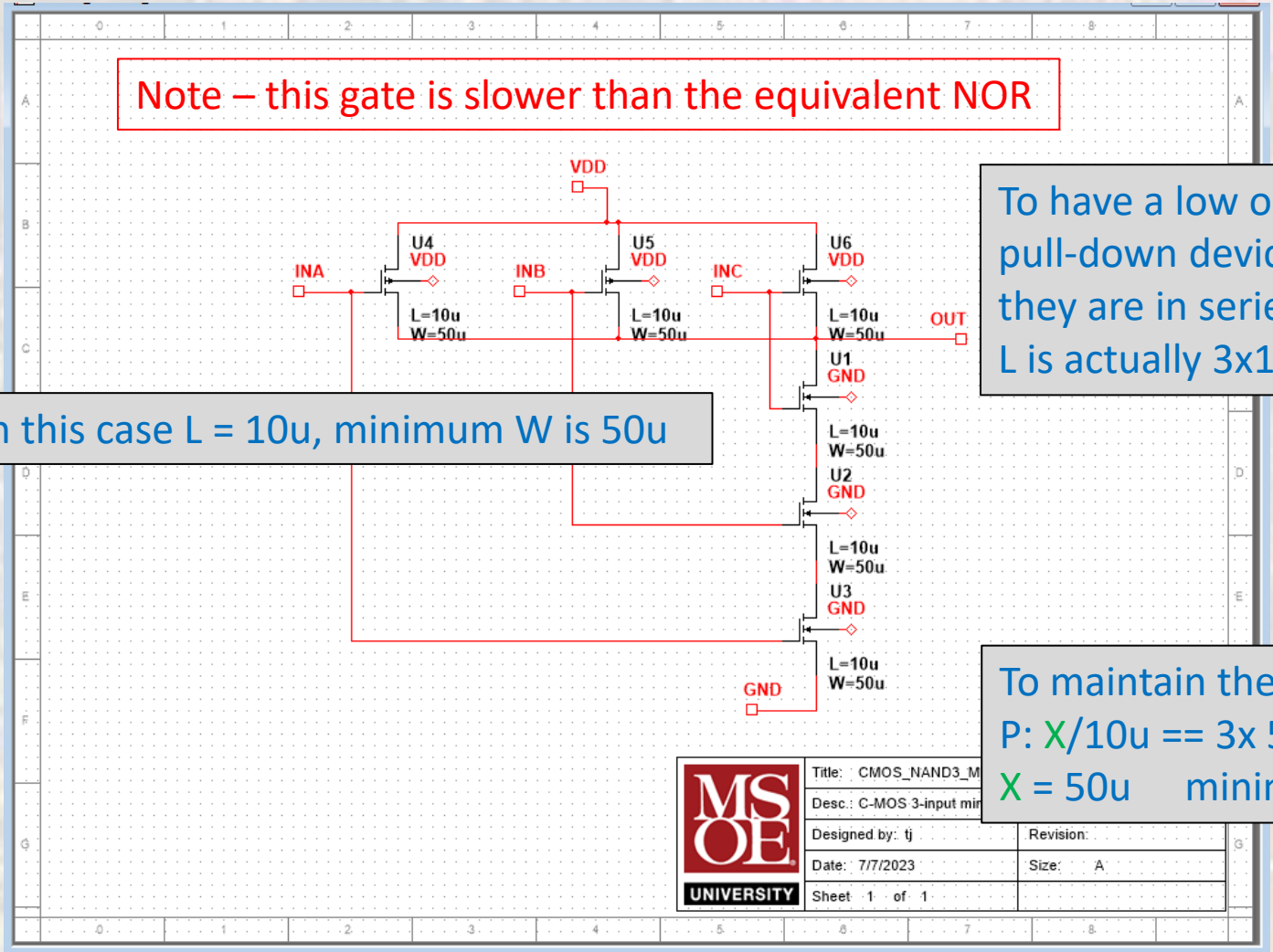
- NAND – Minimum with matched $T_R/T_F/V_{SW}$



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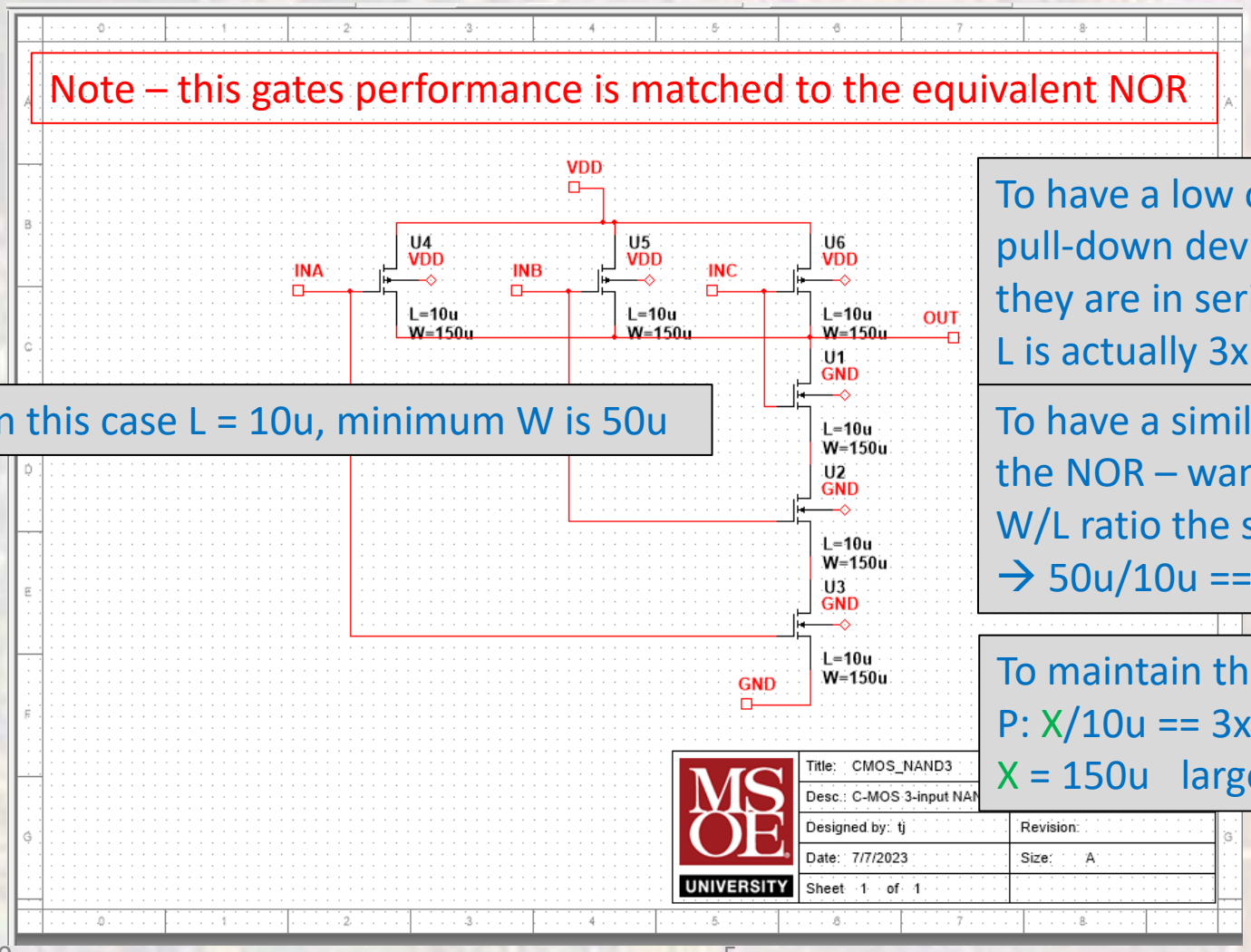
- NAND – Matched to minimum NOR (similar delays)



To have a low output, all 3 pull-down devices must be on, but they are in series so the effective L is actually 3x10u = 30u

To have a similar gate delay as the NOR – want the pull-down W/L ratio the same as the NOR → 50u/10u == X/30u → X = 150u

To maintain the 3x ratio
P: X/10u == 3x 150u/30u
X = 150u large!

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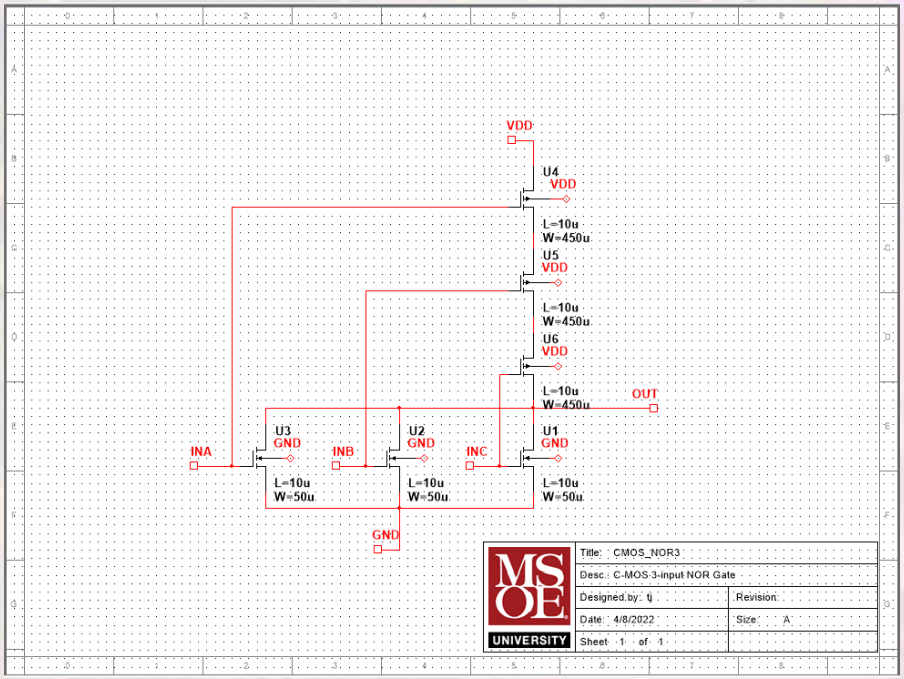
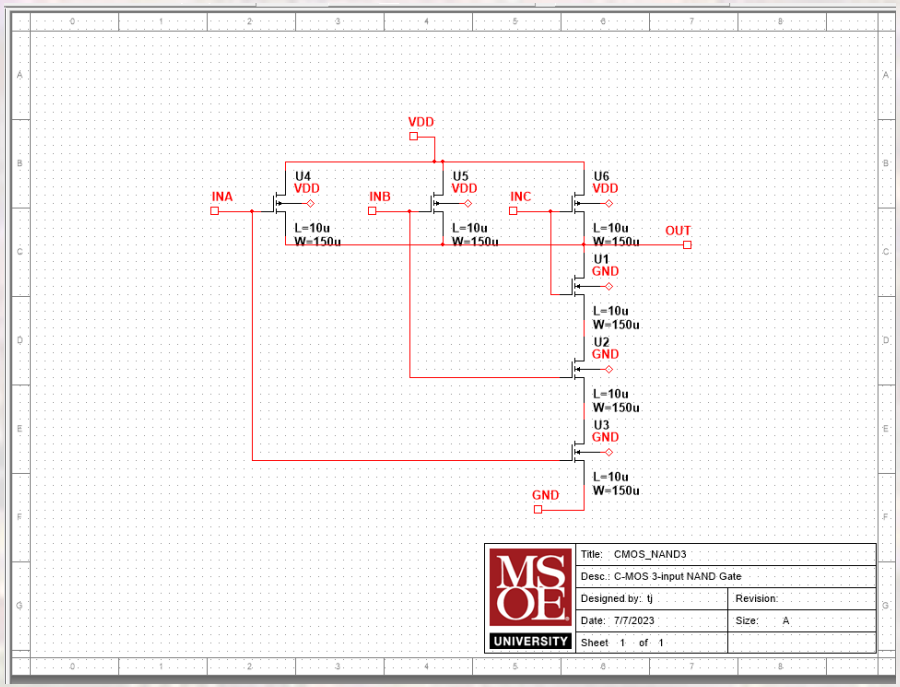
- Matched delay NAND/NOR





Total transistor gate area
15,000u^2

Total transistor gate area
9,000u^2

NAND gates preferred
over NOR gates for area

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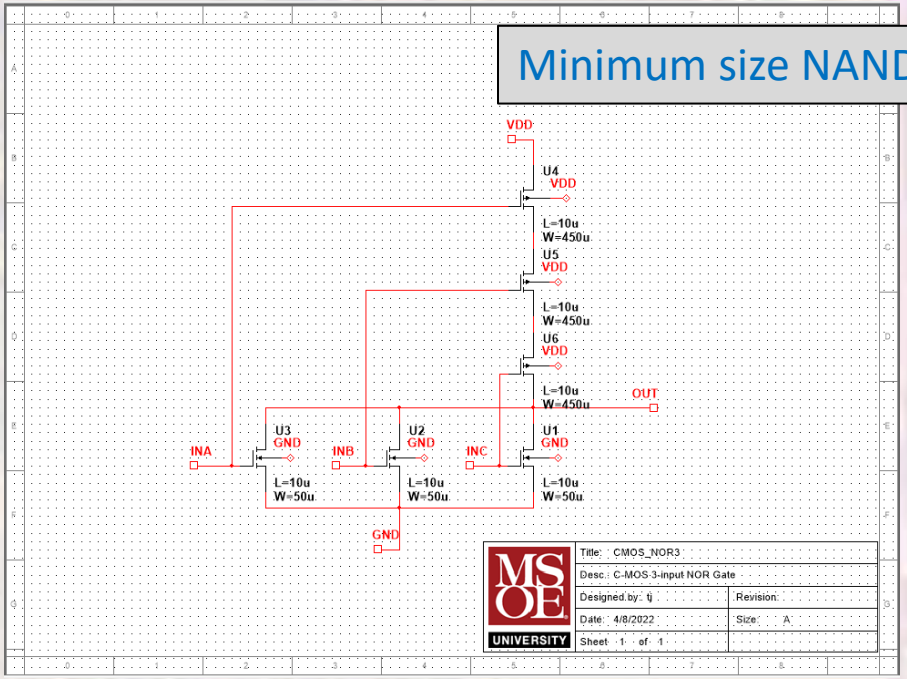
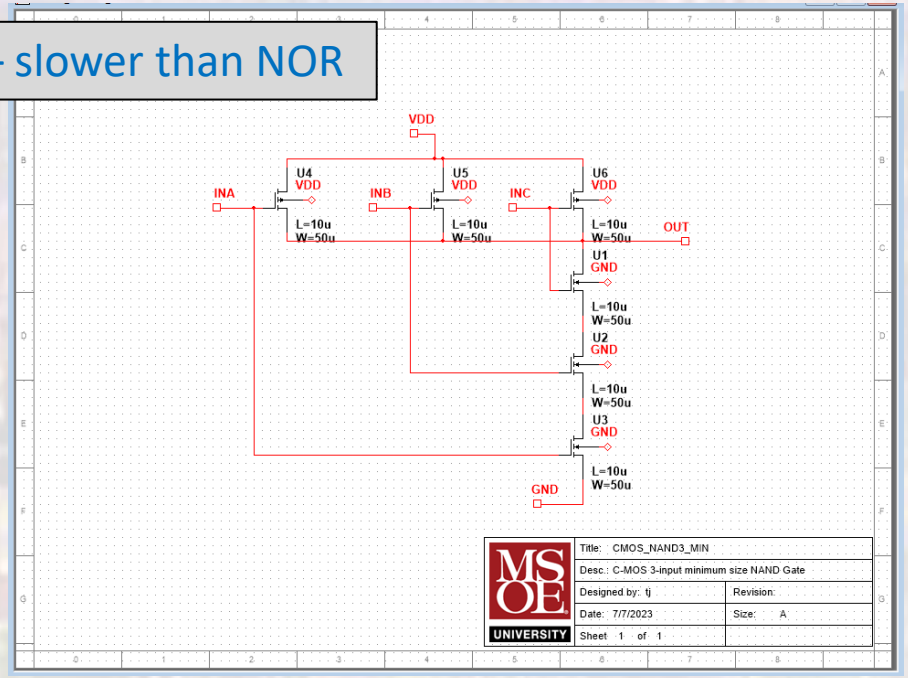
- Mis-Matched Delay NAND/NOR
  - still midpoint switching

Minimum size NAND – slower than NOR





Total transistor gate area
15,000u^2

NAND gates preferred
over NOR gates for area

but

Total transistor gate area
3,000u^2

NOR gates preferred
over NAND gates for speed

CMOS Area

- Gate AREA Equivalence
  - Use a minimum 2 input NAND gate as a reference for size and loading
  - Mismatched NAND/NOR delays
  - Midpoint switching

Overhead ignored
(contacts, power, …)

Relative Size

2 input NAND gate area = 2500u^2 = 1 NAND equivalent

INV gate area = 2000u^2 = 0.8 NAND Eq.
2 input NOR gate area = 7000u^2 = 2.8 NAND Eq.
3 NOR = 6 NAND eq.
4 NOR = 10.4 NAND eq.
3 NAND = 1.2 NAND eq.
4 NAND = 2.4 NAND eq.

This is a specific example
These ratios will depend on
A lot of design factors

Input Load (relative capacitance – 1 input)

2 input NAND gate area/input = 1250u^2 = 1 NAND equivalent

INV gate area/input = 1000u^2 = 0.8 NAND Eq.
2 input NOR gate area/input = 3500u^2 = 2.8 NAND Eq.
3 NOR/input = 4 NAND eq.
4 NOR/input = 5.2 NAND eq.
3 NAND/input = 0.8 NAND eq.
4 NAND/input = 1.2 NAND eq.