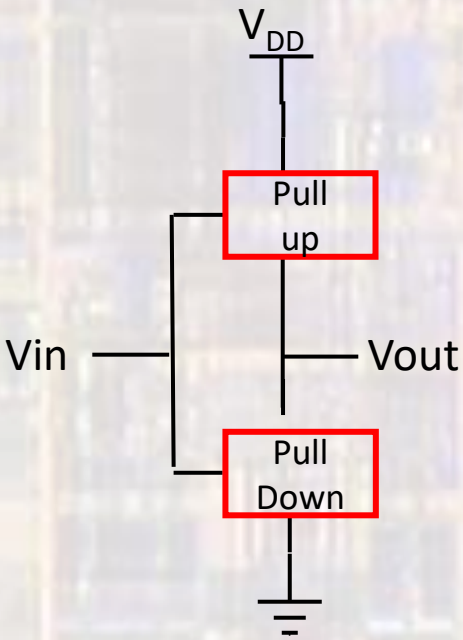
C-MOS Circuits

Last updated 12/29/23

C-MOS Circuits

- Gate Concepts



We can generalize our inverter results to account for more complex gates

Make the effective $(W/L)_{pull\text{-}up} = 3 \times (W/L)_{pull\text{-}down}$

Mid supply switching point

Equivalent rise and fall times

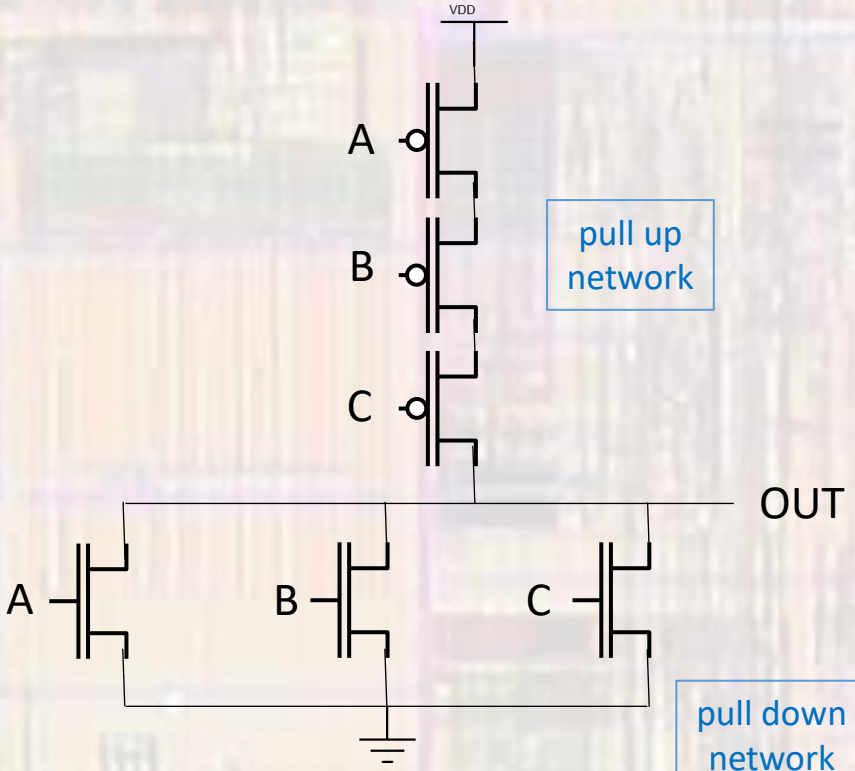
Remember the L of all devices is the same

$W_{pull\text{-}up} = 3 \times W_{pull\text{-}down}$

The ratio (3) is technology dependent

C-MOS Circuits

- C-MOS Gates - NOR

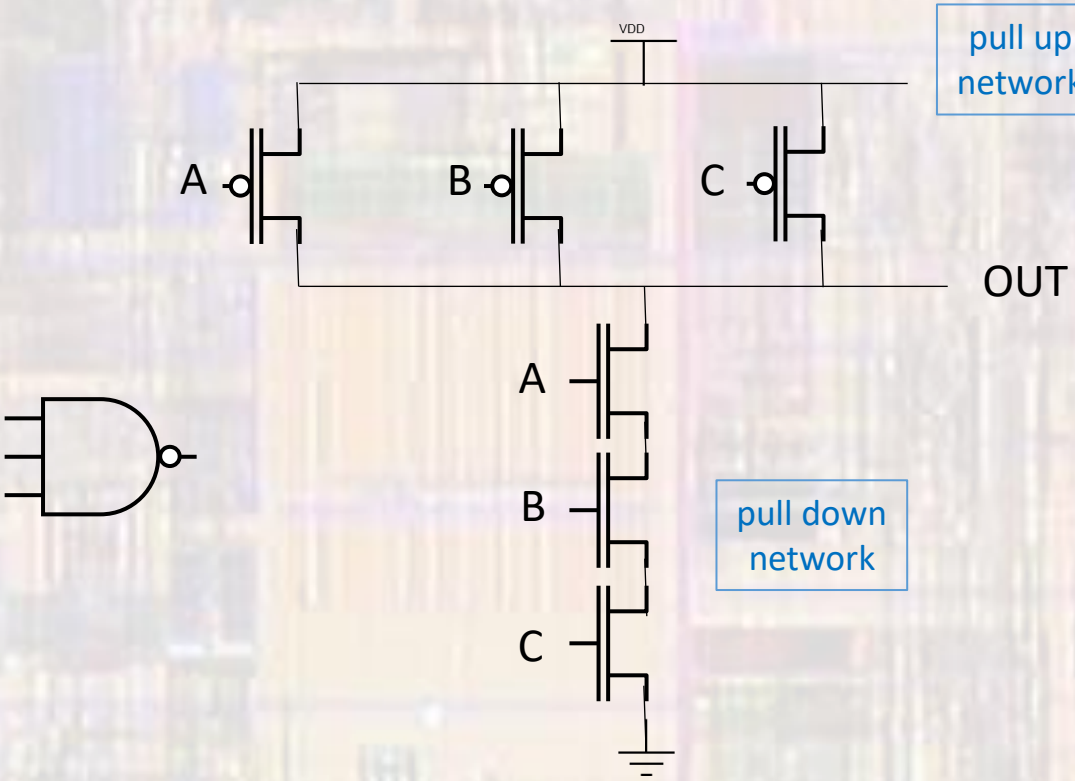


A	B	C	NOR OUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

If ANY input is high, pull-down is on, pull-up is off → output is low
If ALL inputs are low, pull-down is off, pull-up is on → output is high

C-MOS Circuits

- C-MOS Gates - NAND

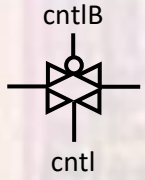


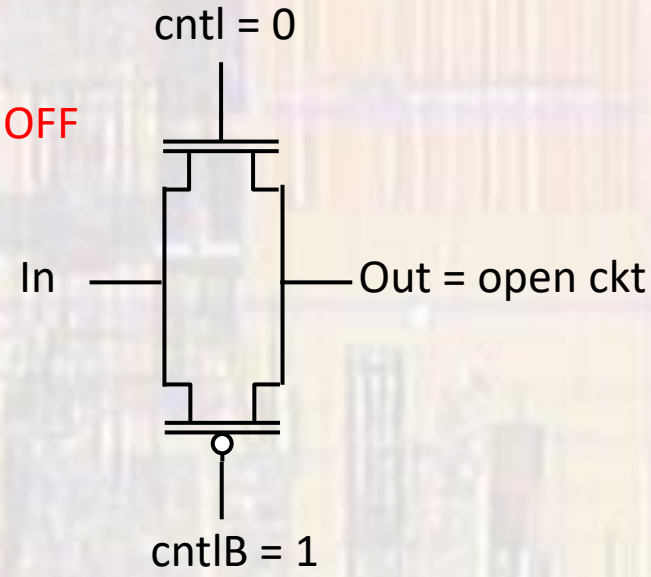
A	B	C	NAND OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

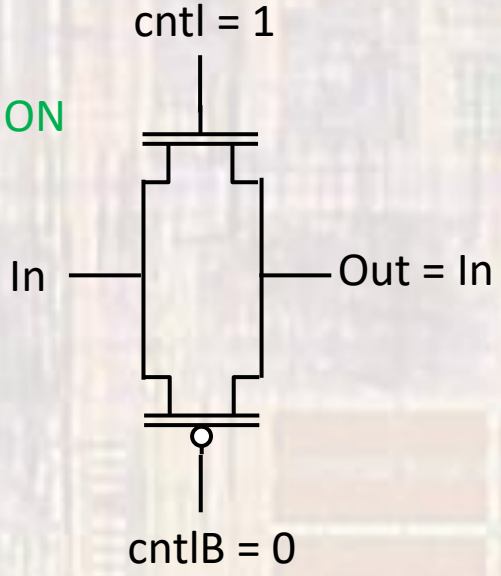
If ANY input is low, pull-up is on, pull-down is off → output is high
If ALL inputs are high, pull-up is off, pull-down is on → output is low

C-MOS Circuits

- C-MOS Transmission Gates
  - Use parallel P-MOS and N-MOS devices as a “pass gate”
    - Passes both ‘0’s and ‘1’s
    - Bi-directional
    - Requires cntl and cntlB

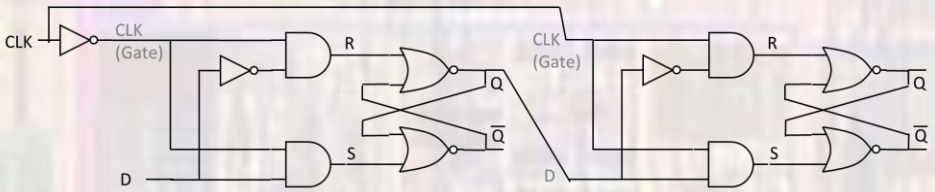




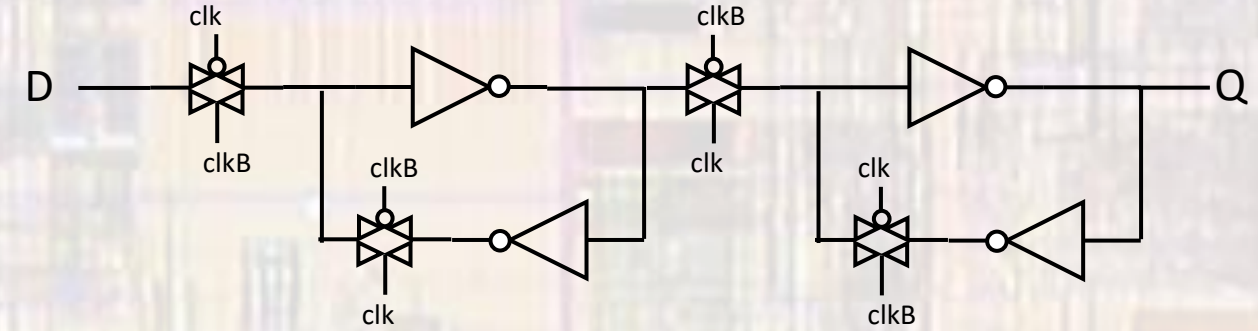


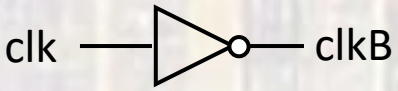
C-MOS Circuits

- C-MOS Flip-Flop
  - Logical Circuit
    - 2, SR latches
    - 19 NMOS, 19 PMOS



  - T-gate version
    - 9 NMOS, 9 PMOS

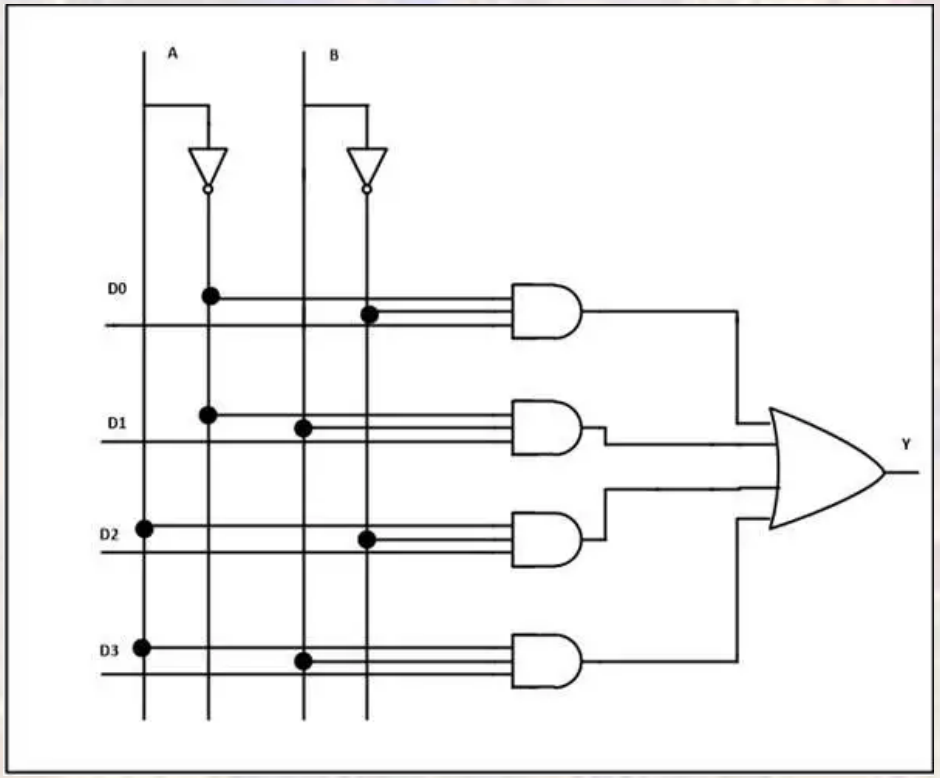




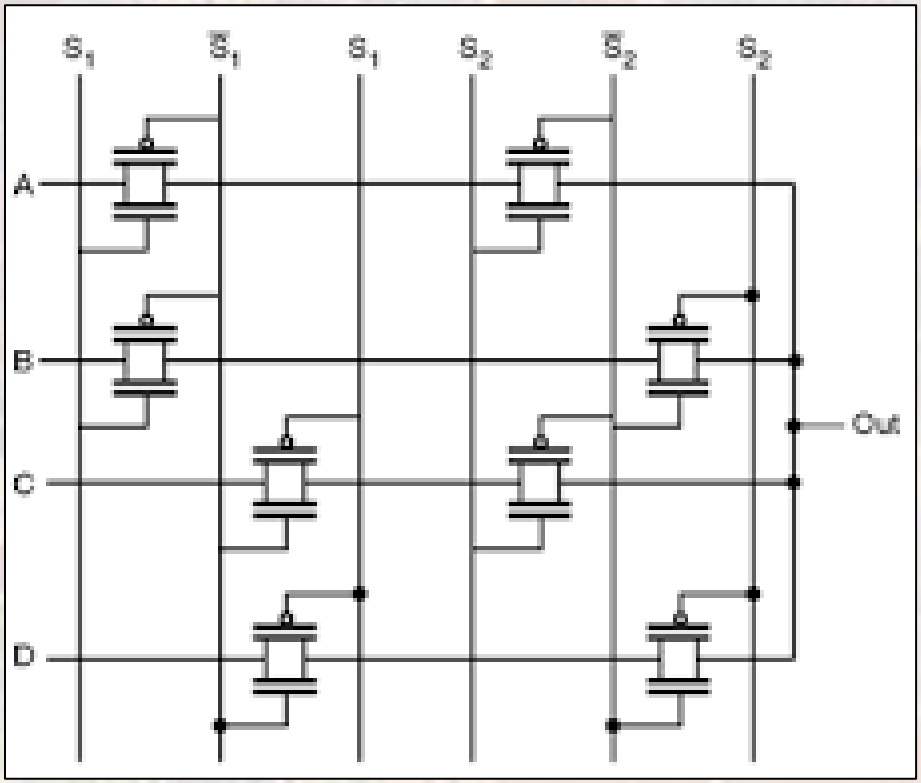
C-MOS Circuits

- C-MOS Mux: 4::1

19 N-Channel, 19 P-Channel



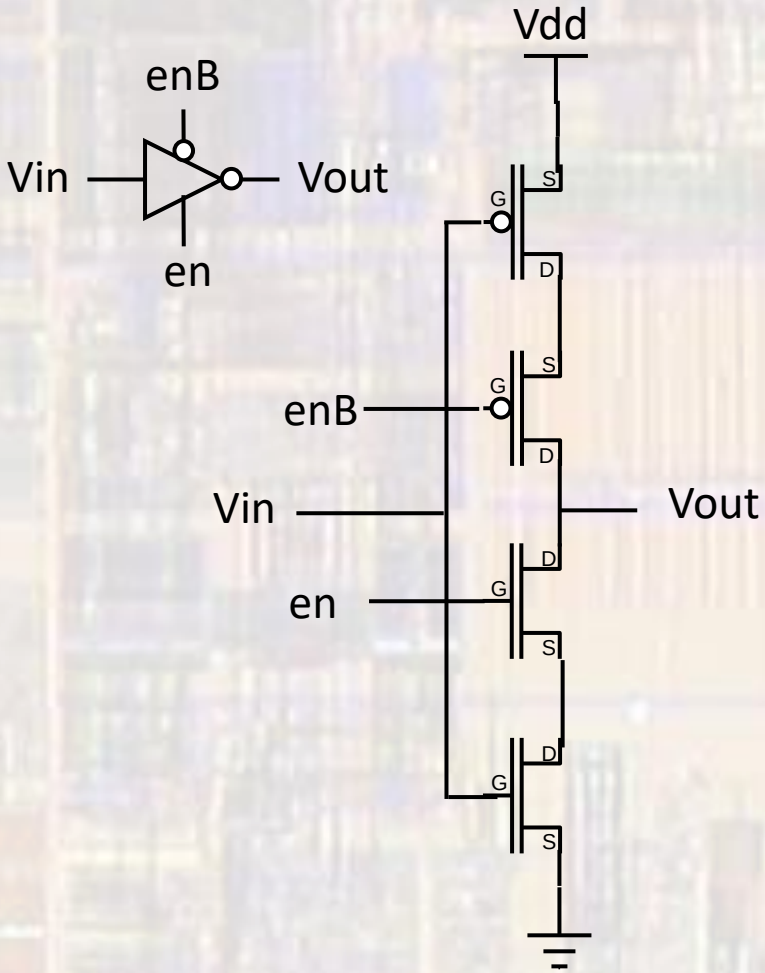
8 N-Channel, 8 P-Channel

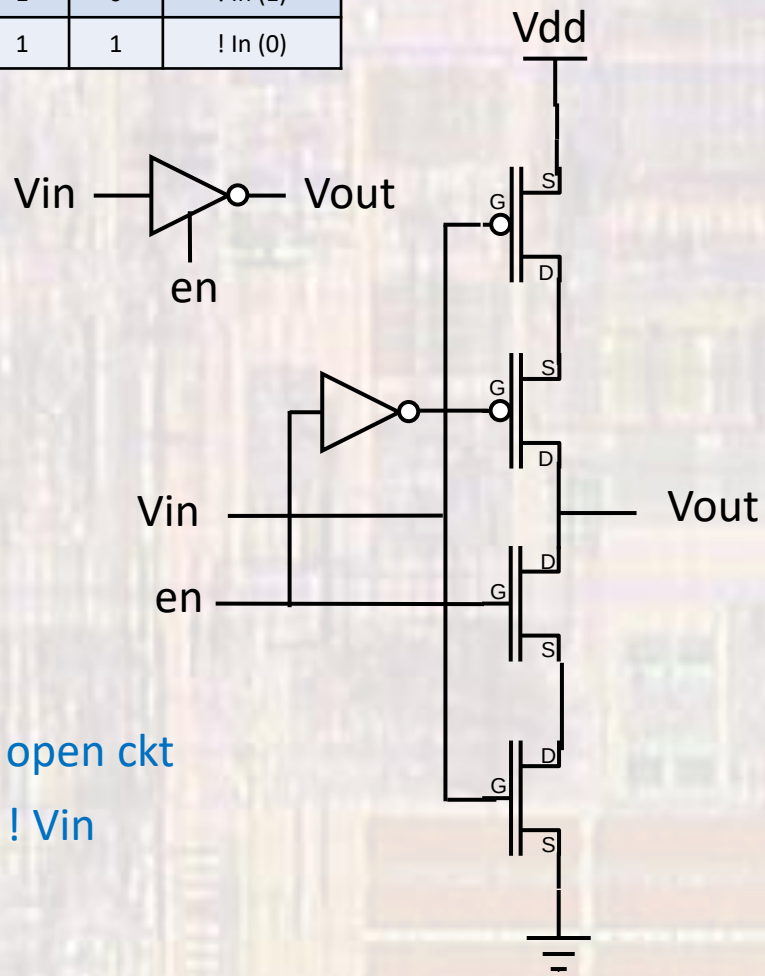


C-MOS Circuits

- C-MOS Tristate Inverter

en	in	OUT
0	0	Open ckt
0	1	Open ckt
1	0	! In (1)
1	1	! In (0)





en = 0 → Vout = open ckt

en = 1 → Vout = ! Vin