C-MOS Design Tradeoffs

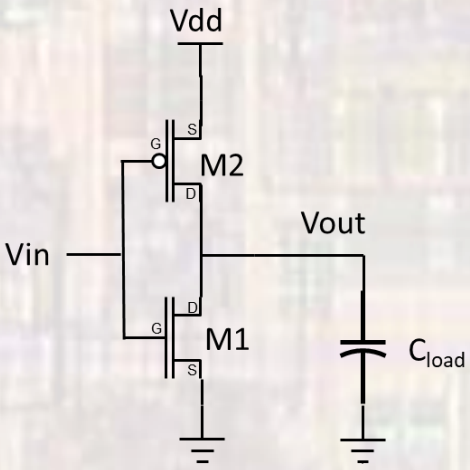
Last updated 12/23/23

Design Tradeoffs: speed-power

- Total power
  - α – proportion of clock intervals actually switching
  - β – leakage factor

$$P = P_{DC} + P_{SW} + P_{Shoot}$$

$$P = \beta V_{DD} + \alpha C_{load} V_{DD}^2 F + \alpha I_{peak} V_{DD} \left(\frac{t_r + t_f}{2}\right) F$$



All terms a function of V_{DD}

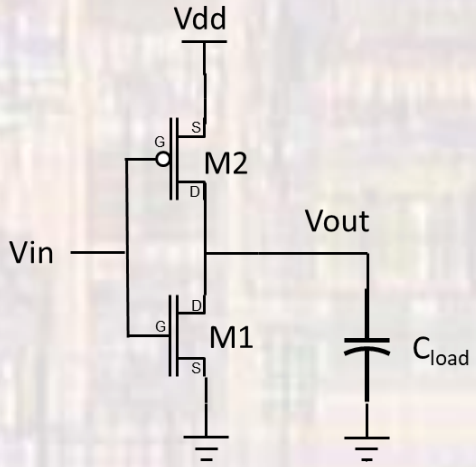
Design Tradeoffs: speed-power

- Power – Speed Tradeoff

Speed:

$$F \propto \frac{1}{t_{pd}} \qquad t_{pd} = \frac{C_{load}\, V_{DD}}{\frac{k'_n}{2}\frac{W}{L}(V_{DD} - V_t)^2} \propto \frac{1}{V_{DD}}$$

Speed (F) is proportional to V_{DD}/ C_{load}



Power:

$$P = \beta V_{DD} + \alpha C_{load} V_{dd}^2 F + \alpha I_{peak} V_{dd} \left(\frac{t_r + t_f}{2}\right) F$$

Power typically dominated by switching power, proportional to C_{load} * V_{DD}^2 * F

Design Tradeoffs: speed-power

- Power – Speed Tradeoff
  - Speed(F) $\propto$ V_{DD} / C_{load} but Power $\propto$ $C_{load} * V_{DD}^3$
    - Can't have both low power and fast circuits
  - Saved by technology advancements
    - Smaller geometry ICs have:
      - Lower logic gate capacitances → smaller loads to drive
      - Shorter channel lengths → Higher drive capability
    - Speed(F): $C_{load} \downarrow$ → F ↑
    - Power: $C_{load} \downarrow$ → P ↓

To date, the technology advancements have provided enough speed improvement to allow V_{DD} to be reduced → reduced power

Design Tradeoffs: speed-power

- Power – Speed Tradeoff
  - While technology improvements have allowed fast processors at low voltages, this is limited
  - The solution is to use multiple processors in parallel
    - Laptop – 4 cores
    - Only run them when needed
  - Lots of strategies
    - Dynamic Voltage and Frequency Scaling (DVFS)
    - Big/Little
  - High performance cores today
    - V_{DD} = 0.8V – 1.2V
    - F_{clk} = 3-4GHz

Design Tradeoffs: area - performance

- Matched switching points →
  - large gate sizes → slower operation
  - Higher drive, higher load capacitances
- Matched NAND/NOR gate t_{PD} →
  - large gate sizes → slower operation
  - Higher drive, higher load capacitances
- Minimum gate sizes →
  - large discrepancies in t_{PD}
  - Unmatched switching points
  - Lower drive, lower load capacitance

Design Tradeoffs: area - performance

- Need multiple versions of commonly used gates
  - Minimum gates for low frequency circuits where the variations in t_{PD} and switching points don't matter
  - Speed optimized gates for high frequency circuits
    - Require additional area
  - Scaled gates to drive long wires or external loads
  - High power (very large) gates to manage large current situations
    - Power gating