C-MOS Inverter

Last updated 12/23/23

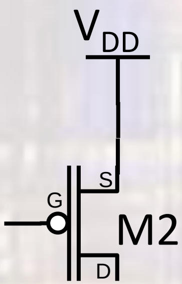
C-MOS Inverter

- MOSFET Digital Configuration – body connections
  - P-MOS body tied to V_{DD}

  - N-MOS body tied to Gnd

C-MOS Inverter

- MOSFET Digital Configuration
  - Nominal source connections



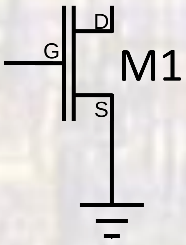
P-Channel

V_G low:

M2 is ON → M2-drain = V_{DD}

V_G high:

M2 is OFF → M2-drain = open



N-Channel

V_G low:

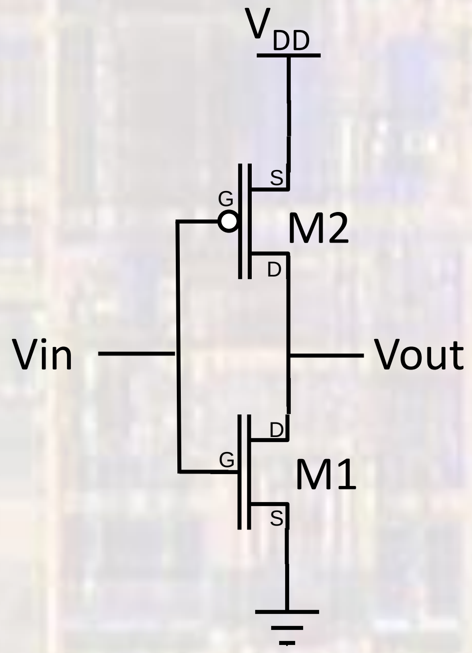
M1 is OFF → M1-drain = open

V_G high:

M1 is ON → M1-drain = Gnd

C-MOS Inverter

- MOSFET Digital Configuration - Inverter



Vin low:

M1 is off → $M1_D$ = open
M2 is on → $M2_D = V_{DD}$
Vout = V_{DD}

Vin high:

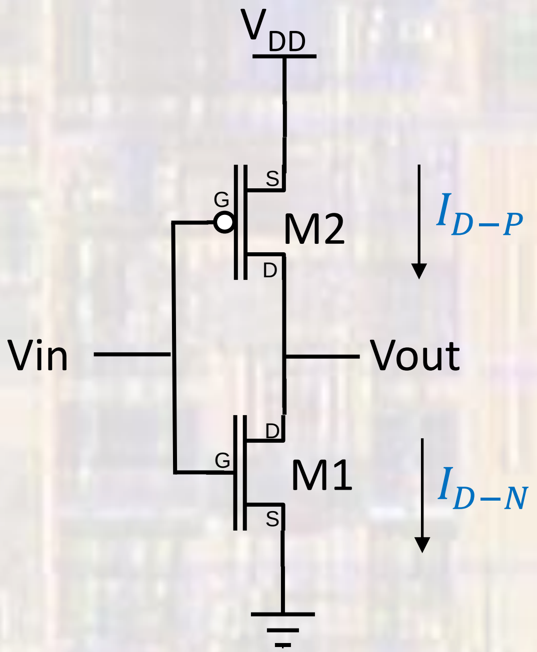
M2 is on → $M2_D$ = open
M1 is off → $M1_D$ = Gnd
Vout = Gnd

Truth Table

IN	OUT
0	1
1	0

C-MOS Inverter

- Inverter – Qualitative – DC
  - Assume $V_{Tn} = V_{Tp}$, and $V_{DD} >> V_T$



Vin low:

$V_{GS\text{-}M1} = 0$ → M1 Cutoff → $I_{DS\text{-}M1} = 0$ → M1 is off

$V_{SG\text{-}M2} = V_{DD}$ ($> V_{tp}$) → Linear or Saturated

M1 off → $I_{DS\text{-}M1} = 0$ → $I_{SD\text{-}M2} = 0$ → M2 Linear

→ $V_{SD\text{-}M2} = 0$

Confirm M2 Linear
$V_{SD} < V_{SDsat} = V_{SG} - V_{Tp}$

Vout = V_{DD}

Vin high:

$V_{SG\text{-}M2} = 0$ → M2 Cutoff → $I_{SD\text{-}M2} = 0$ → M2 is off

$V_{GS\text{-}M1} = V_{DD}$ ($> V_{tn}$) → Linear or Saturated

M2 off → $I_{SD\text{-}M2} = 0$ → $I_{DS\text{-}M1} = 0$ → M1 Linear

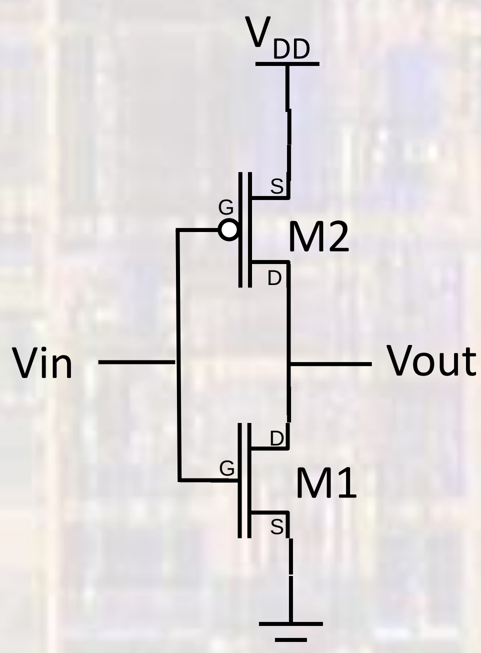
→ $V_{DS\text{-}M1} = 0$

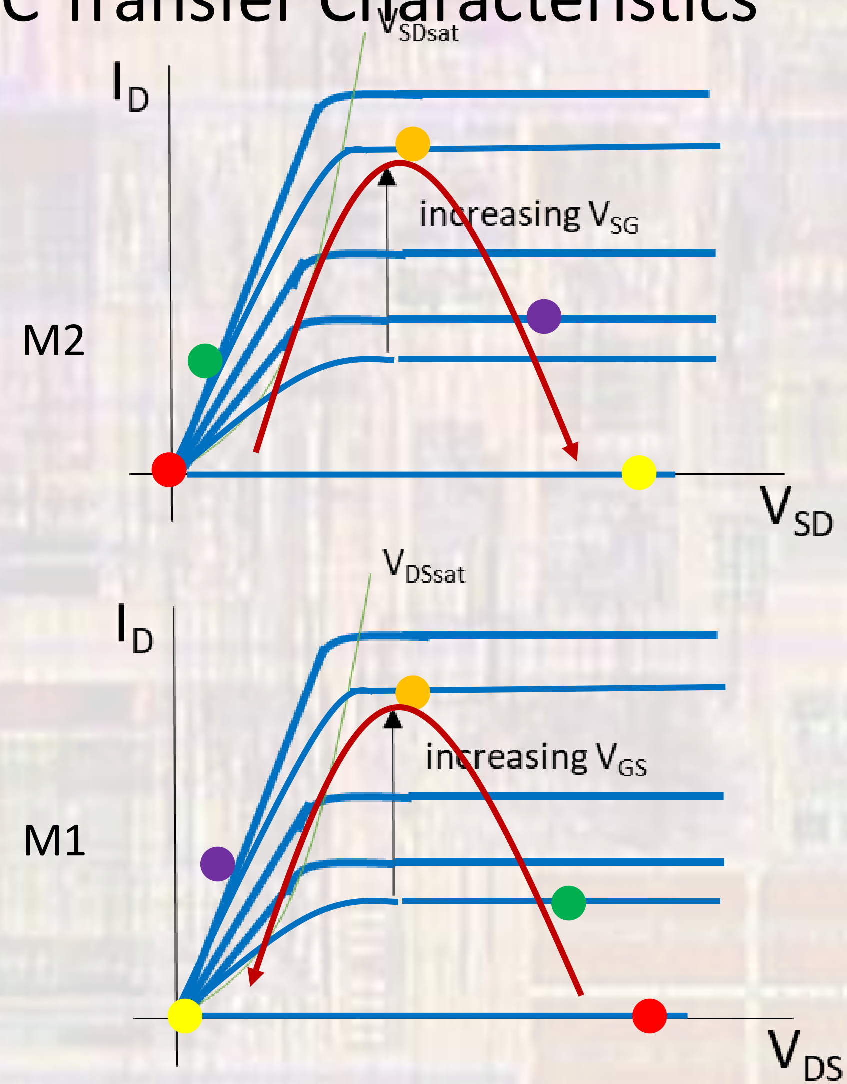
Vout = Gnd

Confirm M1 Linear
$V_{DS} < V_{DSsat} = V_{GS} - V_{Tn}$

C-MOS Inverter

- Inverter – Qualitative – DC Transfer Characteristics





Vin: < V_{Tn} (red)

Vin: > V_{Tn} , < $V_{DD} - V_{Tp}$, Vout > $V_{DD}/2$ (green)

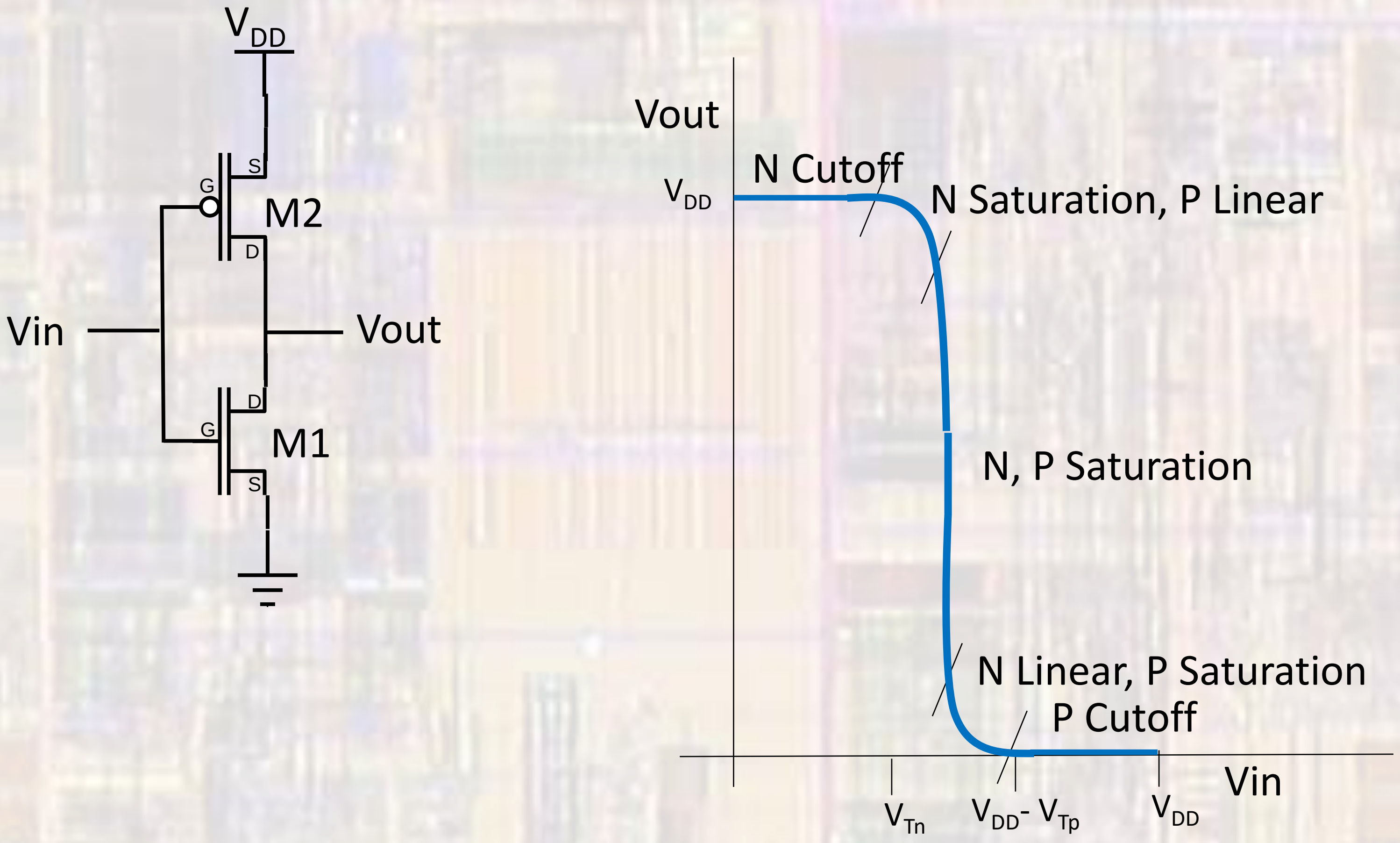
Vin: > V_{Tn} , < $V_{DD} - V_{Tp}$, Vout = $V_{DD}/2$ (orange)

Vin: > V_{Tn} , < $V_{DD} - V_{Tp}$, Vout < $V_{DD}/2$ (purple)

Vin: > $V_{DD} - V_{Tp}$ (yellow)

C-MOS Inverter

- Inverter – Qualitative – DC Transfer Characteristics



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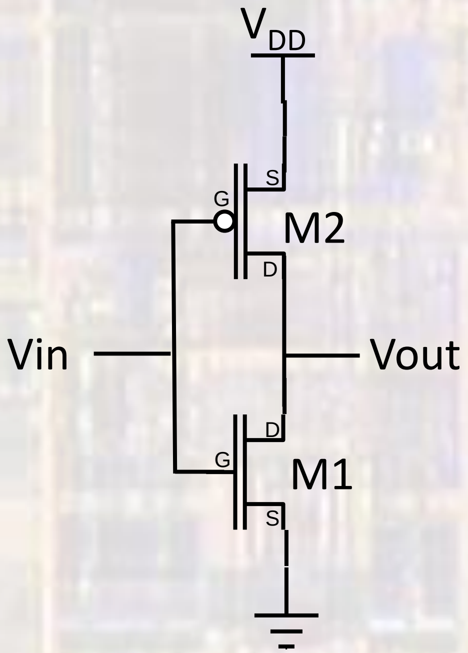
- Inverter - Design



Assuming Vdd is big enough to keep M2 and M1 in saturation at the switching point: $I_{D\text{-}M1} = I_{D\text{-}M2}$

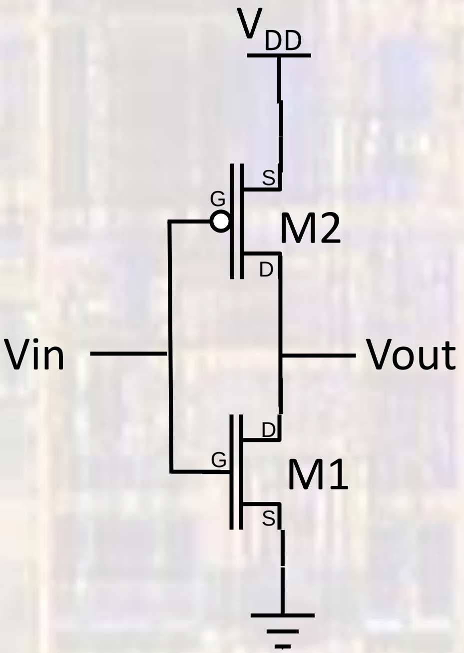
$$\frac{k'_p}{2}\frac{W2}{L2}\left(V_{sg2} - V_{tp}\right)^2 = \frac{k'_n}{2}\frac{W1}{L1}\left(V_{gs1} - V_{tn}\right)^2$$

Desire a consistent switching point: Vin = Vout = Vdd/2

$$\frac{k'_p}{2}\frac{W2}{L2}\left(V_{dd}/2 - V_{tp}\right)^2 = \frac{k'_n}{2}\frac{W1}{L1}\left(V_{dd}/2 - V_{tn}\right)^2$$

C-MOS Inverter

- Inverter – Design – cont'd



Manipulating the equation

$$\frac{W1/_{L1}}{W2/_{L2}} = \frac{k'_p}{k'_n}\left(\frac{V_{dd}/2 - V_{tp}}{V_{dd}/2 - V_{tn}}\right)^2$$

If we make $V_{tp} = V_{tn}$, V_{dd} drops out of the equation

$$\frac{W1/_{L1}}{W2/_{L2}} = \frac{k'_p}{k'_n}$$

And the switching point remains $V_{dd}/2$ regardless of V_{dd}

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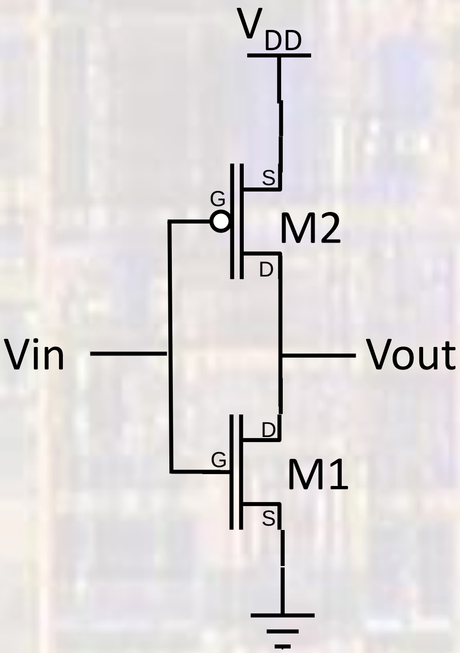
- Inverter – Design – cont'd



Earlier we saw k'_n = ~3 x k'_p

In a typical CMOS digital technology $L_P = L_N$

$$\frac{W1/_{L1}}{W2/_{L2}} = \frac{W_N/_{L_N}}{W_P/_{L_P}} = \frac{k'_p}{k'_n}$$

Resulting in W_P = ~3 x W_N

With $L_P = L_N$, and $W_P = 3 \times W_N$ the current drive of the N and P are the same → switching point = $V_{DD}/2$ →
design is consistent with rising and falling inputs

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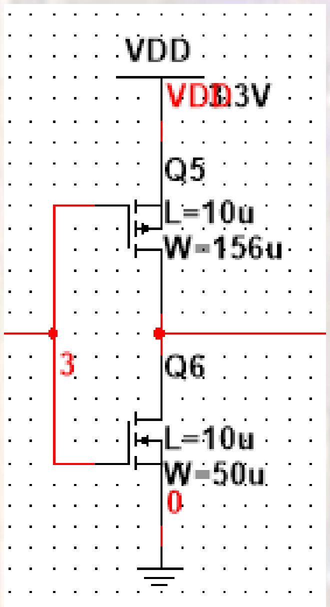
- Inverter - Design



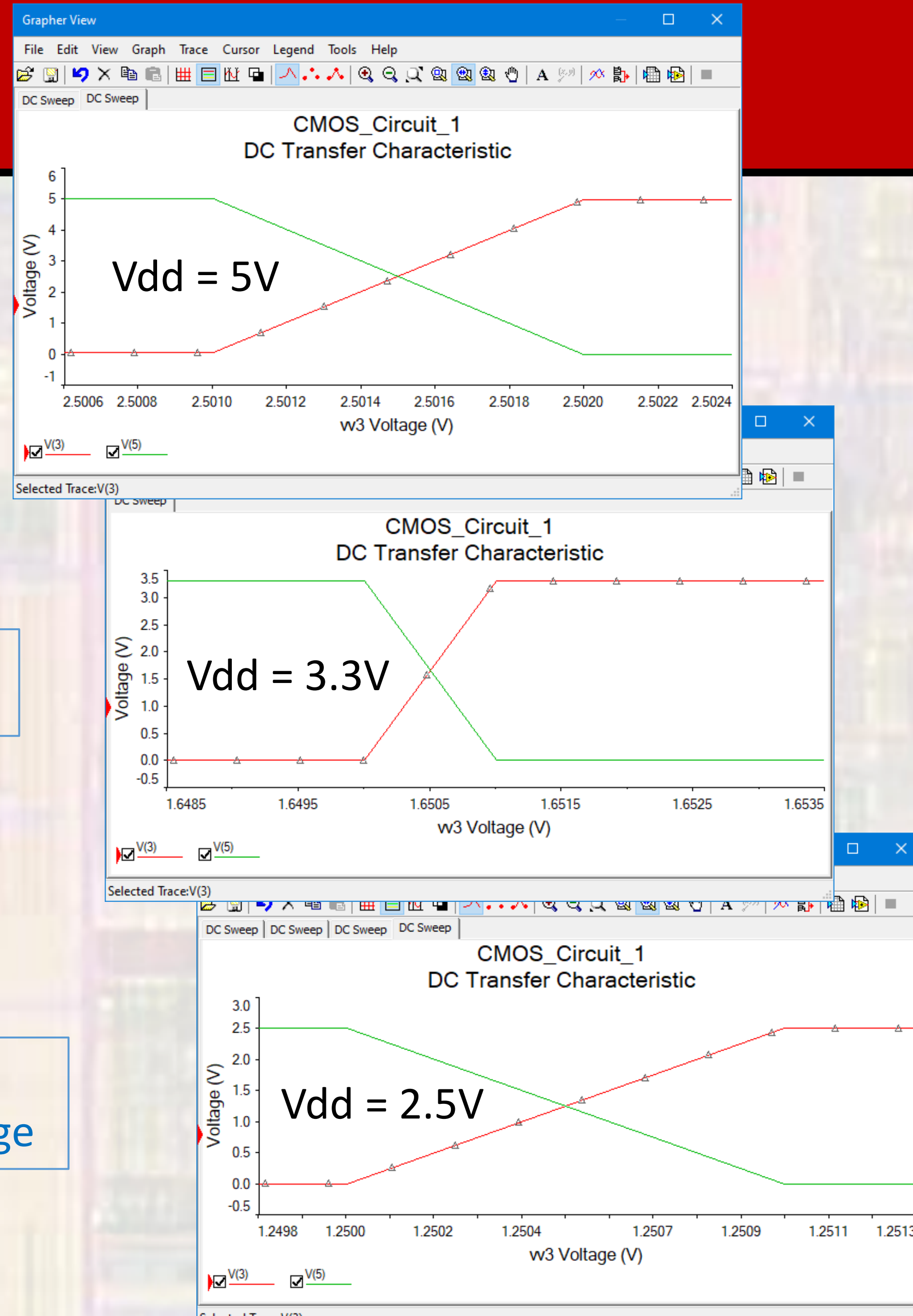
Vtn = 1V

Vtp = 1V

k’n = $14uA/V^2$

k’p = $4.5uA/V^2$

In this case the ratio is 14/4.5 instead of 3



The circuit switches at VDD/2 regardless of the supply voltage