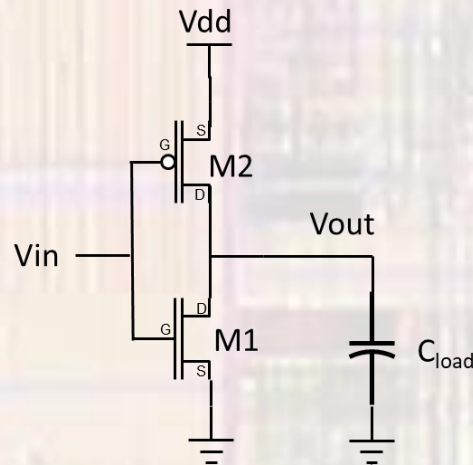


C-MOS Power

Last updated 12/23/23

C-MOS Power

- 3 Major power components
 - DC power
 - Switching Power
 - Shoot-Through



C-MOS Power

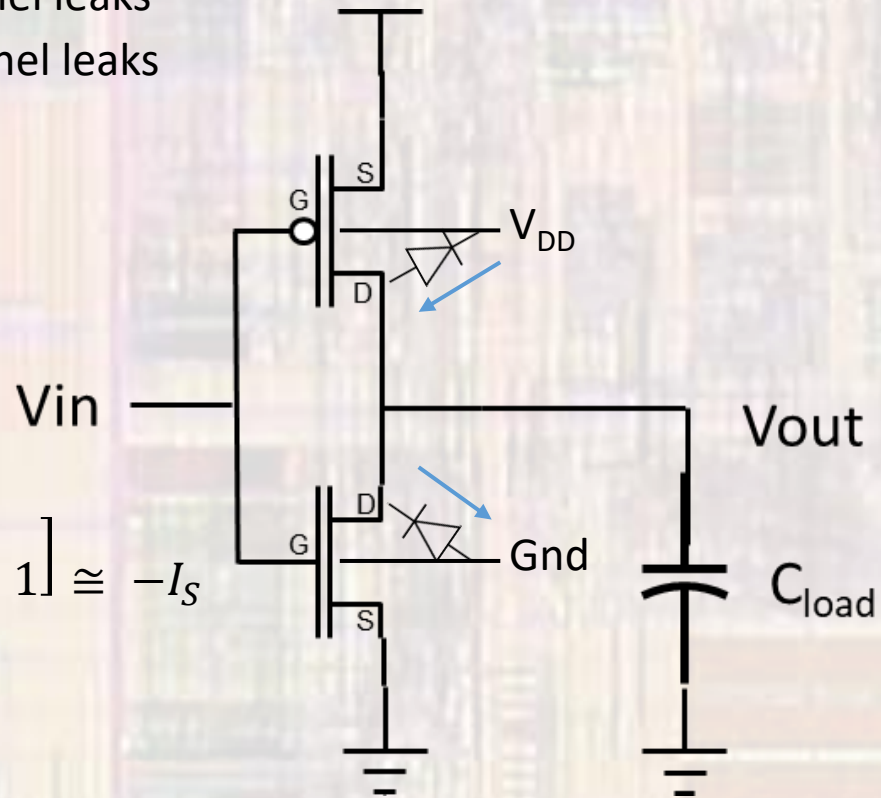
- DC power
 - Junction leakage (Drain to Body)
 - Reverse diode leakage
 - $V_{out} = 0$ P-channel leaks
 - $V_{out} = V_{DD}$ N-channel leaks

$$\text{Power} \cong I_S \times V_{DD}$$

Power is proportional to V_{DD}

$$I_D = I_S \left[e^{\left(\frac{V_A}{nV_T}\right)} - 1 \right] = I_S \left[e^{\left(\frac{-V_{DD}}{nV_T}\right)} - 1 \right] \cong -I_S$$

$$I_D \cong -I_S \quad \text{for } V_{DD} \gg V_T$$



C-MOS Power

- Switching Power

- Charging / Dis-charging the load and parasitic Cs
- Can cause noise in V_{DD} and Gnd

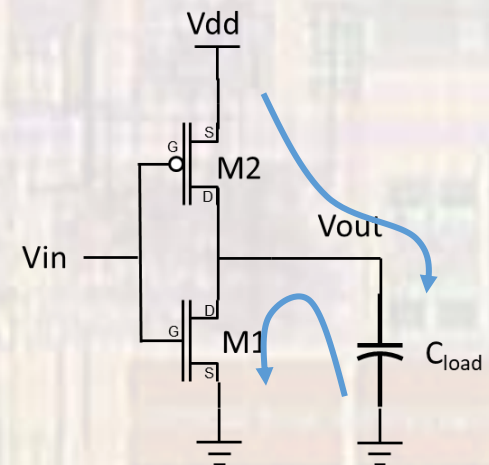
$$E = \int_0^{\infty} i(t)V_{out}dt = \int_0^{\infty} C \frac{dv}{dt} V_{out}dt = \int_0^{V_{dd}} CV_{out}dv = \frac{1}{2} CV_{DD}^2$$

- Worst case

- Rise and fall with every clock edge
- C_{load}^* includes parasitic capacitances

$$P = C_{load}^* V_{DD}^2 F$$

Power is proportional to V_{DD}^2

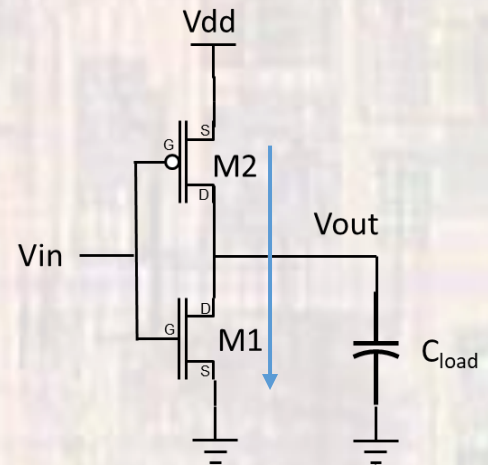


C-MOS Power

- Shoot-Through
 - Short period of time when both devices are on
 - Current from V_{DD} to Gnd
 - Can cause noise in V_{DD} and Gnd

$$P = I_{peak} V_{dd} \left(\frac{t_r + t_f}{2} \right) F$$

Power is proportional to V_{DD}



C-MOS Power

- Total power
 - α – proportion of clock intervals actually switching
 - β – leakage factor (number of gates * leakage current)

$$P = P_{DC} + P_{SW} + P_{Shoot}$$

$$P = \beta V_{DD} + \alpha C_{load} V_{DD}^2 F + \alpha I_{peak} V_{DD} \left(\frac{t_r + t_f}{2} \right) F$$

All terms a function of V_{DD}

